Insulating IGBT Driver with PCB integrated capacitive coupling elements
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Abstract
In many power electronic applications galvanic isolating IGBT/MOSFET drivers are advantageously used. The main reasons are safety issues, driving high voltage power semiconductors with blocking voltages of typically 600 V or above and avoiding or minimizing unwanted ground current loops. This paper deals with a new method for achieving galvanic isolation in high voltage drivers based on printed circuit board (PCB) integrated capacitive coupling elements. The suggested coupling element consists of a pair of plate capacitors by using copper layers and prepregs of a PCB. First, the influence of the isolation barrier capacitance, which is one of the main important parameters of a galvanic isolating driver, is illustrated by a simple model of the capacitive current loop. As a result it is stated that the coupling capacitance should be lower than 5 pF to achieve high dV/dt levels of at least 100 kV/μs. Taking into account the isolation characteristics of the commonly used FR4 PCB material, an integrated capacitive coupling element can be designed. With 360 μm isolation distance and a plate surface of approximately 8 mm², a capacitance of about 1 pF is achieved. A comparison of the developed capacitive coupling element with a comparable inductive coupling element (transformer) shows that the former has advantages due to a much lower current consumption and less dependency on parasitic inductances. In order to achieve high isolation voltages on PCBs, wide creepage and clearance distances are required, especially at higher humidity levels. It is advisable to use special layout were the primary and the secondary circuits of the driver are placed on different sides on the PCB by using blind vias. The well known Manchester coding can be applied to use the advantages of phase modulated signals for transmitting the switching signal over the isolation barrier. By transmitting the carrier signal via a second capacitive coupling element, the complexity for decoding the switching signal is reduced. A half bridge driver was built up to verify the new isolation method. Herewith a bidirectional buck-boost DC/DC converter operating at a DC link voltage of 400 V was successfully controlled. Moreover, measurements with a standardized burst generator have shown, that a fail-safe operation is possible up to high dV/dt levels.

1 Introduction
Generally speaking, galvanic isolation can be achieved by using the characteristics of a magnetic field, an electrical field, an electromagnetic field or by mechanical coupling (with piezoelectric ceramics). Regarding to driver applications for power semiconductors (MOSFETs or IGBTs) up to approx. 1700 V blocking voltage the typical isolating coupling element for signal transmission is the transformer, using magnetic coupling. Higher blocking voltages usually require electromagnetic coupling by using fibre optics. Whereas, up to approx. 600 V blocking voltage, all principals are covered by well known technical solutions: magnetic coupling with discrete placed, wire wound, planar or IC integrated transformers, or magneto-resistive devices, electric coupling with IC integrated capacitive coupling elements and electromagnetic coupling with opto-couplers [1-5]. Piezoelectric drivers are under research [6].

All these devices are placed on a PCB with very good isolation qualities. The minimum electrical strength of the typically used FR4 material is 30 kV/mm. Moreover, galvanically insulating coupling elements can be integrated on a PCB by using spiral coils for transformers or plate capacitors for electrical coupling elements very easily. The question at this point is how to realize a compact and fail-safe signal transmission for gate drive applications with PCB integrated capacitive coupling elements. The answer hereon will be subject of the following chapters.

2 Isolation capacitance
First, the effect of the isolation barrier capacitance will be analyzed.

2.1 Displacement currents
Considering state of the art coupling elements for signal transmission, an isolation capacitance in the range of 1 to 3 pF will be obtained for devices in SO8 packages. Assuming that the isolation capacitance $C_{iso}$ is dominant for common-mode voltage transients $dV_{CM}/dt$, a displacement current $I_{CMT}$, calculated by:

$$I_{CMT} = C_{iso} \cdot \frac{dV_{CM}}{dt},$$  \hspace{1cm} (1)

can be observed. Fig. 1 shows the result of Eq. (1) for different values of $C_{iso}$ and for different common-mode voltage transients in the range of 10 kV/μs up to 400 kV/μs. Driver applications for power semiconductors require a high common-mode voltage transient immunity. The target area (marked in Fig.1) is thus limited by a minimum value of 100 kV/μs [2].
Assuming that the displacement current $I_{CMT}$ should be less than 500 mA, Fig. 1 shows that the maximum isolation capacitance must be lower than 5 pF. In the following section, a more detailed analyze of the capacitive current loop is presented.

### 2.2 Capacitive current loop

Figure 2 shows a simplified model of the capacitive current loop for a galvanically isolating high side driver in a half bridge application.

In the model shown in Fig. 2, the capacitive current loop is closed by capacitors $C_5$, $C_6$, $C_7$ and an electrical conductive chassis (or by a cooling device for mounting the power semiconductors). The coupling device is pictured as an electric quadrupole and the capacitors $C_5$, $C_4$ on both sides are indicating that the displacement current flows over each pin of the coupling element. That means that $C_3$, $C_4$ must be much larger than the isolation capacitances $C_1$, $C_2$. The same assumption also applies for $C_5$, $C_6$, $C_7$ which are representing all parasitic capacitors between the high side driver and the chassis. Measurements on real systems show that usually there is a capacitance of much more than 100 pF between any point of a power circuit and the chassis. That means that the isolation capacitance $C_{iso}$ ($C_1$||$C_2$) dominates the displacement current $I_{CMT}$. Fig. 3 shows the model presented in Fig. 2 as an electrical circuit simulation model (LTspice). The control unit is represented by an output stage V2 with an internal resistance of 100 ohm. In assumption that the connection between control unit and gate driver is very short, the lead inductance is about 10 nH (at 1 nH/mm inductance per unit length). The driver input capacitance $C_{IN}$ is 20 pF, achieving a maximum input signal delay of 10 ns (for 5τ). The half bridge is represented by a disturbance voltage source $V1$.

Figure 4 shows the simulation result for a 100 kV/μs common-mode voltage transient with two different isolation capacitances (2 pF and 5 pF). With a total isolation capacitance $C_{iso}$ of 2 pF and a common-mode voltage transient of 100 kV/μs a displacement current of 200 mA can be expected (see Fig. 1) which could be verified by simulation (Fig. 4). Fig. 4 shows, that with the beginning of the common-mode voltage transient the voltage level at the input logic is disturbed. With an isolation capacitance of 5 pF, which means a displacement current of approx. 500 mA, the unwanted voltage glitch comes near the driver input threshold values. Therefore, it
is advisable to use an isolation capacitance lower than 5 pF for a PCB integrated capacitive coupling element.

3 PCB integrated coupling elements

Figure 5 shows one possibility to realize PCB integrated coupling elements. On the left-hand side a capacitive coupling element is shown, consisting of two plate capacitors with an overall plate surface of $2A_{\text{cap}}$ and plate distance $d$. On the right-hand side an inductive coupling element (transformer) is shown, consisting of two planar spiral coils with same distance $d$, which can be simultaneously used for a galvanically isolated voltage supply [7].

![Figure 5 PCB integrated capacitive coupling element (left), PCB integrated inductive coupling element (right)](image)

3.1 Comparison of PCB integrated capacitive and inductive coupling elements

Inductive coupling elements in the form of signal transformers are well known and widely used for isolated signal transmission [1-3]. In the following section the advantages of using a PCB integrated capacitive coupling element for signal transmission compared with an inductive one with same PCB area will be explained. For example: with a given PCB area $A_{\text{ind}}$ equal to $2A_{\text{cap}}$ of 36 mm², a plate and coil distance $d$ of 360 μm, a minimum trace width and distance $a_{\text{min}}$ of 150 μm and a typical value of 4.5 for the permittivity of FR4, the maximum capacitance and inductance of the coupling elements shown in Fig. 5 can be calculated with:

$$C_{\text{max}} = \frac{A_{\text{cap}} \cdot \varepsilon_0 \cdot \varepsilon_r}{d},$$

$$L_{\text{max}} = \left( \frac{0.29 \text{ nH}}{\text{mm}} \right) \left( \frac{A_{\text{ind}}}{\pi} \right)^{\frac{3}{2}} \cdot 2 \cdot a_{\text{min}}^{\frac{3}{2}}. \tag{3}$$

(Eq. (3) is derived from Eq. (1) in [7]). In Eq. (3) $A_{\text{ind}}$ and $a_{\text{min}}$ must be used in mm) For $C_{\text{max}}$ a value of 2 pF and for $L_{\text{max}}$ a value of 250 nH will be obtained. In the following simulation both elements will be compared. A coupling factor $k$ of 0.8 is assumed for the inductive element (what means a leakage inductance of 90 nH). Due to the same PCB area and the minimum trace width the isolation capacitance of the inductive coupling element can be assumed as equal. Fig. 6 shows the electrical simulation model (LTspice). To stress the positive dynamic behaviour an additional leakage inductance of 90 nH is connected in series to the capacitive coupling element.

![Figure 6 PCB integrated ind. coupling element (top), PCB integrated capacitive coupling element (bottom)](image)

The simulation result given in Fig. 7 shows that the current consumption of the capacitive coupling element is much lower. Moreover, despite an additional leakage inductance the wave form of the output signal ($V_{\text{cap}1}$-$V_{\text{cap}2}$) of the capacitive coupling element is much smoother.

![Figure 7 Current consumption (top), Output signals of the coupling elements (bottom)](image)

By using a faster driver stage, the additional unwanted ringing of the output signal of the inductive coupling element would be much more intensive. In the simulation above the rising and falling time of the driver stage (source $V1$) is 1 ns. That means, the advantages of the PCB integrated capacitive coupling element are a lower current...
consumption and a less dependency on parasitic inductances - if same PCB area is assumed.

3.2 Signal transmission

The usage of PCB integrated capacitive coupling elements in gate drive applications requires a fail-safe signal transmission method. By using the well known Manchester coding it is possible to transmit the gate control signal permanently and change it any time without delay. In order to minimize the effort for decoding the output signal of the coupler at the secondary side of the driver, it is proposed to transmit the carrier signal by a separate capacitive coupling element. Fig. 8 shows the proposed circuit for coding and decoding at a glance.

![Diagram](image)

**Figure 8** Proposed circuit for using PCB integrated capacitive coupling elements in gate drive applications

In Fig. 9 the principal behaviour of the proposed circuit is presented.

![Diagram](image)

**Figure 9** Gate control signals \( V_1, V_2 \) and transmitted signals of the proposed Manchester coding

It shows the gate control signal \( V_1 \), the both Manchester coded signals \( V_{R1} \) and \( V_{R2} \) at the secondary side of the driver circuit, as well the shaped digital signals \( V_{\text{comp1}}, V_{\text{comp2}} \) of \( V_{R1} \) and \( V_{R2} \). Using a logic EXOR relation of \( V_{\text{comp1}} \) and \( V_{\text{comp2}} \) the gate control signal \( V_2 \) can be easily reconstructed at the secondary side of the driver. The circuit elements \( R_1, R_2, R_3, R_4 \) and \( C_3 \) (shown in Fig. 8) are used for filtering the transmitted signal and avoiding a voltage drop of \( V_{R1}, V_{R2} \) to zero level.

4 Verifying the proposed circuit

The proposed circuit shown in Fig. 8 is verified by realizing an IGBT half bridge driver with PCB integrated capacitive coupling elements as presented in Fig. 10. The dimensions of the prototype are 67 mm x 30.5 mm with a maximum height of 4.7 mm (without connector).

![Prototype](image)

**Figure 10** Prototype of an IGBT half bridge driver with PCB integrated capacitive coupling elements

In Fig. 10 the used area for the capacitive signal transmission is marked with dashed lines. Within are realized: the signal coding unit, four PCB integrated capacitors with a surface of approx. 8 mm² per capacitor and 360 μm isolation distance and the signal decoding unit. The two secondary sides of the half bridge driver are supplied by a PCB integrated transformer and the power devices are driven by a resonance voltage clamped circuit as proposed by Zeltner at the CIPS 2008 [7].

The calculated capacitance for one PCB integrated capacitor is 0.9 pF (Eq. (2)). The measured capacitance is with 1.2 pF only slightly higher than the calculated value. The difference is based on the additional signal traces for connecting the PCB integrated capacitors.

The prototype shown in Fig. 10 uses a standard four layer PCB with a thickness of 1.6 mm, without blind and buried vias. Getting 360 μm isolation distance only one plate of the PCB integrated capacitors is inside the PCB (layer 2). Achieving high isolation voltages on PCBs wide creepage and clearance distances are required, especially at higher humidity levels. For example, a distance of 3 mm would be necessary for 600 V applications (pollution degree two) to avoid creepage currents. Thus, a special layout is suggested, were the primary and the secondary circuits of the driver are placed on the top side and on the bottom side of the PCB, using blind (and buried) vias. Fig. 11 illustrates the proposed scheme. In order to minimize additional parasitic capacitive coupling, primary and secondary driver circuitry should not overlap.
Using the proposed layout of Fig. 11, the necessary creepage distance must be kept in mind only at the edges of the PCB. The advantages of the proposed solution are compactness and cost efficiency - particularly for isolations requirements above 600 V.

Figure 12 shows an oscillogram of the received transmission signals at the secondary side of the driver.

Channel 1 and 2 are showing the comparator output signals, verifying the theoretical signal curves of Fig. 9. For the prototype a carrier frequency of 1 MHz is used. Channel 3 shows the output signal of the logic EXOR gate. Due to slightly different delays in the two signal paths and slightly different comparator threshold values, voltage spikes can be observed at every transient of $V_{\text{comp1}}$ and $V_{\text{comp2}}$. Hence an additional low-pass filter at the output of the logic EXOR gate is necessary. The negative aspect is an additional and unwanted signal delay. But this problem can be solved by using adequate ASICs. Channel 4 shows the output signal of the bottom driver unit charging and discharging an equivalent gate load of 22 nF.

With an additional low-pass filter at the output of the logic EXOR, causing a delay of approx. 1 μs, the common-mode transient immunity was measured with a standard burst generator (Schlöder SFT 4000). Fig. 13 shows the measurement setup. The driver input signals have been held constant during measurement (clamped to VCC or GND).

In Fig. 14 the measurement result is presented using a burst signal of 1.2 kV. The measured driver output signal (on capacitor $C_{\text{eq}}$, see Fig. 13) remains constantly low in the moment of disturbance. With a rising time of 5 ns for the interference spike, this means a common-mode transient immunity of 240 kV/μs.

Figure 15 shows an additional measurement setup where the developed IGBT driver is driving a buck-boost DC/DC converter consisting of an half bridge topology (IGBT/SiC-diode), two DC link capacitors and a power coil. A first pulse generator produces the switching frequency of 200 kHz with 53 % duty cycle. In order to simplify the measurement setup it is possible to switch between the bottom driver unit input and the top driver unit operating either in buck mode or in boost mode. The DC link voltage is 400 V at the high voltage side and 200 V at the low voltage side.

Figure 16 shows a photo of the buck-boost DC/DC converter measurement setup.
In Fig. 15 the measurement result is presented.

Figure 15 Buck-boost converter measurement setup

The oscillogram show on channel 1 and 2 the gate drive signals measured on the top and bottom power switch respectively. Channel 3 shows the drain-source voltage measured on the bottom IGBT (with a maximum dV/dt of 44 kV/μs). On channel 4 the load current through inductor L1 is measured. The correct function of the buck-boost converter, controlled by the developed IGBT driver, can be verified through the measured wave forms.

5 Summary

In conclusion a new method for achieving galvanic isolation in high voltage drivers based on printed circuit board (PCB) integrated capacitive coupling elements is presented. The influence of the isolation capacitance is shown by analyzing a simple model of the capacitive current loop. A comparison of PCB integrated inductive (transformer) and capacitive coupling elements with same PCB areas shows that latter can be advantageously used for isolated signal transmission due to a lower current consumption and less dependency on parasitic inductances. The Manchester coding is proposed to achieve a fail-safe signal transmission. A special layout is presented, using blind vias to minimize the PCB area for creepage and clearance distances. The new isolation method was verified by building up an IGBT half bridge driver. Herewith a bidirectional buck-boost DC/DC converter, operating at a DC link voltage of 400 V, was successfully controlled. Moreover, measurements with a standardized burst generator have shown that the gate drive signal remains constant up to a dV/dt level of 240 kV/μs. Finally it should be mentioned that the developed IGBT driver is a prototype. For industrial application much more development effort would be necessary especially to improve the signal coding and decoding unit, as well as to reduce the number of discrete elements by using adequate ASICs.

6 Literature

[1] S. Pawel, J. Thalheim: Getting into Shape, High frequency gate drive module features ultra-flat design, Bodo’s Power Magazine Nov. 08, ISSN 1863-5598