

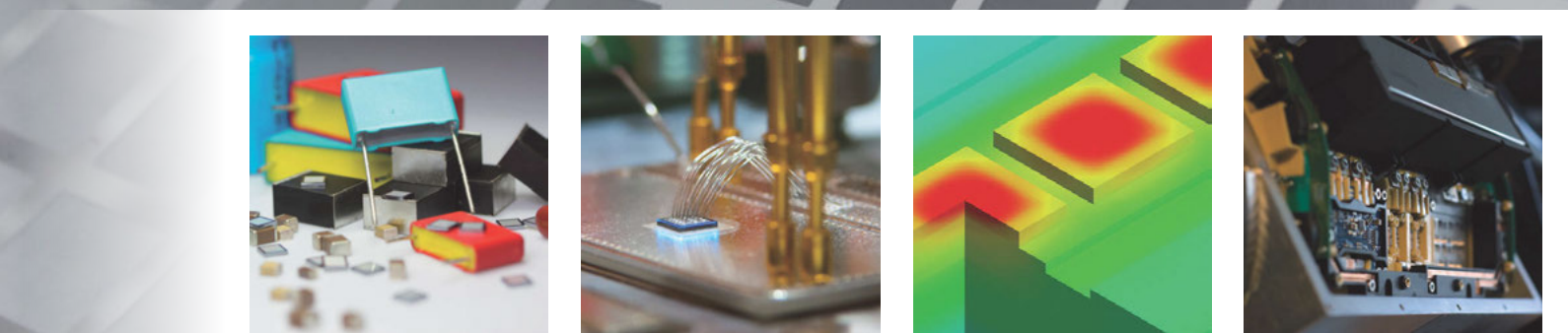
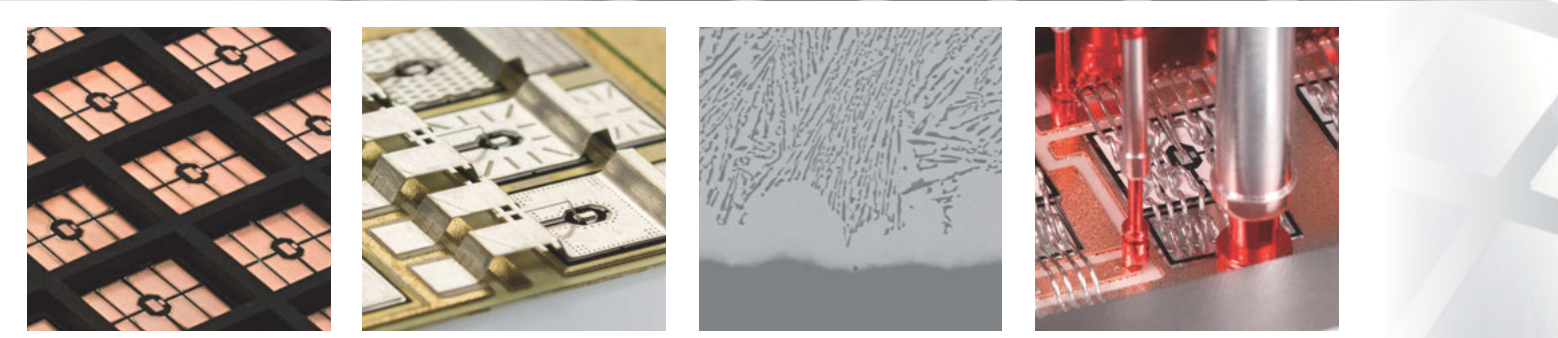


# Fraunhofer

## IISB

FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY

# DEVICES AND RELIABILITY



**BY CAR** Due to the limited number of parking space, we recommend arrival with public transportation. Car park at central railway station, then with line 5 tram to Christuskirche, or car park at Kaufhof, access by Landgrabenstraße (5 minutes by foot to the „Energie-Technologisches Zentrum“ etc).

**BY PLANE** From Nuremberg airport take the subway to central railway station, then with line 8 tram to Christuskirche.

**BY TRAIN** From Nuremberg central railway station use line 5 tram to Christuskirche or 12 minutes by foot.

### Fraunhofer Institute for Integrated Systems and Device Technology IISB

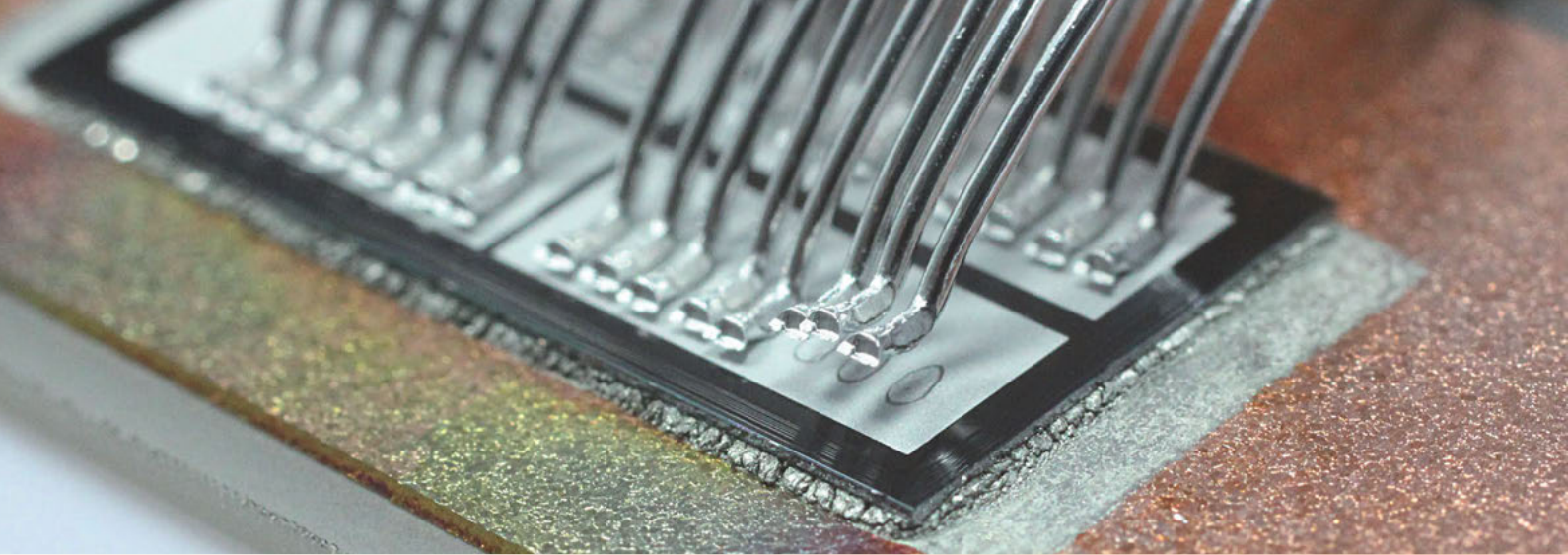
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## Devices and Reliability

The focus of the research and development work of the department “Devices and Reliability” is technology for power electronics. The activity is divided into three areas:

### Devices

The filed „Devices“ covers activities on monolithic integration of electron devices. For the development modern TCAD-simulation tools are used. The manufacturing of novel device prototypes is conducted in our CMOS line. A key focus is on the integration of passives and the development of new power semiconductor devices. In addition there is research on non-monolithic passive devices based on new dielectric materials, especially capacitors. Our micro- and nanoelectronic devices are implemented in power grid applications, in automotive electronics such as electric mobility as well as in the fields of biotechnology and medicine.

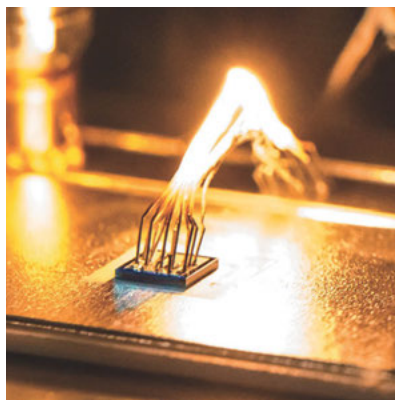
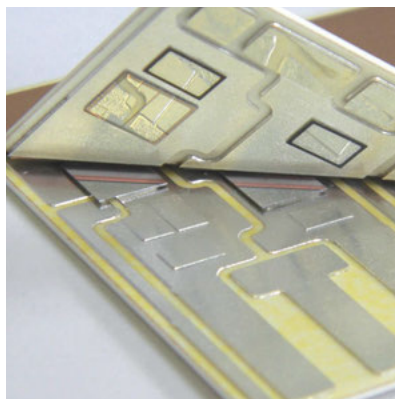
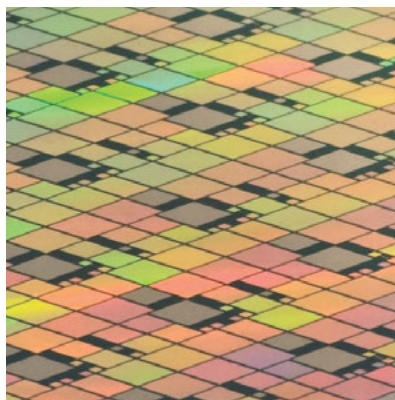
### Packaging

The second research field is packaging of power electronics. The drivers are performance, volume or weight per cost depending on the application. The goal is reached by investigations on different concepts of the electrical, mechanical and thermal design such as single and double sided die attach, single and double sided cooling, materials with minimized or matched coefficient of thermal expansion (CTE). By use of intelligent setups and application relevant choice of the electrical and thermal interconnections the bill of material can be minimized.

Work is done on joining technologies as well. The department has a long experience in silver sintering as an alternative to the state of the art. Meanwhile a process is established to manufacture multichip power modules with high yield. Especially a selective sintering process brings high advantages to electronic packaging. The chip sizes meet the power electronics requirements. While the sintering improvements are ongoing the soldering technology is still covered from state to the art up to new high performance or high temperature materials.

### Reliability and lifetime test

The third field of activity is the investigation of the lifetime of power electronics. Different tests are performed like power cycling, temperature cycling or humidity storage and may others. A huge variety of characterization and analyses tools are available such as for measurement of the thermal impedance of power devices, lock-in thermography, scanning acoustic microscopy, static and lock-in thermography, scanning electron microscopy, focused ion beam sectioning and others. The results are used to improve the technologies further. In addition they are utilized to parameterize existing or to create new lifetime models. The physics of failure method is addressed whenever possible. All activities are not limited to active devices only. Passive components are covered like inductors and capacitors as well as different potting materials.



### Devices – active and passives from sensors to power

- Silicon carbide power devices
- Passive devices for power electronics
- Circuit protection devices, fuses and anti-fuses
- Novel and exclusive fabrication capabilities for silicon (Si) and silicon carbide (SiC)
- Process simulation of device structures
- Reactive ion etching for fabrication of advances electron devices
- Integration of high k dielectrics into gate stacks
- Special metallization material stack of devices, change of the metallization of off-the-shelf wafers and dies

### Packaging concepts, technologies and prototyping for power electronics

- Evaluation of cooling concepts, liquid and air, single and double sided cooling, heat spreading
- Design for electrical, thermal, mechanical and lifetime constraints
- Low parasitic inductance commutation cells especially for SiC and GaN
- High temperature applications up to 300°C junction
- Silver sintering (pressureless and pressure assisted process for small and large areas)
- Soldering (void free soldering with paste and preform material)
- Wire and ribbond bonding (from 25µm gold wire to 500µm aluminum, copper or composites wires)

### Design verification from device to sytem

- Infrared thermography,  $R_{th}$  and  $Z_{th}$  measurements at device and system level
- Electrical characterizations

### Accelerated aging, lifetime, reliability

- Active temperature cycling with up to 1000 A
- Passive temperature cycling for common devices with two chamber shock oven in air
- Climate tests

### Analysis

- Metallography sections, focused ion beam sectioning
- Optical, electron and acoustic microscopy
- Lock-in thermography
- Statistics and lifetime prediction