Fraunhofer IISB

FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY

1 Operator with SiC wafer in front of horizontal oxidation furnace in cleanroom environment. Image: Kurt Fuchs / Fraunhofer IISB

SiC DEVICES

CUSTOM-TAILORED PROCESSES AND PROTOTYPES

Our objective

- Provide a one-stop solution for development and prototype fabrication of SiC devices

Features

- In-house device simulation, fabrication, and characterization
- Hands-on experience on power semiconductor devices across full value chain
- Complete in-house technology from epitaxy, implantation, and trench patterning to device packaging and module assembly in a fully equipped 100 mm SiC pilot line
- Fit for the future: 150 mm-ready SiC manufacturing equipment
- Quality management according to ISO 9001 and statistical process control

Advantages

- Feasibility check and feedback regarding design
- Short development cycles due to full π-Fab access
- Electrical characterization, dicing, and inking service
- Small-volume production available for customer specific devices

Benefits

- Less R&D costs and short time-to-market for your devices
- Reduced work effort due to all-in-one solution
- Competitive fabrication costs even at small volumes

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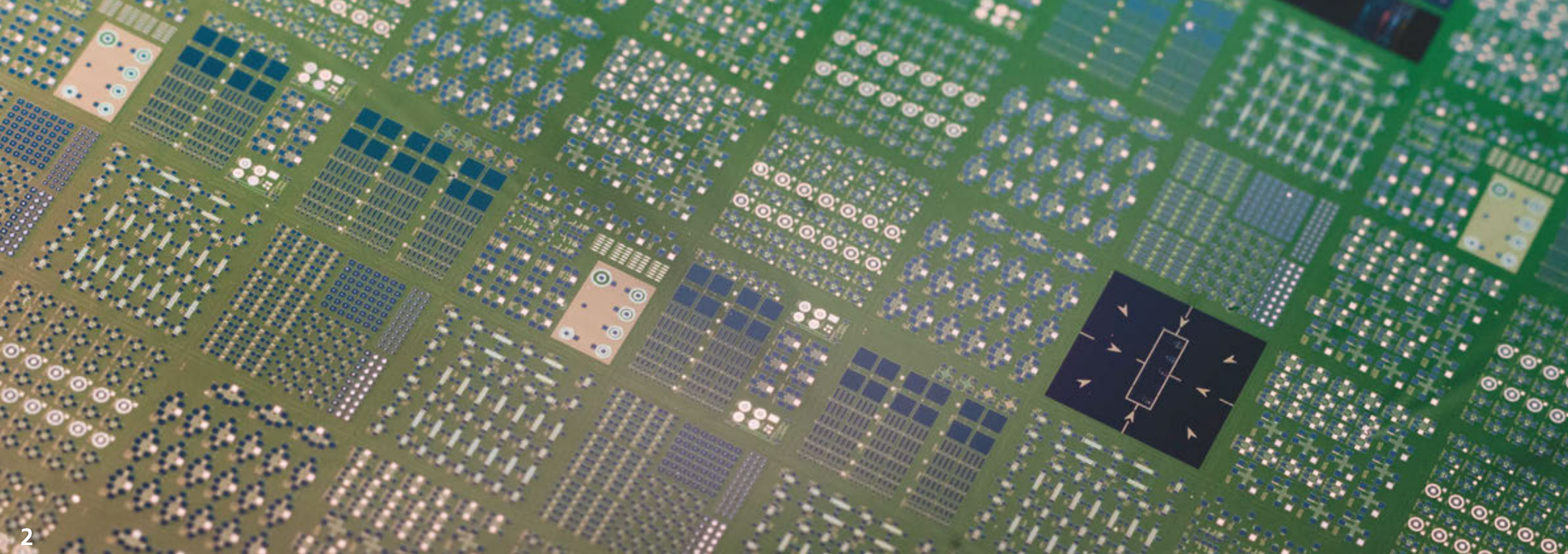

FRAUNHOFER IISB OFFERS R&D SERVICES ON SiC FROM MATERIALS DEVELOPMENT AND PROTOTYPE DEVICES TO MODULE ASSEMBLY AND MECHATRONIC SYSTEMS.

Prototype fabrication for power electron devices and detectors

Front-end processing

- Wet chemistry for cleaning
- Photolithography: Mask aligner and stepper for resolutions down to 0.8 µm
- Ion implantation up to 800 keV, with wafer heating (500 °C) up to 400 keV
- Advanced reactive ion etching of trenches in SiC
- Annealing (furnace and lamp heated) up to 1750 °C in various atmospheres
- Thermal oxidation in N_2O for high channel mobilities
- LPCVD, PECVD, and ALD for dielectric and polysilicon deposition

Metallization and packaging

- Contact formation (Ohmic and Schottky) by RTP
- Deposition and patterning of metallization layers for operation temperatures up to 500 °C
- Passivation by silicon based materials or polyimide
- Soldering and sintering processes as well as wire bonding for packaging

Electron devices and test patterns

- Design and fabrication of test structures
- Manufacturing of power electronic and sensor devices

Characterization

- Electrical characterization of devices (I-V, C-V) up to 500 °C
- Static and dynamic characterization of high-voltage devices
- Parameter analysis of MOSFET devices
- Automatic wafer prober for reliability assessment

Simulation and Modeling

- TCAD modeling of SiC devices
  - Models for channel mobility and avalanche prediction
  - Optimization of cell pitch and junction termination
- Extraction of SPICE models for circuit simulations

2 Top view of a 4H-SiC wafer with various types of electron devices: n- and p-channel MOSFETs, MOS-gated Hall bars, JFETs, PiN diodes, lateral IGBTs, test patterns. Image: Fraunhofer IISB

3 Simulated distribution of electric field in the vicinity of JTE. Image: Fraunhofer IISB