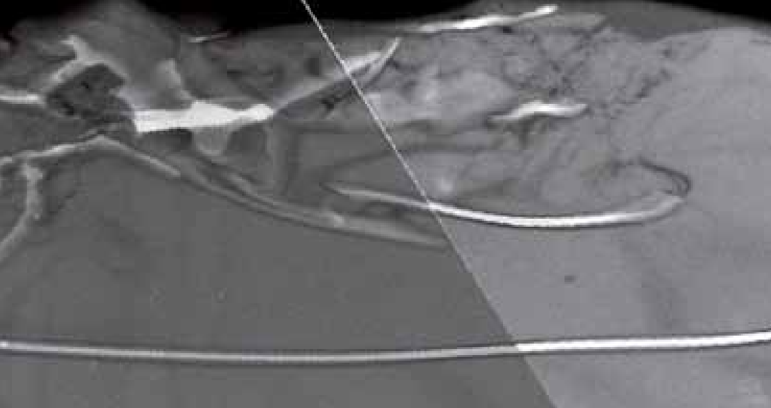

YIELD ENHANCEMENT

Fraunhofer IISB develops defect inspection and flatness metrology solutions for industrial partners. Furthermore, it manages the Yield Enhancement activites of the International Technology Roadmap for Semiconductors (ITRS).

Analytical Equipment

- Defect inspection on non-patterned wafers
- Geometry and flatness measurement
- Atomic force microscope

Methods

- Processing of defect data and defect coordinates
- Robust filtering of surface flatness
- Advanced yield modeling

Applications

- Equipment and process qualification / characterization
- Development of techniques and methods
- Customized developments

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COMPETENCE IN DEFECT DETECTION AND CHARACTERIZATION

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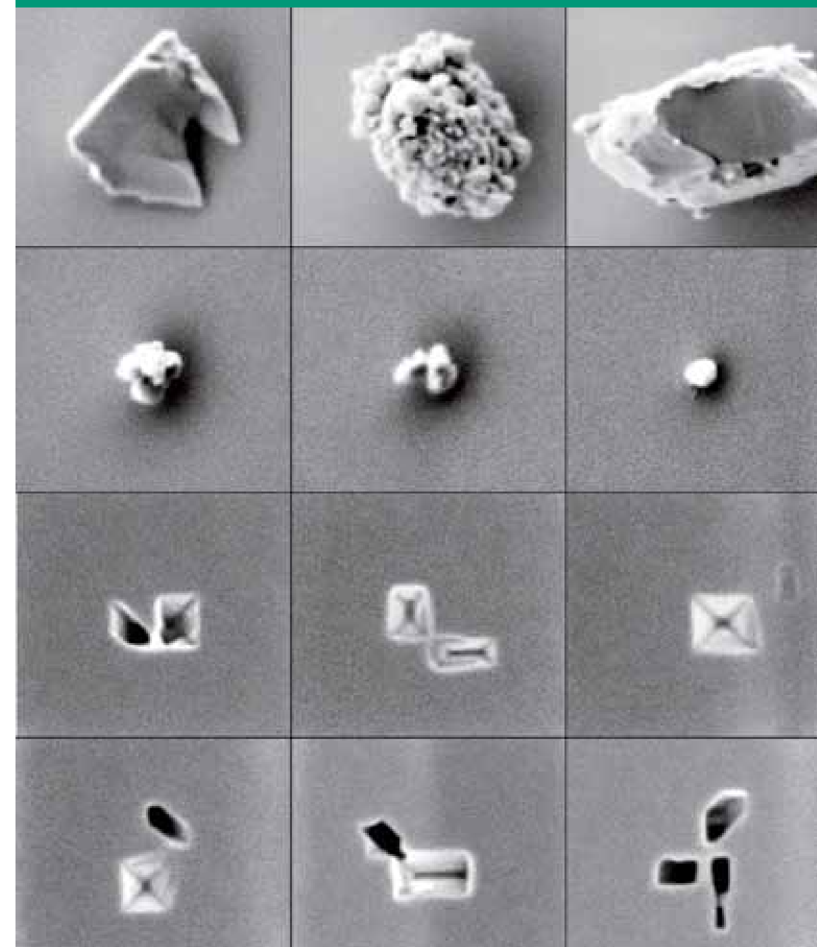
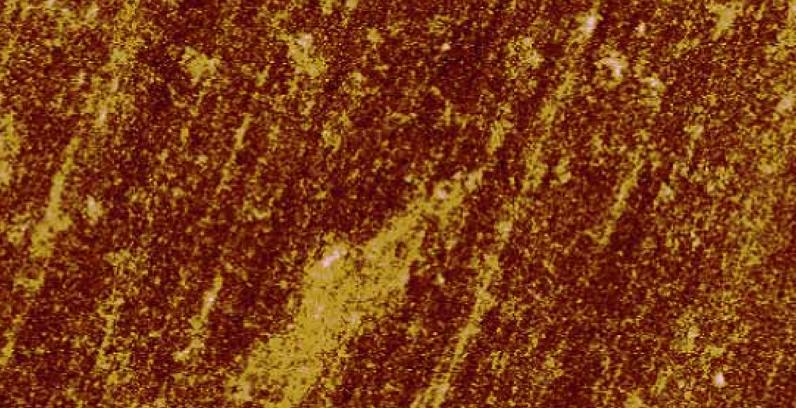
DEFECT CHARACTERIZATION AND YIELD MODELING





DEFECT INSPECTION & REVIEW

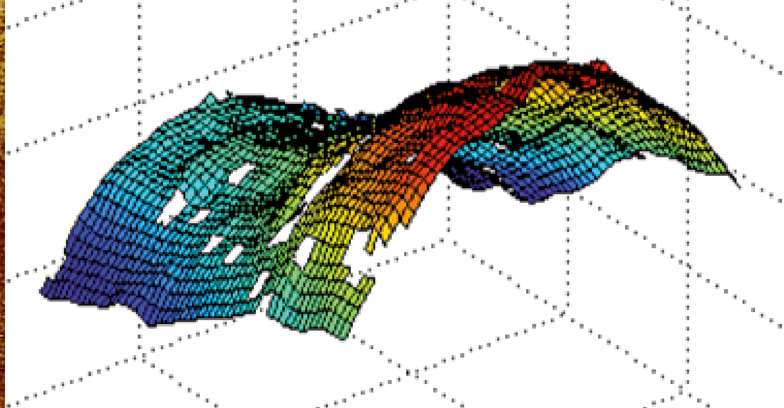
Analytical Techniques

- 200 / 300 mm inspection of non-patterned wafers
- Atomic force microscopy
- Optical microscopy
- Defect types: particle, crystal defects, scratches, roughness

Research

- Characterization and optimization of inspection equipment
- Reliable defect data processing
  - Map comparison
  - Matching and transfer of defect coordinates
  - Determination of particle per wafer pass of semiconductor manufacturing equipment and minienvironments
  - Inspection techniques for 3D integration

REFERENCE MATERIALS SUCH AS BARE TEST WAFERS AND CHARACTERIZED WAFER SAMPLES IN TERMS OF HAZE AND ROUGHNESS



DETERMINATION OF WAFER GEOMETRY

Analytical Techniques

- Global wafer geometry on 200 / 300 mm wafers
- Local topography and flatness determination on mirror-like surfaces
- Determination of wafer edge contour

Development

- Optical techniques, e.g., wave front sensing and long distance microscopy
- Determination of wafer surface topography and wafer edge profiles
- Filtering of surface flatness data
- Defect analysis
- Complementary metrology

CONSTRUCTION OF CUSTOMIZED COMPACT WAVE FRONT SENSORS

$$Y_{line} = \prod_{i=1}^{k}\prod_{j=1}^{n}\left(1+\frac{A\cdot D_{ij}}{\alpha_{ij}}\right)^{-\alpha_{ij}}$$

YIELD MODELING

Engineering

- Development of yield models
- Analysis of semiconductor manufacturing process flow
- Computing of equipment, module, and line yield
- Analysis of critical chip area depending on product and technology

Capabilities

- Use of particle per wafer pass and defect density data of equipment
- Provide yield impact studies of single processing steps, equipments, and defect types
- Study of yield impact of equipment used for different products and technologies

DEVELOPMENT OF CUSTOMIZED ALGORITHMS