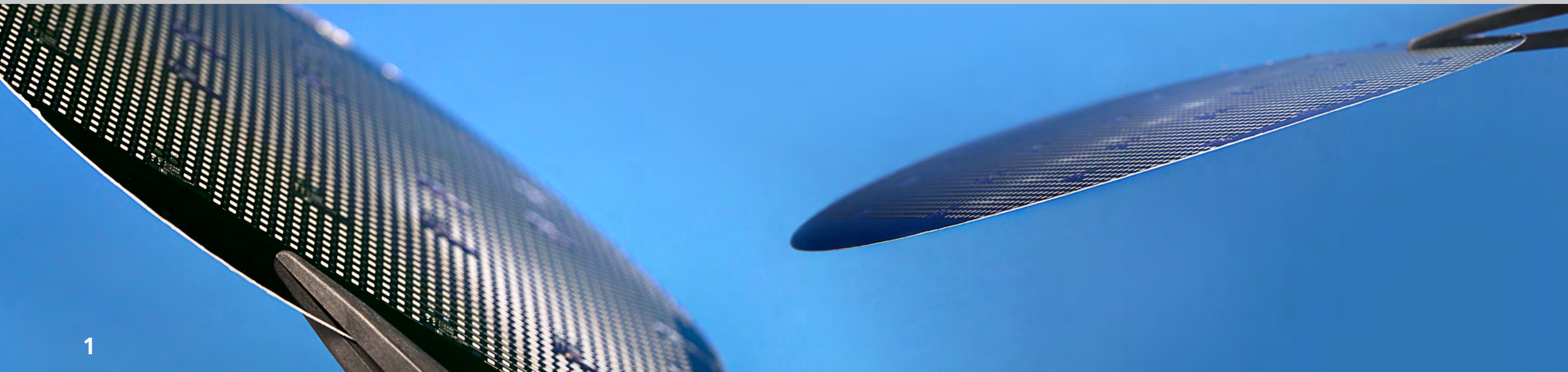
Fraunhofer IISB

FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY



1 *Processed SiC device wafer with 90 µm total thickness.*

BACKEND OF LINE PROCESSING FOR SiC

PROCESS LINE FOR WAFER THINNING AND BACKSIDE CONTACT FORMATION UP TO 150 MM

Benefits of thin-wafer technology

- Minimizing of power losses
- Less deterioration of blocking voltage
- Improvement of thermal connectivity
- Significant increase of power density

Process line

- Bonder for temporary bonding with thermoplastic polymer
- Debonder with thermal slide off
- Grinder and polisher
- Laser annealing tool

Process flow

- Temporary bonding of front-end finished device wafer to carrier wafer
- Backgrinding of device wafer's backside to final thickness
- Deposition of ohmic contact metal
- Formation of ohmic contact by laser annealing
- Deposition of solderable metal stack
- Debonding of temporary bonded device wafer

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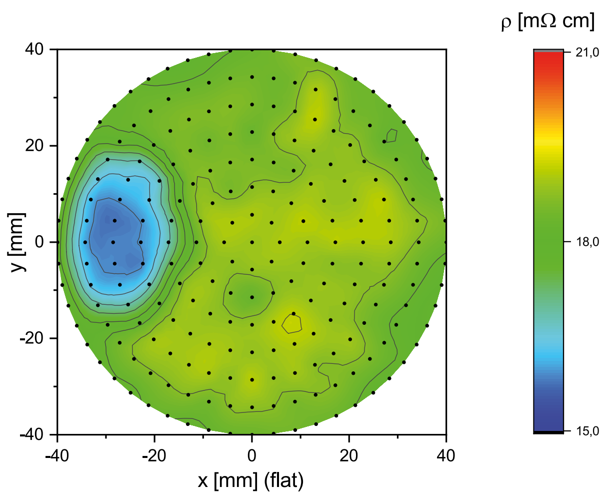
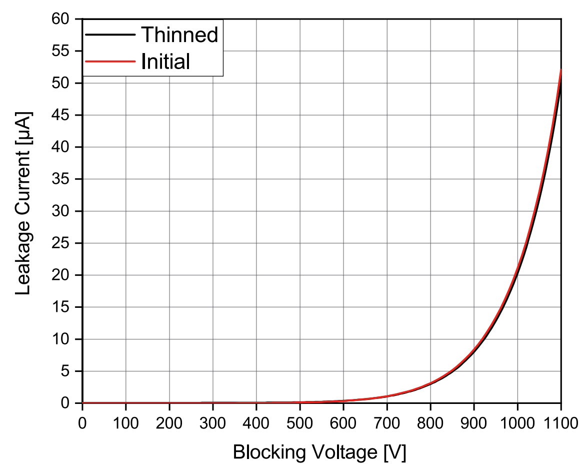
2 *Line for backend of line processing at Fraunhofer IISB. © Kurt Fuchs / Fraunhofer IISB*

Example: 6 A / 650 V SiC JBS diodes

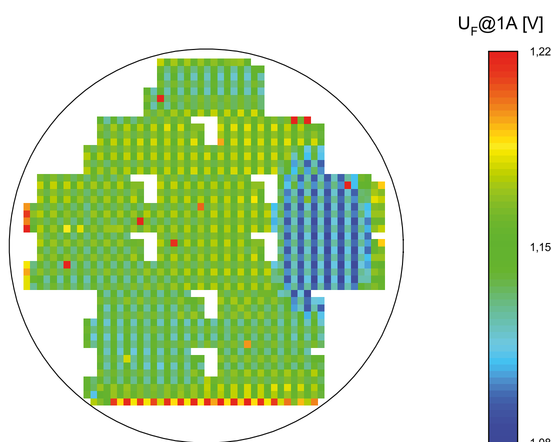
- Total thickness reduction from 370 µm to 90 µm ⟶ Final substrate thickness around 65 µm
- Backside ohmic contact resistance reduction and uniformity improvement by laser annealing
- Electrical parameters like voltage blocking capability of 1.1 kV and leakage current < 1 µA at 650 V not affected by backside processing
- Reduction of ON-state forward voltage drop from 1.78 V to 1.62 V at 6 A
- ON-resistance of 650 V Schottky diodes lowered to 90 mΩ ⟶ Reduction of more than 30 %



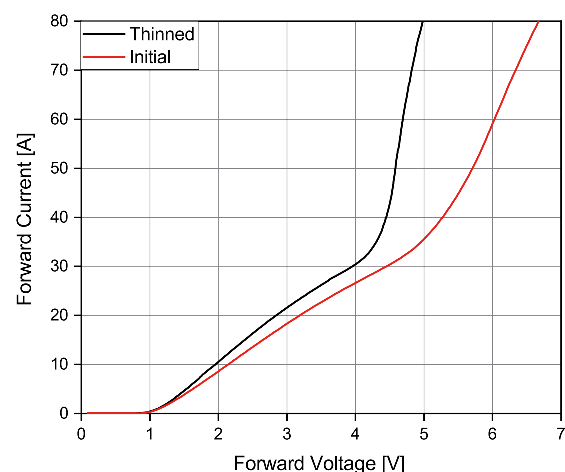
Specific resistance on wafer backside after laser annealing.



Blocking characteristic of 650 V SiC JBS diode initial vs. thinned.



Forward voltages of thinned 650 V SiC JBS diodes at 1 A.



Forward characteristic of 650 V SiC JBS diode initial vs. thinned.