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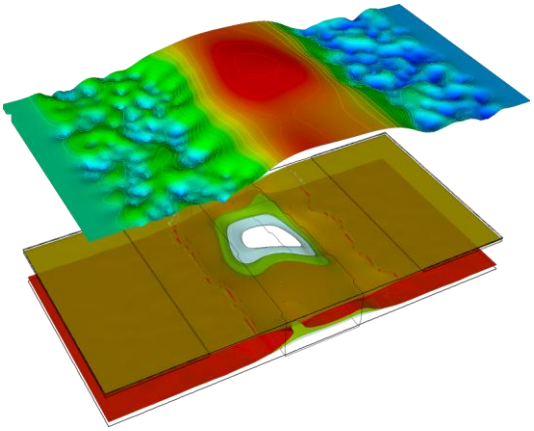
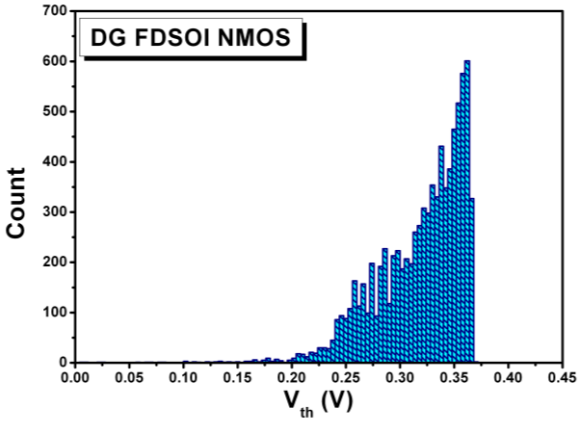
Advanced Simulation Tools to Fight Microchip Variations

European Research Consortium to Develop Simulation Tools Minimizing the Impact of Process Variations on Microelectronic Chips

Process, device, and circuit simulation tools are essential in reducing time to market and the cost of new microchip technology development, delivering faster computers, better consumer products and fueling the digital economy. The International Technology Roadmap for Semiconductors (ITRS) estimates that the use of such tools reduces chip development times and costs by about 40%. Advanced semiconductor devices and circuits are increasingly affected by different kinds of variations which occur during the process of chip fabrication. Within the European project SUPERTHEME, a tool chain for the simulation of the impact of process variations on the devices, circuits and systems fabricated will be developed. This will allow the global semiconductor industry to minimize the detrimental effects of such variations on chips used e.g. in computers, tablets and mobile phones.



3D simulation example of a FDSOI MOSFET transistor subject of random dopants, line edge roughness and metal gate granularity (source: University of Glasgow / GSS)



Simulation example for distribution of switching voltage of an advanced CMOS transistor due to focus variations in optical lithography (source: Fraunhofer)

CMOS process variability includes both systematic variations caused by equipment settings and inhomogeneities which cannot be controlled with sufficient accuracy, and statistical variations which are for instance caused by the discreteness of charge and the granularity of matter in nanometer scale transistors. Effects from various sources of process variations, both systematic and stochastic, influence each other and lead to variations of the electrical, thermal and mechanical behavior of devices, interconnects and circuits. This presents a major challenge for the continued scaling of transistor dimensions and the increase in the complexity and functionality of computer chips which are essential for the economic success of the semiconductor industry. Correlations between different effects of variability are of key

importance because they drastically affect the production yield and the performance of chips and corresponding consumer products. Whereas the comprehensive experimental investigation of these effects is largely impossible, suitable simulation tools offer the possibility to predict the effect of process variations on subsequent process steps and on the behavior of final fabricated devices and circuits. This important application of simulation is among others highlighted in the ITRS.

The SUPERTHEME consortium will address and remove the most problematic weaknesses which limit the use of current simulation software to study the influence of both systematic and stochastic process variability and its interaction with electro-thermo-mechanical effects. Particular emphasis will be put on the study of correlations as their treatment needs to be an essential feature of the simulation system. The project will efficiently combine the use of commercially available software and leading-edge background results of the consortium partners with the research, development and implementation of the key missing elements bridging the current critical gap between variability simulation at the process and device/interconnect level. The capabilities of the software system will be demonstrated both on advanced analog circuits and on aggressively scaled digital CMOS technologies.

To reach these ambitious goals, a consortium of European companies active in complementary fields and leading European research institutes and Universities has been formed, which covers a wide range of expertise from semiconductor equipment and technology to modelling and simulation, and finally industrial exploitation.

On October 2, 2012, the project coordinator, the Fraunhofer IISB in Erlangen, Germany, hosted the kickoff meeting for the 3-year project, which has a total budget of 4.79 million Euros.

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SUPERTHEME

SEVENTH FRAMEWORK PROGRAMME

Project participants:

- Coordinator: Fraunhofer-Gesellschaft zur Förderung der angewandten Forschung e.V. (Germany)
- ams AG (Austria)
- Gold Standard Simulations ltd (United Kingdom)
- University of Glasgow (United Kingdom)
- Technische Universität Wien (Austria)
- ASML Netherlands B.V. (Netherlands)
- Excico France (France)
- HQ-Dielectrics GmbH (Germany)
- IBS (France)

Contact:

Dr. Jürgen Lorenz

Fraunhofer IISB
Schottkystrasse 10, 91058 Erlangen, Germany

Tel. +49-9131-761-210
Fax +49-9131-761-212

juergen.lorenz@iisb.fraunhofer.de

Project web page:

www.supertheme.eu

Fraunhofer IISB:

The Institute for Integrated Systems and Device Technology IISB is one of the 60 institutes of the Fraunhofer-Gesellschaft. It conducts applied research and development in the fields of micro and nanoelectronics, power electronics, and mechatronics. A staff of 170 works in contract research for industry and public authorities.

The institute is internationally acknowledged for the development of technology, equipment, and materials for nanoelectronics and its work on power electronic systems for energy efficiency, hybrid and electric cars.

In addition to its headquarters in Erlangen, the IISB has two branch labs in Nuremberg and Freiberg.

The institute closely cooperates with the Chair of Electron Devices of the Friedrich-Alexander-Universität Erlangen-Nürnberg.