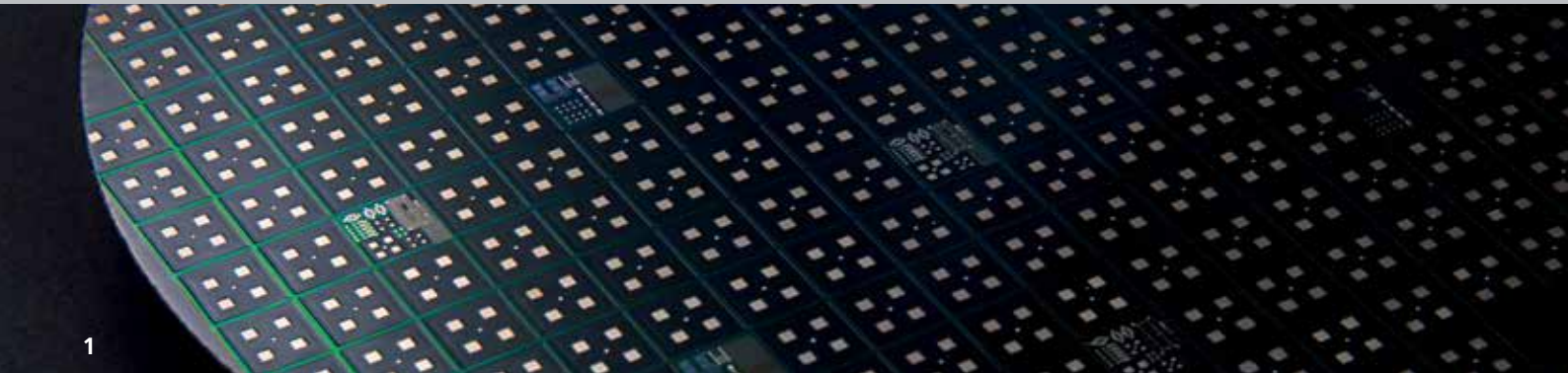




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FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY



1 100mm SiC wafer
with 1.2 kV SiC Power
MOSFETs

1200/3300V SiC POWER MOSFET RELIABILITY AND YIELD

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General Description

SiC Power MOSFET combines the features of nearly ideal switching with superior electrical and thermal properties of wide-bandgap semiconductor materials. High breakdown voltage of the vertical device is supported on a high-quality epitaxial layer, while threshold voltage and electrical current transport are precisely defined by ion implantation. Top and bottom sides of the devices are metalized for assembly in power modules or packages.

Features

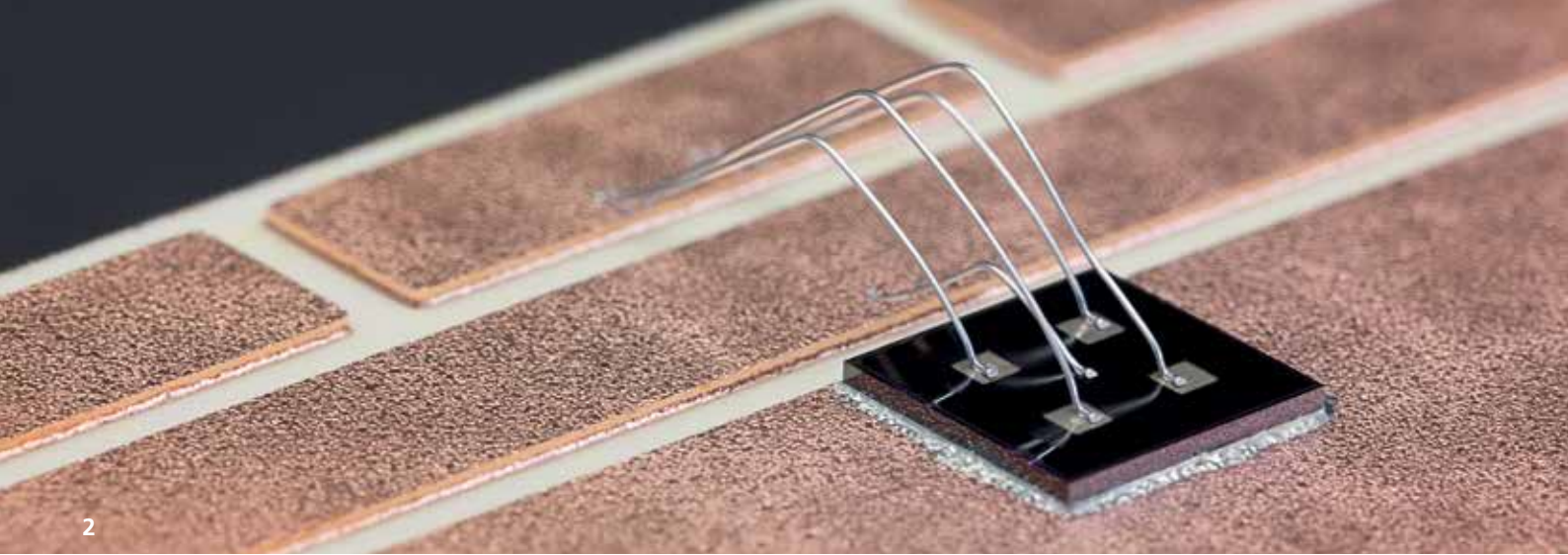
- Wide-bandgap device
- High thermal conductivity and electron drift velocity
- Unipolar current conduction
- Fabrication integrated into existing silicon line
- Available as bar die or in power modules

Advantages

- Decreased on-state resistance compared to silicon device (typ. $R_{DS(on)} < 50 \text{ m}\Omega\text{cm}^2$)
- Stable device operation above 200°C
- Excellent heat transfer between device and package
- Fast switching and low dynamic power losses compared with silicon devices
- Can be used in applications with higher switching frequencies
- Reduced power losses of discrete devices and of full system compared with silicon-based applications

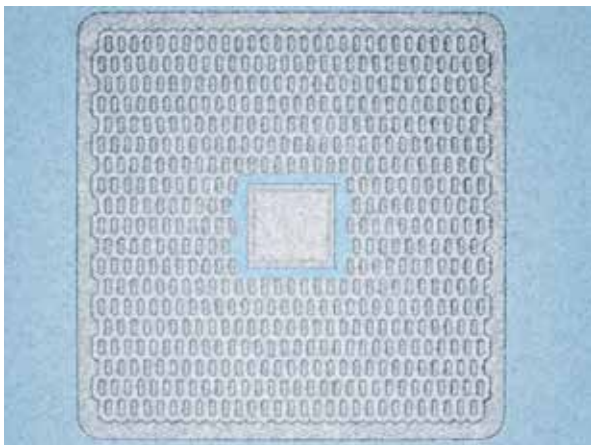
Benefits

- Easier design and cost reduction due to simplified cooling of switching devices
- Decreased weight and volume of passive components and lower total cost of the application using high switching frequencies
- Environment-friendly solution

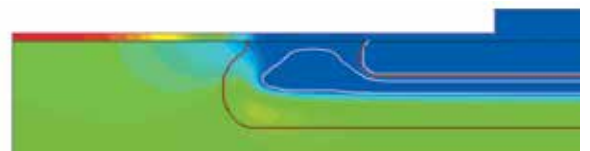


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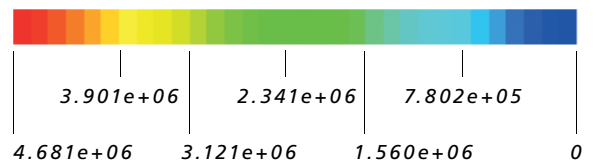
2 Discrete SiC chip mounted on a DCB substrate



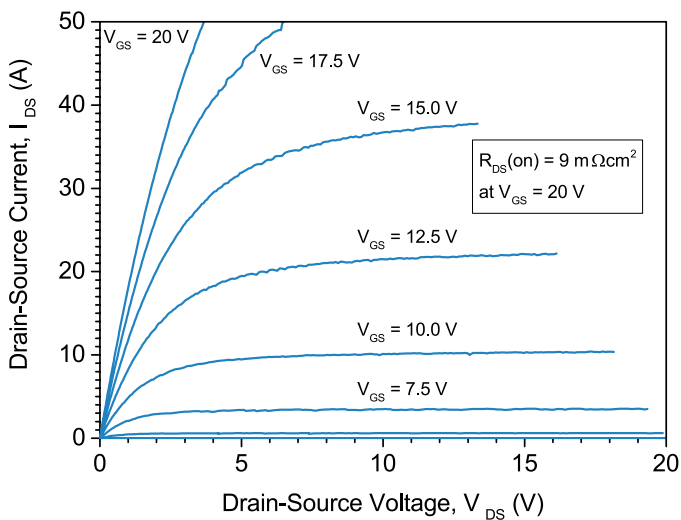
Top view of small SiC Power MOSFET, designed using quasi-hexagonal unit cells.



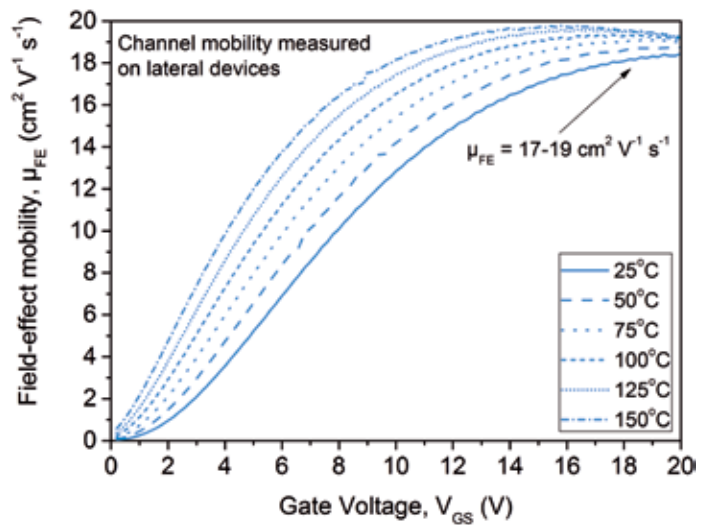
Electric field (V/cm)



TCAD simulation of 1.2 kV SiC Power MOSFET, predicting electric field distribution in the gate oxide.



Example of high current density and low on-state resistance in forward conduction mode.



Example of process technology optimization: oxide and semiconductor/oxide interface optimized for channel mobility and lifetime.