A robust digital PFC control method suitable for low-cost microcontroller

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Abstract
This paper describes the basic principles and experimental results of a digital control method for switching power converter operating in continuous conduction mode (CCM). The method is especially suitable for boost converter in power factor correction applications. In contrast to other well known approaches, the new method requires very low hardware and CPU resources and is thus well suited for low-cost 8 bit microcontroller. With that it becomes realistic that a microcontroller which is already available in most systems today becomes powerful enough to control an active PFC circuit or a switched mode power supply virtually in a sideline.

Keywords: Power factor correction, digital control, current mode, continuous conduction mode

1. Introduction
Due to legal regulations power factor correction (PFC) is necessary in many line-fed applications today. Since considerable additional costs arise from this without a direct customer benefit, equipment manufacturers opposed against these regulations for a long time. Many efforts are also aimed at a cost reduction therefore.

The main lever for PFC cost reduction is a system approach. In the case of an active PFC this means both, to develop all cost reduction potentials in a system which arise from the specific properties of the PFC – e.g. a stabilized d.c. link voltage - as well as to make use of all possibilities for a shared use of system components. Since a microcontroller is available in most applications today, it seems reasonable to examine, whether this couldn't perform the PFC control in a sideline.

Several digital control strategies for a PFC have been published (e.g. [1], [2], [3]). In general the requirements on the microcontroller (µC) performance are quite high and a considerable number of external components like amplifiers, comparators or even PLL circuits is still necessary. Thereby the costs easily exceed the costs for a simple analog PFC control IC. However, there are some very interesting approaches like the method described in [1], which gets by without any kind of current measurement.

We started with some investigations about PFC control strategies which are only based on voltage measurements, but we found them rather problematic since they either required a high computational power or have proved as sensi-

![Fig. 1: Block diagram of the proposed digital current control of a boost converter for PFC](image-url)
tive on line voltage distortions. It was also difficult to parameterize these circuits for a stable operation over the full load range. The necessary line synchronization required either a software filter or an external signal processing for a reliable zero-crossing detection in the case of a noisy line voltage.

In the following, a very simple but nevertheless rugged digital control method for a boost converter in CCM mode for a single-phase power factor correction is described. No special microcontroller or DSP with a high speed, high resolution PWM unit are necessary to generate the clock signal for the boost switch. The new procedure puts minimal demands on µC resources and external circuitry and has been successfully implemented in 8 bit microcontroller of the undermost price range like the ATtiny15L from Atmel or the drive controller SAF C868 from Infineon.

2. Basic function

Fig. 1 shows the block circuit diagram of the proposed digital PFC controller, which is based on a free-running hysteretic current mode control. The only necessary active component in addition to the microcontroller is an inexpensive medium-speed voltage comparator. Two analog inputs of the µC are used to read both, the time dependent input voltage $V_{in}$ and the d.c. link output voltage $V_{out}$. One PWM unit of the µC is used as a slow DA converter which sets the threshold value for the comparator and with that the reference signal for the current controller.

Fig. 2 shows the inner current control loop as it has been realized in the prototyp, fig. 3 illustrates the operation.

When the µC provides a control voltage $V_C$ then the boost switch $T$ is turned-on. The current $I_L$ will increase with a slew rate which is only determined by the actual input voltage and the boost choke inductance $L$ according to

$$\frac{dI_L(t)}{dt} = \frac{V_{in}(t)}{L}$$  \hspace{1cm} (1)

until the turn-off threshold current

$$I_{L,off}(t) = V_C(t) \cdot \frac{R_s}{R_s + R_t}$$  \hspace{1cm} (2)

is reached. During the off-state of $T$ the current $I_L$ decreases according to

$$\frac{dI_L(t)}{dt} = \frac{V_{out}(t) - V_{in}(t)}{L}$$  \hspace{1cm} (3)

until the turn-on threshold $I_{L,on}$ is reached and the next switching cycle starts. The resulting current ripple is given by

$$\Delta I_L = V_{cp,max} \cdot \frac{R_s}{R_s + R_t} \left( 1 + \frac{R_s}{R_t} \right)$$  \hspace{1cm} (4)

with $V_{cp,max}$ as the high-level output voltage of the comparator. Thus by simply adjusting the comparator hysteresis the ripple amplitude of the boost choke current is predefined.
Since the input voltage changes within a line half period, the switching frequency becomes time-dependent. Under the assumption of a bridge rectified ideally sinusoidal input voltage, the frequency characteristics according to eq. (5) is shown in fig. 4. In reality, the switching frequency does not decrease to zero at the line voltage zero-crossings. In this range one has to consider that the approximation which equation (5) is based on, is no longer fulfilled. With the same parameters as used for fig. 4, experimental measurements resulted in a minimum switching frequency of about 30kHz. The dotted line in fig. 4 is valid for a non-negligible signal delay between the shunt resistor and the switching transistor, e.g. due to the delay time of the comparator, the gate driver, etc.

The special course of the switching frequency over a line period, which is a result of the new control method, is especially advantageous for two reasons:

1. The switching losses in the power switch (T) are reduced, because the switching frequency is lowered in a phase with high line voltage and high line current.

2. The EMI level is reduced because of the inherent jitter (modulation) of the switching frequency. This is particularly beneficial for an average noise detection mode. The benefit increases with the order of the switching frequency harmonics.

The control voltage $V_C$ is generated as a direct mirror of the actual line voltage shape. This is done by the microcontroller which reads the input and output voltages via its on-chip AD converter. The input voltage is then multiplied by the output of a PI controller and converted back to an analog signal by means of a PWM modulator connected to a simple RC low-pass filter (s. fig. 5). Input for the PI controller is the deviation between the actual output voltage and the set value. The output voltage of the boost converter is kept constant this way whereas the line current precisely follows the line voltage shape. This results in a pure resistive behaviour at the line connector.

In contrast to some other digital PFC control methods, the control loop operation is not dependent on a precise line synchronization which makes the proposed solution quite insensitive to line noise.

**3. Practical implementation**

The experimental investigations have been carried out using a low-cost 500W drive inverter board with active power factor correction (s. fig. 6). The on-board processor was a SAF C868 from Infineon whose main task was the V/f control of an induction motor. The processor was operated at an internal clock frequency of 37.5MHz.

The basic drive software has been extended by an interrupt controlled PFC routine. Two free AD
channels were used to read the input and output voltage with a resolution of 8/10 bit at a sampling rate per channel of 5000 values/sec. The PFC routine was written in C, with a code length of about 300 bytes and an execution time below 70µsec. To synthesize the analog output voltage necessary for the current control loop, we took a free internal 16 bit PWM counter together with an external RC low-pass filter. The corner frequency of this filter was 3.5kHz. An actual PWM resolution of 9 bit has proved as absolutely sufficient.

As an additional protection function, a software shutdown has been implemented which stops any pulses whenever the output voltage exceeds a certain threshold value - in our case 400V. Together with a restart hysteresis this provides a very stable behaviour under no-load conditions and soft motor braking. Restart is always done via a softstart.

The CPU load due to the PFC related tasks was about 30%. With critical tasks written in assembler instead of C, we expect a CPU load below 20%. Only 6 Byte RAM for data storage have been necessary, a great advantage in comparison to many other PFC control strategies which require large pre-calculated tables, e.g. for the sine function. The inherent line synchronization saves external circuitry or a software solution for zero-crossing detection.

For reasons of cost reduction, it is essential to make use of the reduced ripple current load for the d.c. link capacitor, which results from the active PFC. When the d.c. link capacitor is chosen with respect to the ripple current rating, this results in quite small capacitance values in the range of 0.5µF per watt output power or lower and a correspondingly high d.c. link voltage ripple. In order to avoid the well-known detrimental effect of the second harmonic ripple voltage across the output capacitance when this ripple is introduced into the multiplier of the voltage control loop, we used a software sample and hold method ([3], [4]). This is simply realized by refreshing the input variable of the voltage control loop (\( V_{\text{out,act}} \)) only as long as the input voltage (\( V_{\text{in}} \)) is below a small threshold value. The output voltage is sampled near the line zero-crossings this way and held constantly during the rest of the line half-period.

The test board was based on a Tyco V23990-P372-01-PM power module which integrates all power semiconductors like the input bridge rectifier, the boost switch and boost diode, the three phase IGBT bridge as well as the necessary shunt resistor (s. \( R_{\text{s}} \) in fig. 2). The d.c. link capacitor was a 220µF/450V aluminium electrolytic capacitor.

4. Measurements

Fig. 7 shows measured line voltage and current waveforms, fig. 8 the line current harmonics spectrum in front of the limits which are defined in the standard EN 61000-3-2. Both measurements were taken with the test board directly fed from the laboratory mains. The line voltage waveform shows the soft-clipped sine shape which is typical for the line voltage in large office buildings.

![Fig. 7: Measured line voltage and current waveforms with the PFC directly fed from laboratory mains \((V_{\text{in}}=230V, V_{\text{out}}=380V, P_{\text{out}}=480W)\).](image)

![Fig. 8: Spectrum of line current harmonics for two different loads.](image)

Since the presented control method provides a resistive behaviour at the line terminals, any distortion of the line voltage is reflected in the line current too. This however doesn’t mean any restriction with respect to practical applications,
since the compliance of the limits is always checked with an ideal sinusoidal line voltage waveform.

As one can see from fig. 8, the line current distortions remain far below the limits. It seems realistic therefore that the sampling rate for the input and output voltage and with that the number of calls of the PFC routine can be considerably reduced below the actual value of 5000/sec. This would further decrease the CPU load.

A stable behavior of the PFC circuit at load variations is essential. Fig. 9 shows the d.c. link voltage regulation in the case of a load step from half load to nearly full load.

The most critical situation for PFC circuits is generally a sudden load release from full load to no-load. As one can see from fig. 10, this situation is handled without any problem by the proposed controller. The d.c. link voltage remains far below the critical value of 450V (i.e. the voltage limit of d.c. link capacitor) under all operating conditions including line overvoltage.

5. Conclusions

With the proposed control method it is possible to realize a full active PFC functionality with inexpensive 8 bit microcontrollers. The CPU load could be reduced to values below 30% so that modern 8 bit controller can perform the task in a sideline. The PFC properties with respect to line current harmonic distortions and dynamic control loop response are absolutely sufficient for the target applications in the consumer and mass markets.

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7. References


