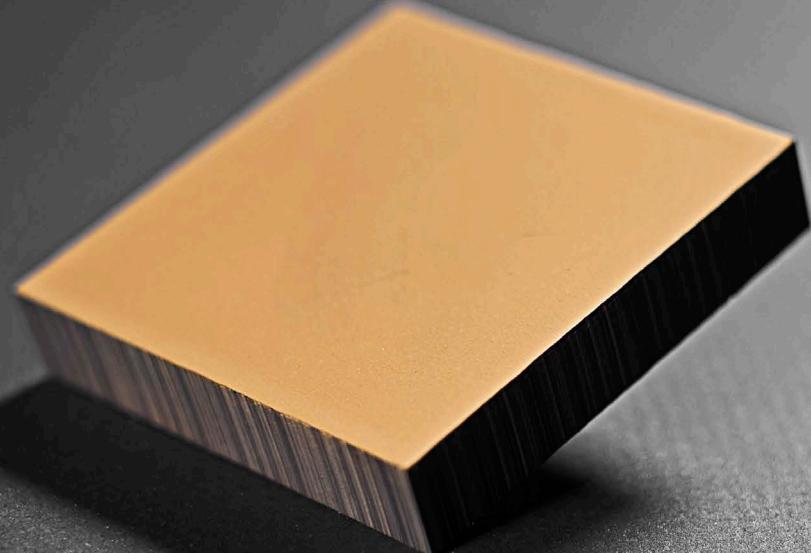


2025

HIGH TEMPERATURE  
AND CORROSION RESISTANT COATING

TACOTA®



NIPPON  
KORNMEYER



Fraunhofer  
IISB

TACCOLA®

EFFICIENT PROTECTION OF GRAPHITE PARTS USED IN  
SEMICONDUCTOR PRODUCTION & PROCESSING



# HIGH TEMPERATURE AND CORROSION RESISTANT COATING

Nippon Kornmeyer Carbon Group GmbH and Fraunhofer IISB present their innovative and patented **tantalum carbide coating technology TACCOTA®**.

The high temperature and corrosion resistant coating can be applied to graphite substrates and used in semiconductor material production and processing. It secures graphite parts from decomposition and corrosion in typical high temperature and reactive gas processes like SiC and nitride PVT crystal growth and epitaxy, ion implantation, and plasma processing. The benefit is an increased lifetime and improved cost of ownership.

## R&D BY FRAUNHOFER IISB:

- Delivery of test parts and application demonstrators
- Application testing support
- Custom tailored coating developments and short feedback loops
- R&D project collaboration

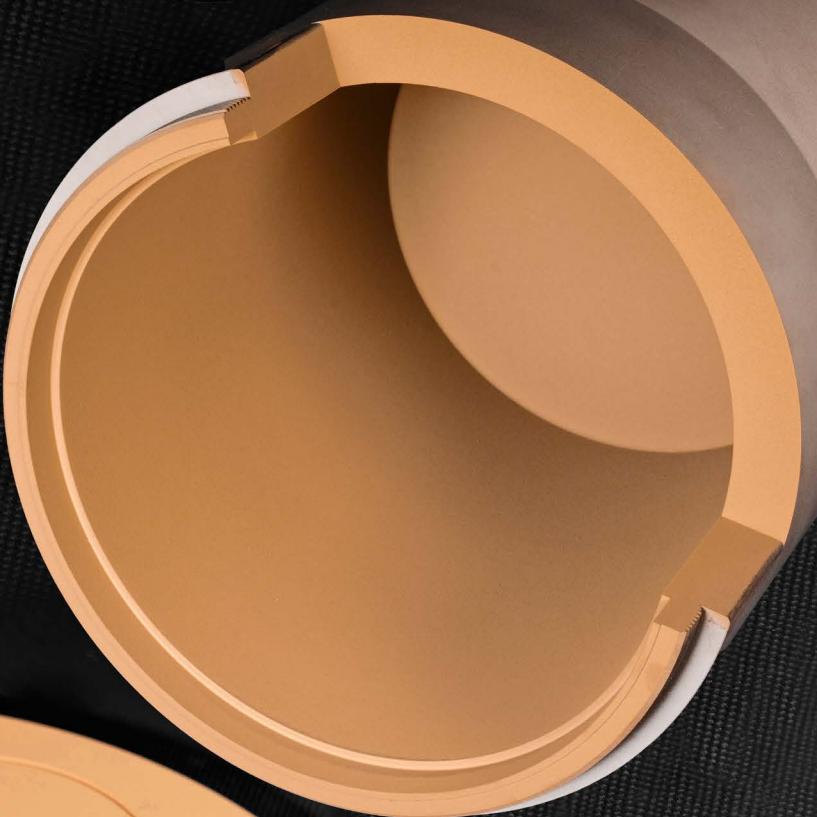
## PARTS SUPPLY BY NIPPON KORNMEYER CARBON GROUP GMBH:

- From small batches to relevant production quantities

**TACCOTA®**  
STABILIZES PROCESS  
CONDITIONS IN SiC  
PVT GROWTH AND  
PROTECTS PARTS IN  
SiC EPITAXY REACTORS



300 mm  
DIAMETER  
PLANETARY EPI-DISC



250 mm  
DIAMETER  
PVT CRUCIBLE

# ADVANCED COATING TECHNOLOGY

## TECHNOLOGY BENEFITS

- Flexible for part size and geometry
- Partial and all around coating possible
- Part refurbishment
- Resource efficient and environmentally friendly
- Use of conflict-free materials only
- Industry ready

## COATING FEATURES

- High temperature resistance (up to 3000°C)
- Resistance against corrosive gases and fluids, molten metals and salts
- Excellent wear resistance and good adhesion to the graphite substrate
- Thickness between 20-300 µm adjustable
- Surface roughness  $R_a$  of about 1-2 µm independent of coating thickness
- Adjustable from porous to dense layers with different permeabilities
- Variable coating composition (mixtures with other UHTC materials)

# TACCOTA® FLEXIBLE COATING PROPERTIES

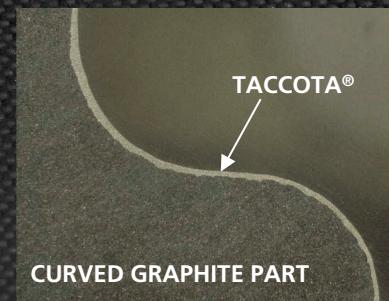
The process technology allows the adjustment of the desired coating properties such as thickness ...



TYPICAL PART COATING THICKNESS UP TO 150 μm

INCREASING COATING THICKNESS UP TO 300 μm POSSIBLE

NO THICKNESS LOSS AT WELL-DEFINED GEOMETRY



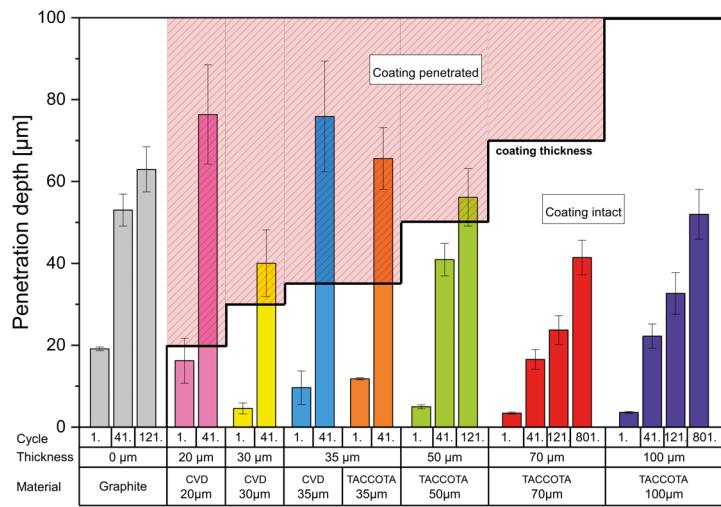
... and composition (i.e. blend with other high temperature ceramic materials)



UNDER DEVELOPMENT!

## TACCOTA® MECHANICAL STABILITY

- At least 8 MPa bonding strength to substrate according to pull off test after DIN EN ISO 4624:2014-06
- Low penetration depth according to scratch test after DIN 50324 / ASTM G99 and G133):



ENHANCED WEAR  
RESISTANCE DUE  
TO INCREASED  
COATING THICKNESS



## TACCOTA® READY FOR HIGH TEMPERATURE APPLICATION

- Resistivity of 2.3  $\mu\Omega\text{cm}$  (four point measurement @ RT) certifies a good electrical conductivity
- Thermal conductivity of 27-32 W/m\*K measured from 1500°C to 2000°C
- Emissivity of 0.55-0.6 measured from 1500°C to 2000°C @ 1 µm wavelength (infrared range)

# TACCOTA® LOW-CONTAMINATION WAFER CARRIERS

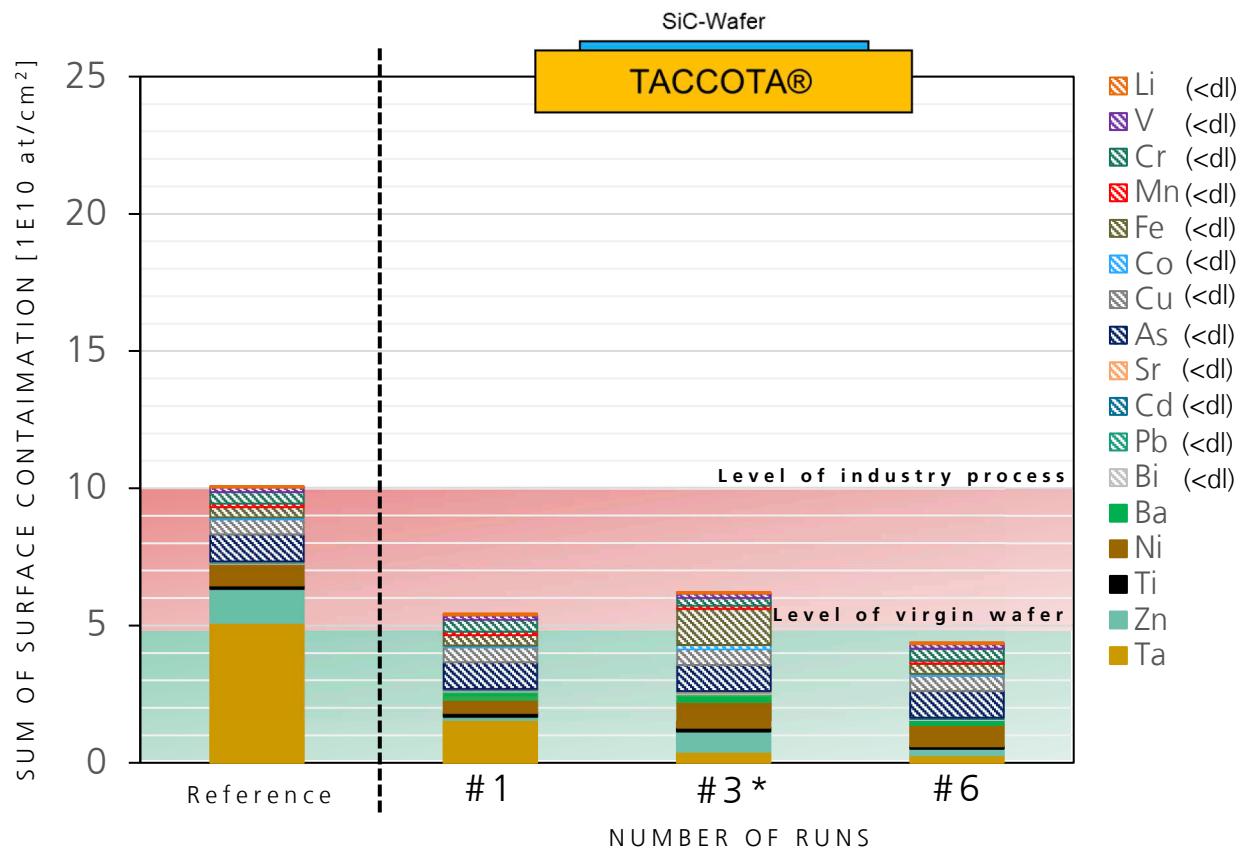
- THE INTRODUCTION OF A NEW TACCOTA® WAFER CARRIER DOES NOT LEAD TO ADDITIONAL TANTALUM CONTAMINATION OF THE SiC WAFER TOP SURFACE
- EVEN THE LOWER SiC WAFER SURFACE WHICH IS IN DIRECT CONTACT TO TACCOTA® SHOWS NO SIGNIFICANT CONTAMINATION (RUN #3)
- MINIMUM OF 9 RUNS WITHOUT ANY DAMAGE OF THE CARRIER AND COATING DEMONSTRATED



TACCOTA® WAFER CARRIER BEFORE SiC EPITAXY RUN

## TACCOTA® COATING PERFORMANCE UNDER SiC EPITAXY CONDITIONS

ADDING A NEW TACCOTA® WAFER CARRIER TO A REFERENCE SETUP  
(CONTAMINATION LEVEL COMPARABLE TO INDUSTRY PROCESSES):

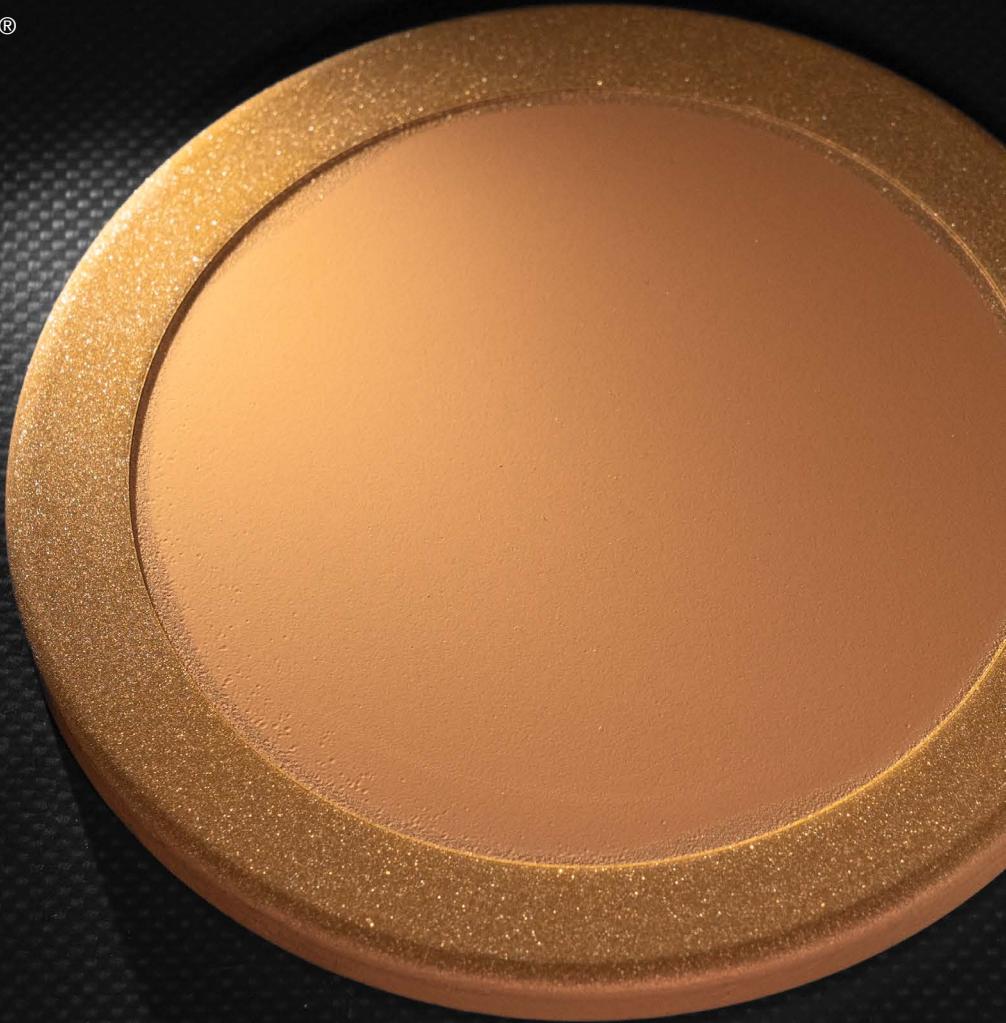


Surface contamination was measured by VPD ICP-MS on Si-side of epi-ready Ø100 mm SiC-wafers. For each run, a virgin cleaned SiC-wafer was used with Si-side on top. <dl means below detection limit.

\*In run #3, the SiC-wafer was intentionally flipped with Si-side in direct contact to TACCOTA® wafer carrier.

# TACCOTA® LOW-CONTAMINATION WAFER CARRIERS

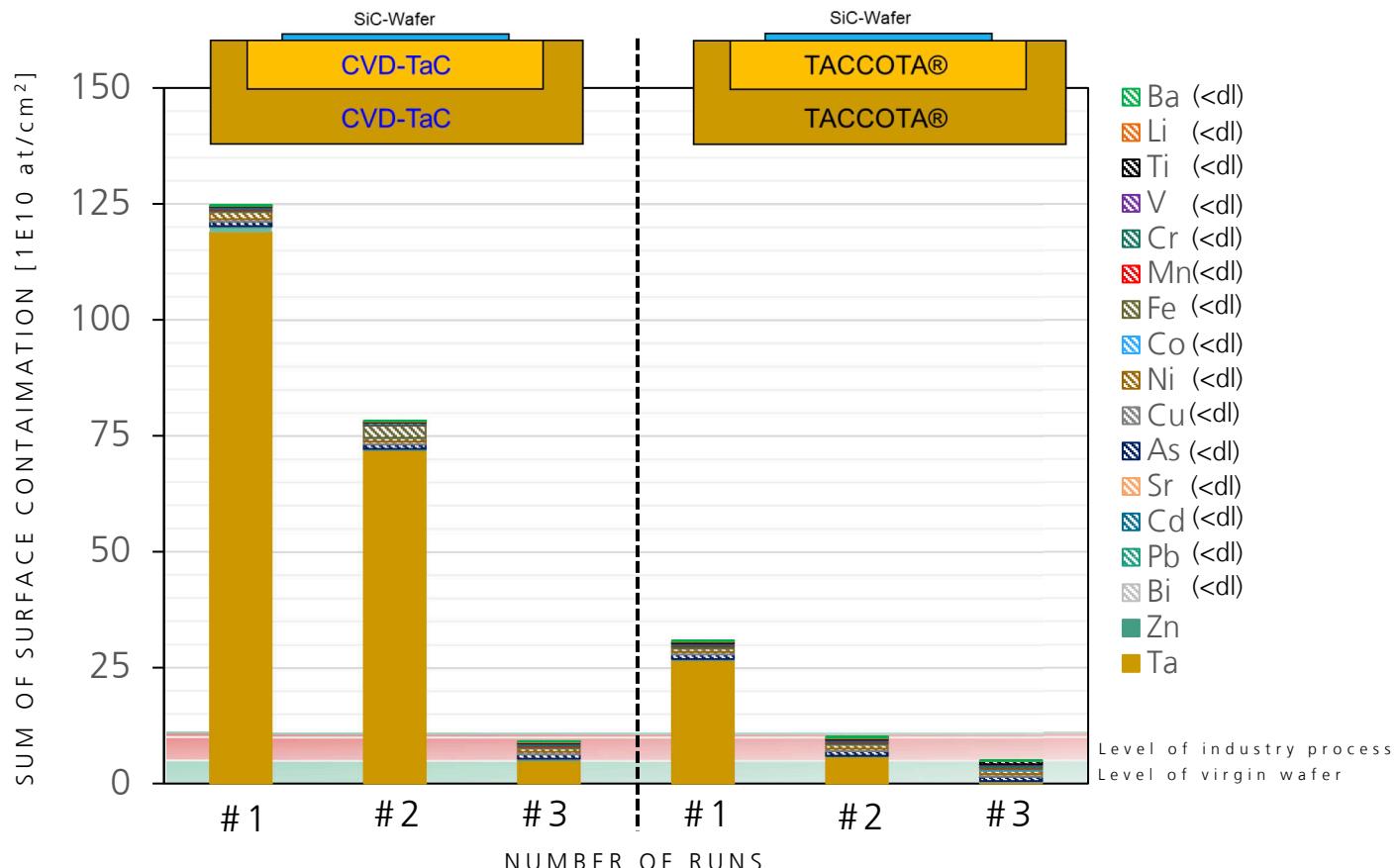
- BY THE USE OF TACCOTA® SUSCEPTOR & WAFER CARRIER, THE INITIAL TANTALUM SURFACE CONTAMINATION ON THE SiC WAFER TOP SURFACE CAN BE REDUCED BY 75 %.
- THE NUMBER OF FIRST EPI RUNS AFTER WHICH THE TANTALUM CONTAMINATION REACHES A NON-CRITICAL LEVEL CAN BE REDUCED.



TACCOTA® WAFER CARRIER AFTER 6 SiC EPITAXY RUNS

# TACCOTA® COATING PERFORMANCE UNDER SiC EPITAXY CONDITIONS

CHANGE COMPLETE SETUP (SUSCEPTOR AND CARRIER) FROM  
CVD-TaC TO TACCOTA®:



Surface contamination was measured by VPD ICP-MS on Si-side of epi-ready Ø100 mm SiC-wafers. For each run, a virgin cleaned SiC-wafer was used with Si-side on top. <dl means below detection limit.

**Fraunhofer Institute for Integrated Systems and Device Technology IISB**

Schottkystraße 10  
91058 Erlangen  
Germany

**Contact:**

Dr.-Ing. Matthias Trempa  
Group Manager Crystallization and Coating Technologies  
Phone +49 9131761268  
[matthias.trempa@iisb.fraunhofer.de](mailto:matthias.trempa@iisb.fraunhofer.de)

**[www.iisb.fraunhofer.de](http://www.iisb.fraunhofer.de)**

**Nippon Kornmeyer Carbon Group GmbH**

Im Nassen 3  
53578 Windhagen  
Germany

**Contact:**

Dirk Muetzenich  
Global Product Management & Sales  
Phone +49 16096073490  
[dirk.muetzenich@carbongroup.de](mailto:dirk.muetzenich@carbongroup.de)

**[www.nk-carbon.com](http://www.nk-carbon.com)**

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