The Effect of Etching and Deposition Processes on the Width of Spacers Created during Self-Aligned Double Patterning

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Abstract

Topography process simulation has been used to study the interaction of etching and deposition processes for spacer creation for self-aligned double patterning (SADP). For the deposition process, the influence of the layer conformality was investigated. For the etching process, the directionality of the ion flux was varied. The simulations show that by an appropriate combination of the deposition and etching processes, spacers can be created with the desired critical dimension (CD) and a small deviation between the inner and outer spacer CD values. In addition to using the simulation flow for tuning the processes, it can be employed to investigate the influence of variations. As an example, we studied the effect of the across-wafer non-uniformity of the thickness of the deposited oxide layer. For the process sequence considered, the relative change of the spacer CD is 4 to 5 times larger than the relative change of the oxide thickness.

Introduction

The basic principle of SADP is shown in **Figure 1**. The positions of the spacers have to follow the layout for instance of the SRAM cell. In this study, we keep the lithography process fixed and vary the etching and deposition processes, in order to study the impact of the variations on the resulting CD values of the spacers.

Influence of the Etching and Deposition Processes

For the deposition process we considered a non-conformal process (such as used for instance in [1]) as well as a conformal one (for instance using TEOS). For modeling of the non-conformal deposition we assumed a typical low-temperature oxide chemical vapor deposition (CVD) process which can be simulated using a sticking coefficient of 0.5 as parameter for the physical deposition simulator DEP3D [2]. The dry-etching process has been modeled with the etching simulator ANETCH [3] assuming that the etching of the oxide is governed by the ion flux, where the angular distribution of the ions is given as a Gaussian distribution with varying σ.

Figures 2 and 3 shows simulation results for both types of deposition processes and for three different values of σ corresponding to a varying directionality of the ion flux. An overview of the resulting spacer CD values is given in **Table 1**. Choosing an appropriate combination of deposition (conformal vs. non-conformal) and etching (directionality of the ion flux which can be adjusted for instance by changing the substrate bias or the pressure in the etching reactor) allows one to reduce the difference ΔCD between the CD values of the inner and outer spacers.

Influence of Variations

As an example for demonstrating the effect of a varying deposition rate (e.g., across the wafer), we consider a variation of the oxide thickness (defined as thickness in planar regions of the topography) deposited in the CVD process. The other quantities of the simulation flow (σ for the etching process, sticking coefficient for the deposition process) are kept constant. The simulations considered before (**Figures 2 and 3**, **Table 1**) are based on an oxide thickness of 20 nm. **Table 2** shows the CD values of the spacers obtained for varying thickness of the oxide. For both 5 % and 10 % reduction of the oxide layer thickness, the relative change of the spacer CD is about 4 to 5 times larger than the relative change of the oxide thickness. The spacer geometries for the 10 % thickness reduction (oxide thickness = 18 nm) are shown in **Figure 4**.

Conclusions

By means of topography process simulation, we have demonstrated the interaction of etching and deposition processes for spacer creation for SADP. In addition to employing the simulation flow for tuning the processes, we can use it for investigating the influence of variations. As an example, we studied the influence of the across-wafer non-uniformity of the thickness of the oxide deposited by CVD. For the process sequence studied in our examples, the relative change of the spacer CD is 4 to 5 times larger than the relative change of the oxide thickness.

References

[1] H. Zang, Y. Wang, F. Xiao, ECS Transactions **69** (2015) p. 215
[2] E. Bär, J. Lorenz, IEEE Trans. Semicond. Manufact. **9** (1996) p. 67
[3] E. Baer, D. Kunder, P. Evanschitzky, J. Lorenz, Proceedings SISPAD 2010, p. 57

Acknowledgment

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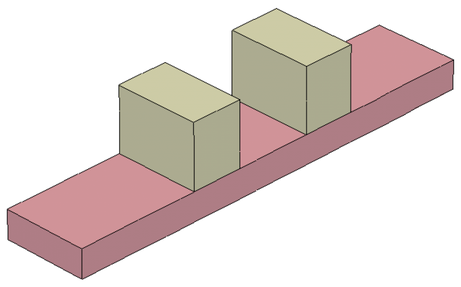
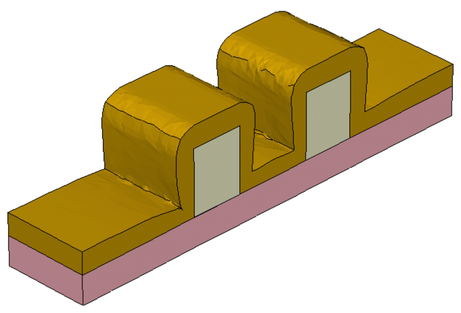
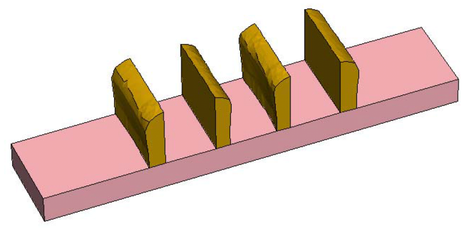


(a)

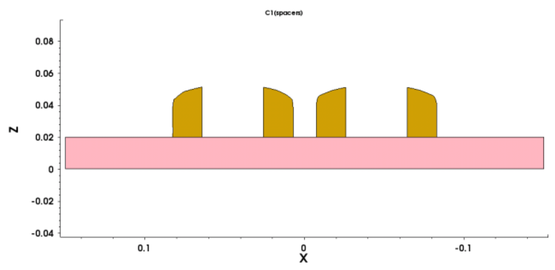


(b)

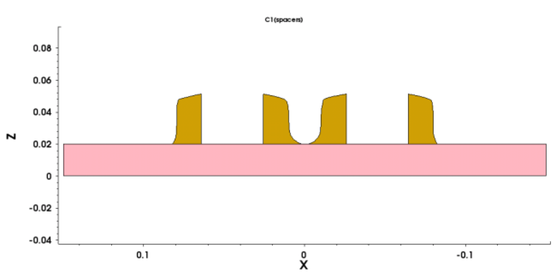


(c)

Figure 1: Sequence for creating the SADP spacers. (a): Carbon lines as patterned by the lithography step. (b): Deposition of an oxide layer. (c): Back etching to create the spacers.

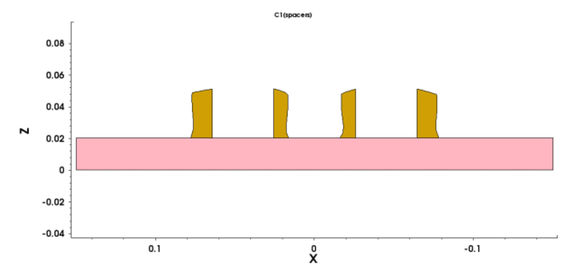


(a)

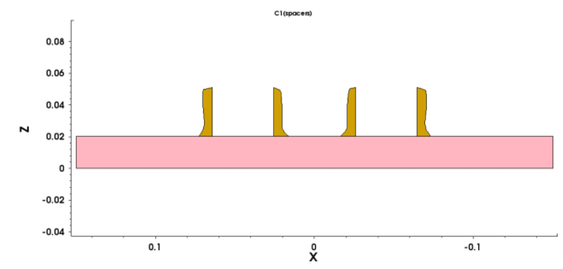


(b)

Figure 2: Spacer geometries for a conformal deposition process and an etching process with varying σ of the angular flux distribution of the ions (a: σ=0.05, b: σ=0.3, c: σ=0.8).



(a)



(c)

Figure 3: Spacer geometries for an LTO deposition process and an etching process with varying σ of the angular flux distribution of the ions (a: σ=0.05, b: σ=0.3, c: σ=0.8).

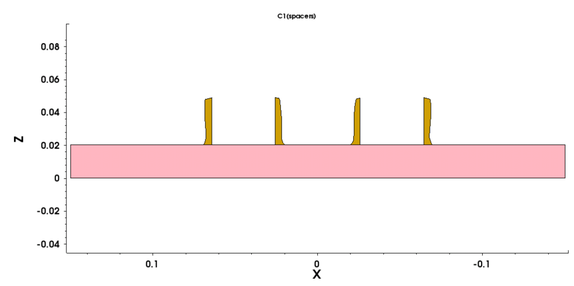


Figure 4: Spacer geometry for an LTO deposition process and an etching process with σ=0.8 where the thickness of the layer deposited by CVD is reduced by 10 % compared to the process for which the result is shown in Figure 3 (c).

Table 1: CD values (nm) for inner spacers/outer spacers for different deposition and etching processes.

	σ = 0.05	**σ = 0.1**	**σ = 0.3**	**σ = 0.8**
Conformal deposition	18.5 / 18.5	18.5 / 18.5	24 / 18	fail / 14.5
LTO deposition	12 / 16	12 / 16	10 / 14	10 / 9

Table 2: CD values (nm) for inner spacers/outer spacers for different thicknesses of the LTO layer used for spacer creation.

	d = 20 nm σ = 0.8	**d = 19 nm σ = 0.8**	**d = 18 nm σ = 0.8**
LTO deposition with thickness d	10 / 9	7.5 / 7	6 / 5

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