Project no. 027152

ATOMICS

Advanced Front-End Technology Modeling for Ultimate Integrated Circuits

Public Final Report

The ATOMICS Consortium

Version of October 12, 2009

1 Introduction

Technology-computer-aided design (TCAD) is an indispensable tool for development and optimization of new generations of electronic devices in industrial environments. It was estimated in the 2007 International Technology Roadmap for Semiconductors that TCAD reduces technology development costs by 40%. However, to continue to be that useful for the 32 nm technology node and beyond, the capabilities of TCAD have to follow the paradigm shifts to processes and materials considered for such nanodevices.

The objective of ATOMICS is to extend the capabilities of TCAD to the materials and doping processes used at the 32 nm node and beyond. In particular, quantitative models for the deactivation and activation mechanisms for dopants in silicon were developed which are suited for the low ion implantation energies and low-temperature or millisecond-annealing strategies of future nanodevices. These models are able to predict the effects of point-defect engineering and, for boron, the influence of fluorine. For strained and unstrained silicon-germanium alloys, strained silicon, and silicon-on-insulator materials, models were developed for the evolution of extended defects and for the activation, segregation, and diffusion of dopants. Special test structures were also used to investigate a possible diffusion anisotropy in isolated semiconductor layers. The models developed were implemented and integrated into Sentaurus Process to be of immediate value to the semiconductor industry and validated with respect to their needs.

To reach these ambitious goals, the consortium consists of companies active in complementary fields of competence (STM-France: device manufacturing, Mattson: equipment production, Synopsys: TCAD software, CSMA: characterization) in addition to three leading European research institutes (Fraunhofer-IISB, Univ. Newcastle, CNRS-LAAS/CEMES) with extensive experience in modeling and simulation.

In the following parts of this document, some of the findings are highlighted in dedicated contributions. For further information on the topics, please contact the person indicated at its end.

2 Electrical characterization of ultra-shallow junctions

Continuous scaling of semiconductor devices towards smaller dimensions drives the need to characterize the positions of electrical and chemical junctions with nanometer accuracy, as well as to measure detailed concentration profiles and electrical activation levels.

Advanced doping and annealing scenarios result in activated dopant profiles which lead to inconsistent results if standard four point probe characterization is done. Therefore different methods to characterize sheet doping and doping profiles on shallow implanted as well as deposited p- and n-type junctions are compared. In general these experiments are done on unstrained silicon substrates but measurements on strained silicon and SiGe wafers are also included. Spike and flash annealed wafers were characterized. The sheet doping characterization is done with standard four-point-probe sheet resistance measurement where probes with different probe weight, to vary the penetration depth of the measurement, are used. The results of these measurements are then compared to Hall-effect measurements. For chemical depth profiling secondary ion mass spectrometry (SIMS) is used and compared to spreading resistance profiling and differential Hall-effect measurements.

As a result a consistent measurement protocol for the full suite of silicon-based materials investigated in the ATOMICS project, involving a standard “golden tool” reference method and a reliable routine method is developed.

2.1 State of the art

In semiconductor fabrication sheet resistance measurement with four-point-probe (FPP) is a standard measurement for characterizing the sheet electrical activity of blanket-implanted dopants. For the very thin layers, defined by the probe tip penetration and probe tip spacing, the resulting voltage to current ratio can be converted to the sheet. The method was originally developed for deep junctions, for which the measurements correspond very well to other methods. Since sub-keV junctions were introduced, with shallow, highly doped layers, this approach has become less reliable and reproducible, owing to contact and puncture issues. If the penetration depth of the tips is close to or deeper than the junction depth, this may lead to parallel leakage currents through the deeper layers (see also Figure 1). In practice it can be expected, that deeper penetration leads to lower R_S values and increased variance in measurement values.

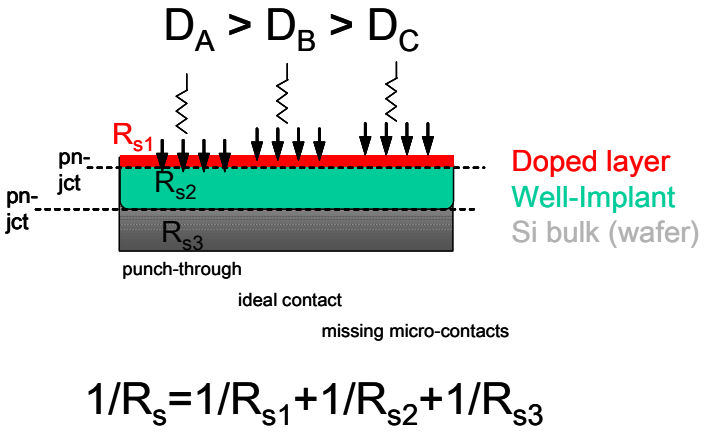

Figure 1: Schematic of sheet resistance (R_S) calculation and the influence of different probe weights with varying penetration depth D

It has been reported before [1] that the spring load of the FPP tip influences the penetration depth of the tip. Clarysse et al. used three different probes with different nominal tip radius from different metrology tools (two four-point-probes and one spreading resistance probe) with spring loads of 5 g, 60 g and 100 g.

2.2 Experimental Details

State of the art implanted wafers

For these experiments, n-type (6-24 Ωcm resistivity) and p-type (10-20 Ωcm resistivity), 200 mm prime Si wafers of (100) orientation were used with a well implantation of $^{11}B^+$ 20 keV to a dose of 5×10^{12} cm^{-2} for n-type wafers and $^{75}As^+$ 130 keV to a dose of 5×10^{12} cm^{-2} with 7° tilt for the p-type substrate wafers. The well implants were subsequently annealed in a Mattson 2800 RTP system at IHP at 1030 °C for 10 s in an ambient of 10% O_2 in N_2.

The different state of the art ultra shallow implantation conditions in this study were $^{11}B^+$ 500 eV, $^{49}BF_2^+$ 1.1 keV, $^{75}As^+$ (500 eV and 1 keV) implanted into crystalline silicon. For all implants the dose was up to 1×10^{15} cm^{-2}. All the implants were performed on an Applied Materials Quantum batch implanter under 0° tilt and 0° twist conditions.

The spike anneal was performed in a Mattson 3000 Plus RTP system equipped with Mattson's absolute temperature measurement, a temperature controller optimized for spike anneals, and wafer rotation. The ramp-up rate to the pre-stabilization step was 50 K/s. The recipe included pre-stabilization at 650 °C for 10 s followed by a spike with a ramp-up rate set to 250 K/s. The peak temperature of the spike anneal was 1000 °C. The anneals of $^{11}B^+$ and $^{49}BF_2^+$ implanted wafers were done in a 100 ppm oxygen in nitrogen ambient at atmospheric pressure and the $^{75}As^+$ implants were annealed in an ambient of 10% oxygen in nitrogen [2]. The flash anneal was carried out in a Mattson Millios fRTP™ in a nitrogen ambient. From an intermediate temperature of 750 °C the wafer was flashed to a peak temperature of 1300 °C [3].

The sheet resistance was measured by a KLA-Tencor RS-100 four point probe using five different type D probes (with a tip radius of 0.508 mm) with a circular 121 site pattern and 3 mm edge exclusion. The probes consisted of a standard KLA Tencor Type D with 100 g probe load, and four different D-type Jandel probes with 10 g, 30 g, 60 g and 100 g probe load.

Epi-layers with box-like profile

Because of their flexibility to produce junctions with defined depths, epi layers were used. Therefore 200 mm prime Si wafers of (100) orientation n-type (6-24 Ωcm resistivity) and p-type (10-20 Ωcm resistivity), were cleaned in SC1 and SC2 received a well implantation with $^{11}B^{+}$ 20 keV with a dose of 5×10^{12} cm^{-2} in case of n-type substrate wafers and the p-type substrate wafers were implanted with $^{75}As^{+}$ 130 keV and a dose of 5×10^{12} cm^{-2} with 7° tilt. The well implants were subsequently annealed in a Mattson 2800 RTP system at IHP at 1030 °C for 10 s in an ambient of 10% O_2 in N_2.

The boron and arsenic epi-deposition processes were carried out in an ASM Epsilon 2000 reduced pressure, single wafer CVD tool. The epi-growth was performed at 700 °C at a pressure of 80 Torr with H_2 as carrier gas. For p-doping a mixture of SiH_4 and B_2H_6 and for n-doping SiH_4 and AsH_3 was used. Prior to the epi-growth a pre-bake at 1000 °C, 30 s in H_2 ambient at 80 Torr was run.

The spike and flash anneals were performed in the same way as described above.

Sheet resistance measurements were done in the same way than for the characterization of the implanted layers.

The As profiles were measured using a Cameca IMS 7F using Cs primary ions at 50 degrees and at an energy of 900 eV. The B measurements were also done on the same instrument using 500 eV O_2 primary ions under non-roughening conditions. The implant dose was determined by the Relative Sensitivity Factors (RSF) derived from the ion implanted reference samples, calibrated against NIST (National Institute of Standards, US) standards or Rutherford Backscattering Spectrometry (RBS). The depth calibrations were carried out using either a calibrated Dektak or a Tencor profilometer. Repeatability is typically within 1% for both, junction depth and dose.

Several samples were measured with a CAPRES microRSP-M150 with a microscopic four-point probe. The electrode pitch of the four-point probe is three orders of magnitude smaller than conventional four-point probes. The contact force is 1,000,000 times smaller than that of a macroscopic 4PP which ensures non-destructive probing [4].

On a few samples spreading resistance profiling (SRP) measurements were done by SSM on a SSM 2000 system. SRP technology provides a direct measurement of the resistivity and carrier density profiles of electrically active dopants. The SSM 2000 features a dynamic range in carrier density measurements from $<10^{11}$ cm^{-3} to the dopant solid solubility limit, and a spatial resolution in depth profiling on the order of 1 nm.

Selected samples were also measured by Hall-effect which provides additional information on the electrically active dose, N_S, and the carrier mobility, μ. In the absence of advanced techniques to measure other important activation parameters, an empirical method for the self-consistent interpretation of SIMS and Hall-effect measurements of ultra-shallow junctions was used, that allows to estimate most of those critical activation parameters. In particular, by this method it is possible ***(i)*** to determine the activation level of the doped layer (maximum active dopant concentration, activated dose fraction) and, for the case of partially activated structures, ***(ii)*** to assess whether or not the carrier mobility is affected by electrically inactive clustered dopants.

Hall measurements were carried out by CNRS/LAAS on an Accent HL5500 Hall-effect system and based on the Van der Pauw technique (VDP) on Greek-cross structures. Measurements were performed at both, room temperature and liquid nitrogen temperature.

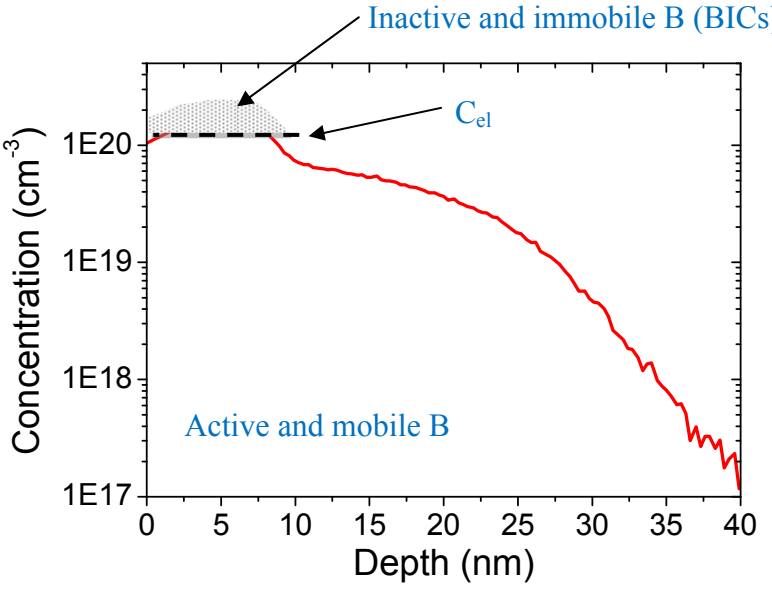

Figure 2: SIMS profile of 10 nm boron doped epitaxial layer submitted to a 1050 °C spike annealin. This profile exhibits a static peak, a "kink" at a B concentration of about 7×10^{19} cm^{-3} (C_{el}), and, below this concentration level, a diffused tail. C_{el} indicates the concentration level above which B forms immobile and electrically inactive boron interstitial clusters (BICs). Below this concentration, all dopants are assumed to be mobile and electrically active.

As it was mentioned before, for this work we do not dispose of measured carrier depth profiles, as SIMS measurements provide information on the total chemical dopant distribution that includes both the electrically active and inactive fractions. However, the typical features of SIMS profiles measured from ultra-shallow doped layers, allow to establish an approximate relation between the chemical and the electrically active dopant profiles.

Figure 2 shows a boron SIMS profile of the 10 nm boron doped epitaxial layer submitted to a 1050 °C spike annealing. Similarly to the typical ion-implanted boron-doped junctions, this profile exhibits a static peak, a "kink" at a B concentration of about 7×10^{19} cm^{-3}, and, below this concentration level, a diffused tail. The kink indicates the concentration level above which B forms immobile boron interstitial clusters (BICs) which are commonly assumed to be electrically inactive. Below this concentration, previous SRP studies indicate that, if the annealing occurs at sufficiently high temperatures (>1000 °C), the totality of the dopant distribution is electrically active.

Based on these features, we therefore define, from the chemical dopant profile measured by SIMS, $C(x)$, the active dopant concentration profile, $C_a(x)$, as follows:

for $C(x) \geq C_{el}$, $C_a(x)=C_{el}$

for $C(x) < C_{el}$, $C_a(x)=C(x)$

where C_{el} is the maximum active dopant concentration, which may or may not coincide with the concentration corresponding to the observed "kink".

In addition, we will also assume that the active dopant concentration profile, $C_a(x)$, is identical to the carrier concentration profile, $p(x)$ (in the case of B), that is to say that the carrier spilling effect is negligible. Indeed, a difference between $C_a(x)$ and $p(x)$ is expected to arise only at low concentration levels, however this difference would have a very small impact on the calculated values of R_S, $\langle N_S \rangle$ and $\langle \mu_C \rangle$.

Finally, we make the assumption that, in the presence of an immobile and electrically inactive peak, i.e. in the presence of BICs the carrier drift mobility μ_p may be reduced. This translates the hypothesis that the presence of such defects can introduce an additional scattering mechanism that affects carrier mobility. We therefore define an effective drift mobility, μ_{eff}:

$\mu_{eff} = \alpha \cdot \mu_p$, with $\alpha \leq 1$

For a totally activated junction (i.e. without BICs), we will have $\alpha=1$, while in the presence of a high concentration of BICs, we expect to find, for α, a value lower than unity.

It has to be noted at this point, that, in principle, the Hall scattering factor (HSF), *r*, could also be modified in the presence of inactive dopant clusters. As a first approximation the proposed protocol will assume that the HSF, estimated from fully activated reference samples, is constant for all the investigated structures.

According to all previous assumptions it finally can be written:

$$R_s = \frac{1}{q\int_0^t C_a(x)\mu_{eff}(x)dx} \qquad \langle N_S \rangle = \frac{(\int_0^t C_a(x)\mu_{eff}(x)dx)^2}{\int_0^t C_a(x)\mu_{eff}^2(x)dx} \qquad \langle \mu_C \rangle = \frac{\int_0^t C_a(x)\mu_{eff}^2(x)dx}{\int_0^t C_a(x)\mu_{eff}(x)dx} \qquad \textbf{(1), (2), (3)}$$

Then, from the SIMS profiles of the investigated samples and the theoretical values of drift mobility against carrier concentration [5], the sheet resistance R_S, active dose N_S and mobility μ_C can be calculated and matched to the measured values using 2 fitting parameters ($\boldsymbol{C_{el}}$ and $\boldsymbol{\alpha}$).

Advanced layers (strained silicon, strained SiGe and relaxed SiGe)

CNRS/LAAS provided us with 12 samples with different relaxed SiGe layers with approximately 2 µm thickness. Two different types of background doping with phosphorous were used for bulk wafers as well as for SiGe wafers with different Ge concentrations, ranging from 20% to 50%. The second implant was $^{11}B^+$, 15 keV with a dose of either 10^{14} cm^{-2} or 3×10^{15} cm^{-2}.

The sheet resistance was measured by a KLA-Tencor RS-100 four point probe using five different type D probes (with a tip radius of 0.508 mm). The 2×2 cm² samples were measured with a 4×4 pattern. The probes consisted of a standard KLA Tencor Type D with 100 g probe load, and four different D-type Jandel probes with 10 g, 30 g, 60 g and 100 g probe load. Additionally, van der Pauw sheet resistance measurements were done at CNRS/LAAS as already described above. Further sheet resistance measurements were also done at CNRS/LAAS on a CMT-SR200N 4PP tool with a Jandel probe on 10 sites.

Another set of wafers was prepared by IHP (Frankfurt/Oder) with strained silicon, strained SiGe as well as relaxed SiGe layers. 2×2 cm^2 samples were processed in a 200 mm recessed wafer in a Mattson 3000 Plus RTP system. The anneals were done in a wide range of temperatures and times ranging from 700 °C to 1000 °C from spike anneals to 1000 s soak anneals: These anneals were performed in an ambient of 100 % N_2.

The sheet resistance was measured by a KLA-Tencor RS-100 four point probe with a KLA Tencor type D probe (with a tip radius of 0.508 mm). The 2×2 cm^2 samples were measured with a 4×4 pattern. Van der Pauw measurements were done at University of Newcastle using a cloverleaf sample geometry. In this case the sample centre is under test while each of the four leaves acts as an edge contact to the central region. The leaves can be made relatively large in order that a metal alloy can be applied for ohmic contact formation with the probes. Photolithography and etching is used to desirably modify the structure of a 1 cm^2 sample surface and form a cloverleaf shape. Samples are then glued to the dedicated sample holder using black wax. Metallic contacts are created on each of the four cloverleaves by painting on a liquid gallium/indium eutectic. The very light, non-penetrating probes of the Accent

HL5500 Hall kit are then placed onto the eutectic using tweezers. In addition to making van der Pauw resistance measurements, Hall measurements can be made on cloverleaf samples to determine the carrier type, carrier density and, in combination with the resistance measurement, carrier mobility. The cloverleaf is also a desirable geometry when performing Hall-effect measurements on the same samples. In this study, all van der Pauw resistance and Hall measurements were performed on an Accent HL5500 Hall kit. When determining sheet resistance, multiple measurements are performed for all permutations of pairs of contacts, using both forward and reverse currents. The average of the eight values is used as the most accurate value of sheet resistance.

2.3 Results

State of the art implanted wafers

The first step in this task was to evaluate state of the art ultra shallow implanted wafers. Half of the wafers received a p^+/p respectively n^+/n well implant prior to shallow junction implantation. The wafers were annealed with a spike and flash anneal. Four-point-probe measurements were done on these wafers to measure sheet resistance.

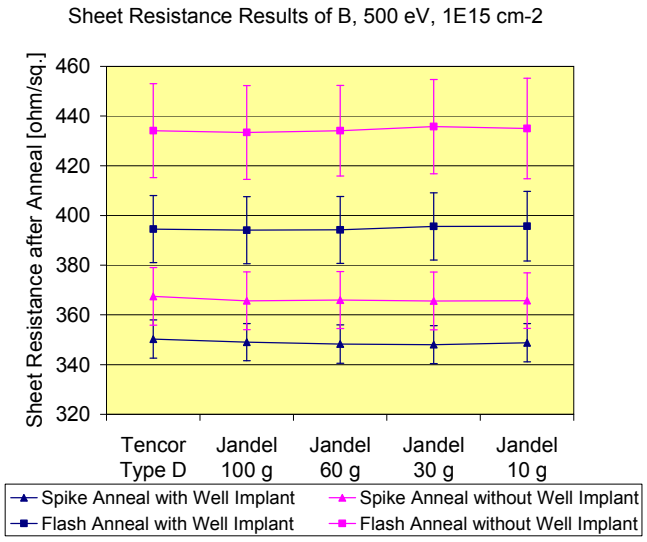

Figure 3: Sheet resistance results of B, 500 eV, 1×10^{15} cm^{-2}

The sheet resistance measurement results for Tencor D, Jandel 100 g, 60 g, 30 g and 10 g are visualised in Figure 3 for $^{11}B^+$ 500 eV. Detailed results for $^{75}As^+$ 1 keV, of $^{49}BF_2^+$ 1.1 keV and of $^{75}As^+$ 500 eV are not shown here.

In general spike or flash annealed standard $^{11}B^+$, $^{49}BF_2^+$ and $^{75}As^+$ shallow implants can be measured with 4PP with weights from 100 g down to 30 g without any measurement issues. Also fewer measurement errors are obtained with the use of a deep p^+p respectively n^+n implantation (well implant). In general the sheet resistance with well implant is lower than without owing to the additionally doped layer (cf. sheet resistance calculation of several layers with parallel circuit in Figure 1). The spike annealed arsenic implants could not be measured with a 10 g probe due to the oxide layer formed during annealing in an ambient with 10% O_2 in N_2. Several publications during previous years [6] and [7] show good agreement (below 10% standard deviation) of Hall-effect measurements and sheet resistance on implanted wafers.

Epi-wafers with box-like profiles

Sheet resistance measurements on B- and As-epitaxial layers with the different probes show that reliable measurements of shallow B-epi layers down to 35 nm (nominal layer thickness 25 nm) are possible with all probe loads (see e.g. Figure 4 and Figure 5). Shallower layers should be measured with a probe load smaller than 60 g. For As-epi layers reliable measurements are possible down to 30 nm layer thickness (nominal 10 nm) with probe loads from 100 g down to 30 g. Only shallower layers should be measured with the 60 g or 30 g probe load.

From the theoretical sheet resistance calculations much lower sheet resistance values were expected with the assumption that all dopants in the grown layer are electrically active.

SIMS measurements on the as-deposited B- (Figure 6 and Figure 7) and As-epitaxial layers showed that the layers are not always matching the requested target thickness. A comparison of the as-grown, spike and flash annealed SIMS profiles for B-epi layers are given in Figure 8 and Figure 9 for 5, 10 and 25 nm nominal epi-layer thickness. For As-epi layers the SIMS profiles are not shown here. In collaboration with CAPRES some wafers were measured for their sheet resistance using a micro-4PP tool (μRSP).

The 25 nm B- and As-epi layers with well implant were measured with SRP by SSM. SSM used two different methods, the standard and a surface corrected, for carrier concentration calculation. The results of these two different methods are quite contradictory as it can be seen in

Table **1**. For example the spike annealed B-epi layer shows an electrically active dose of 108% (calculated with the surface corrected profile) whereas the as-deposited wafer has 35% electrically active dose. Also the As-epi layer results are unusual, the as-deposited wafer has a sheet resistance of 649 Ω/sq. with 30% electrically active dose whereas the spike annealed wafer has a lower sheet resistance of 602 Ω/sq. but according to SRP results only 26% of the dopants are electrically active. These discrepancies show that although not particularly shallow profiles were investigated with SRP the results are extremely difficult to interpret. In Figure 10 a comparison of electrical carrier concentration determined with SRP to chemical concentration measured by SIMS for B-epi layers with nominally 25 nm with well implant for as-deposited and 1050 °C spike annealed wafers is shown.

A comparison of 4PP, μRSP and Hall-effect measurements for B-epi with 10 nm nominal layer thickness without well implant is graphically shown in Figure 11. The as-deposited wafer with a junction depth of 12 nm (determined by SIMS at a concentration of 1×10^{18} cm^{-3}) has a relatively high sheet resistance in the order of 4000 Ω/sq. going along with a high range in sheet resistance of the different methods, especially μRSP and Hall-effect show much higher sheet resistance values than conventional 4PP measurements. The flash and also the spike annealed wafers show sheet resistance deviations below 10%.

For the nominal 25 nm B-epi layers (with well) only the Hall-effect result of the flash annealed wafer is out of 10% range. The results of all the other measurement methods for as-grown, spike and flash annealed wafers are within 10% range (see Figure 12). Striking is also the high error bar for the spike annealed wafer measured with Jandel 10 g probe weight which is due to some measurement issues owing to a thin oxide layer formed during the spike anneal which can not be penetrated sufficiently by the probe.

In general we see good agreement between 4PP and μRSP measurement results and the μRSP measurements usually show a slightly higher sheet resistance value than the other methods. A more detailed analysis of the Hall measurements indicates that the as-deposited layer is not fully electrically active and that a partial (or total) dopant reactivation probably occurs during annealing. The spike annealing leads instead to an almost complete activation of the deposited layer. However, improved SIMS profiles for these samples would be necessary to confirm such conclusions.

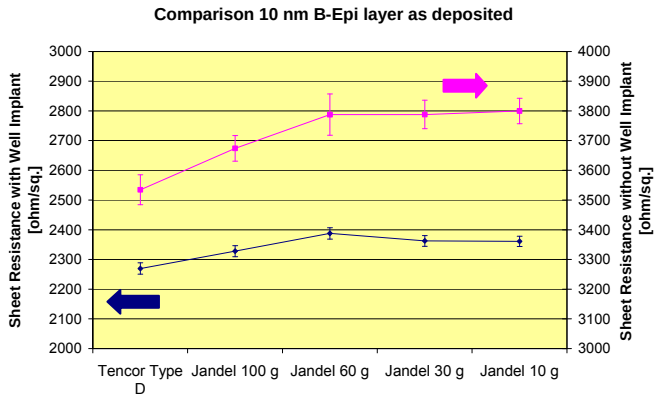

Figure 4: Sheet resistance results of 10 nm B-Epi layer as deposited

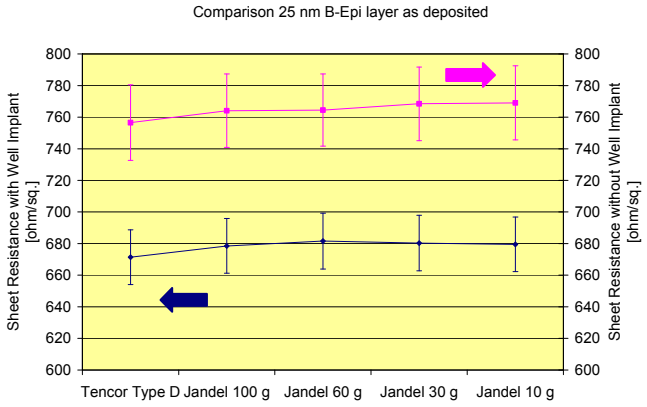

Figure 5: Sheet resistance results of 25 nm B-Epi layer as deposited

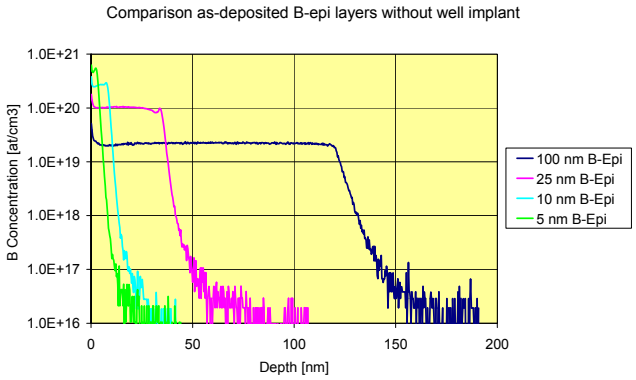

Figure 6: SIMS profiles of as-deposited B-epi layers without well implant

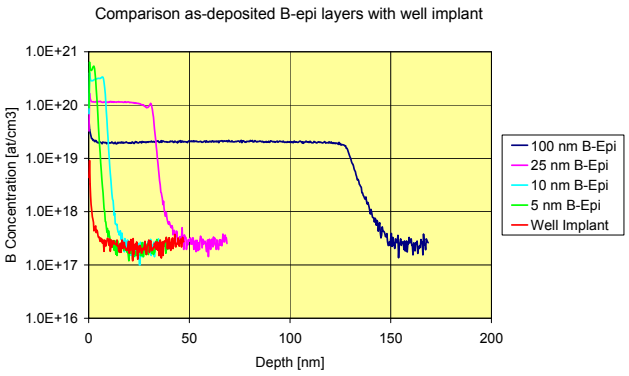

Figure 7: SIMS profiles of as-deposited B-epi layers with well implant

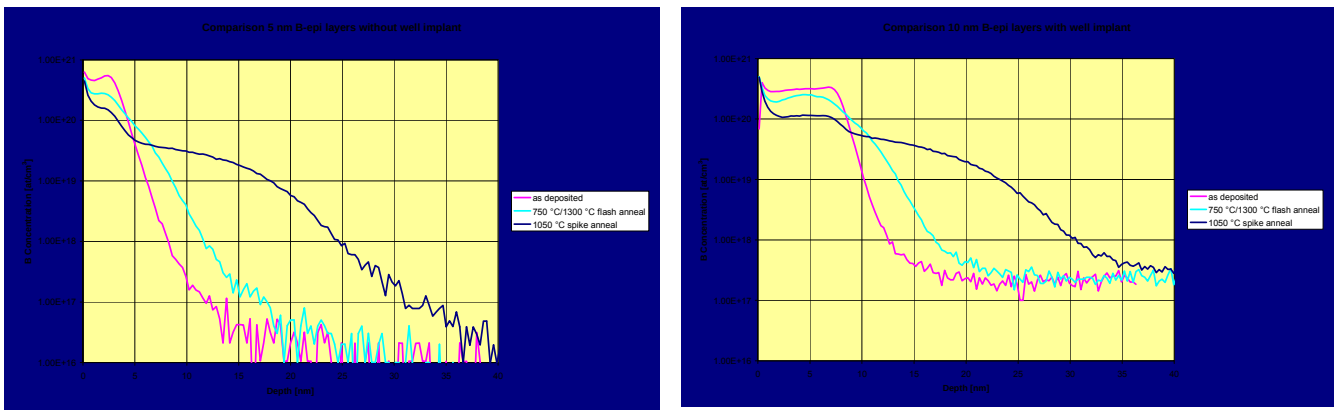

Figure 8: SIMS profiles of 5 nm B-epi layers without well implant (left) and 10 nm B-epi layer with well implant

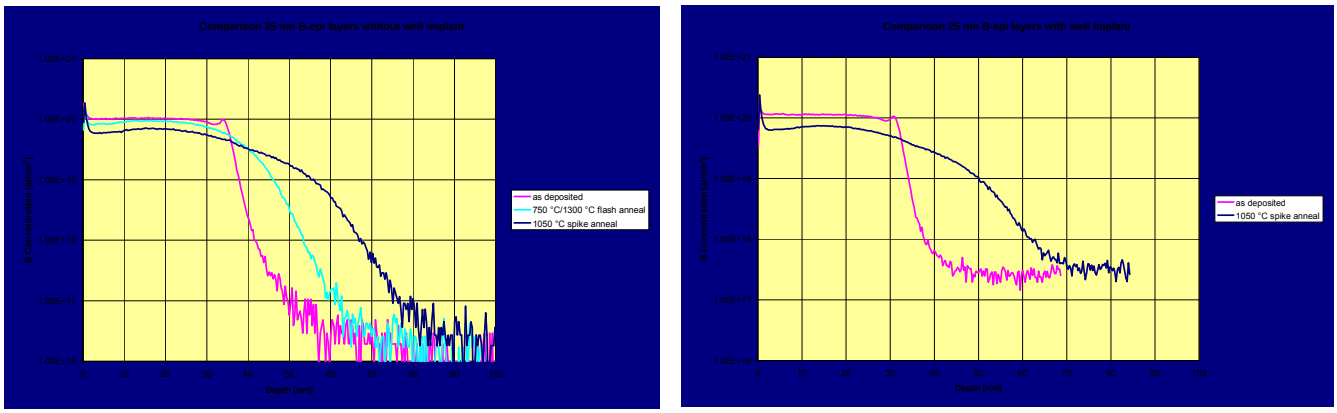

Figure 9: SIMS profiles of 25 nm B-epi layers without (left) and with (right) well implant

Table 1: Comparison of sheet resistance and electrically active dose of the SRP carrier concentration in relation to the chemical dopant profile determined by SIMS

			Rs Tencor Type D	Electrically Active Dose [%]	
Well	Epi-Layer		Mean 81 P [ohm/sq.]	with Standard Correction	with Surface Correction
x	B - 25 nm	as deposited	671.38	14.58	35.00
x	B - 25 nm	Spike	389.98	62.36	108.59
x	B - 25 nm	Flash	366.76		
x	As - 25 nm	as deposited	649.42	18.96	30.57
x	As - 25 nm	Spike	602.38	12.16	26.56
x	As - 25 nm	Flash	631.53	7.63	25.90

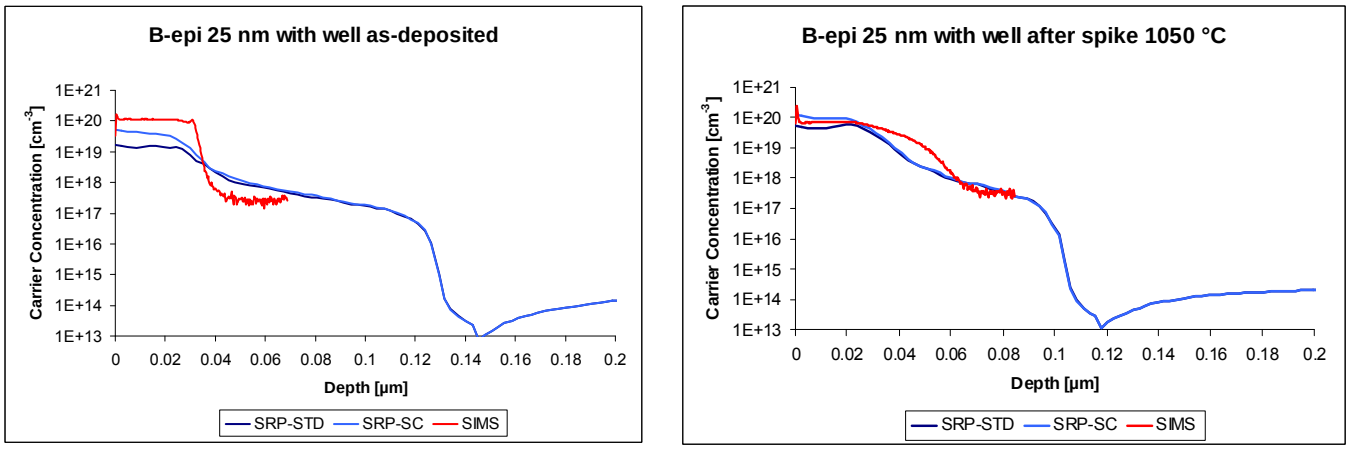

Figure 10: Comparison of electrical carrier concentration determined with SRP (STD: standard; SC: surface correction) to chemical concentration measured by SIMS for B-epi layer with nominally 25 nm with well implant for as-deposited and 1050 °C spike annealed wafers

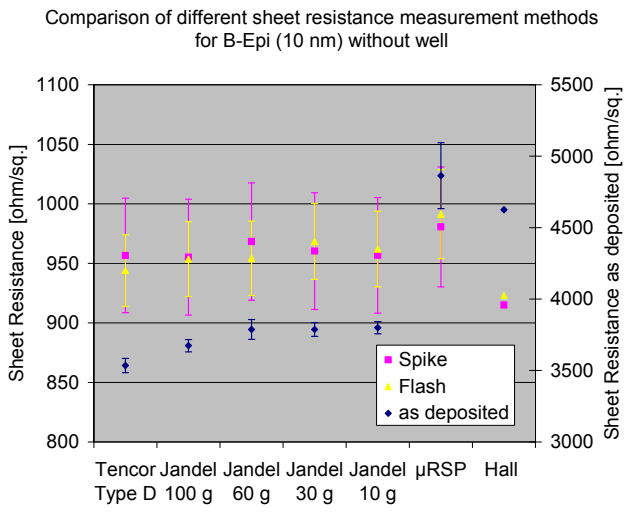

Figure 11: Comparison of different sheet resistance measurement methods for B-epi (nominal 10 nm) without well, the error bars (if shown) represent the standard deviation of the respective measurement method

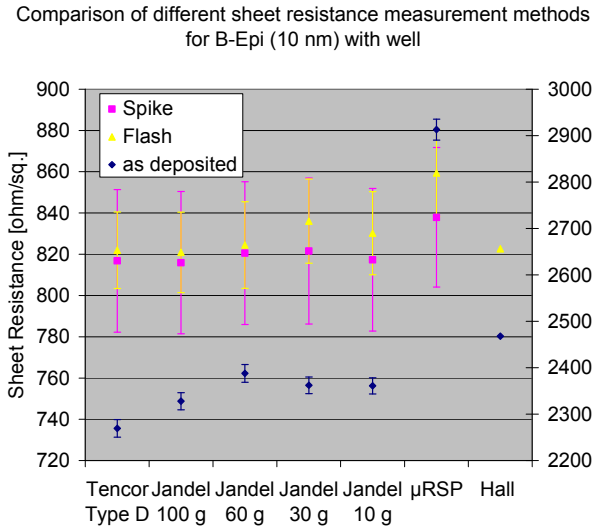

Figure 12: Comparison of different sheet resistance measurement methods for B-epi (nominal 25 nm) with well, the error bars (if shown) represent the standard deviation of the respective measurement method

Advanced layers (strained silicon, strained SiGe and relaxed SiGe)

In this task one requisition was to test if standard 4PP measurements on strained silicon, strained SiGe and relaxed SiGe wafers deliver reliable sheet resistance results. Different probe types D with probe loads of 10 g, 30 g, 60 g and 100 g were used for sheet resistance measurements.

4PP measurements on the relaxed SiGe samples from CNRS/LAAS with different probes as well as the van der Pauw measurements done by CNRS/LAAS reveiled that the best results regarding 4PP measurement are achieved with the KLA Tencor type D probe, which always shows the lowest standard deviation. No measurements were possible with the Jandel 60 g probe. The sheet resistance results of 4PP measurements at Mattson with KLA Tencor type D as well as the 4PP measurements done at CNRS/LAAS are compared to the results of VDP measurements in Figure 13 and Figure 14 below. For the low dose implant no 4PP Rs measurements on KLA Tencor type D were possible on the control Si substrate as well as the SiGe 20% sample. From Ge concentrations of 30% to 50% the Rs results between 4PP and VDP match quite well. The sheet resistance results of the high dose implant look even more consistent as the results of the different measurements are mainly within ±5% of the mean sheet resistance and in most cases even better. Boron SIMS profiles of both implant doses are shown in Figure 15.

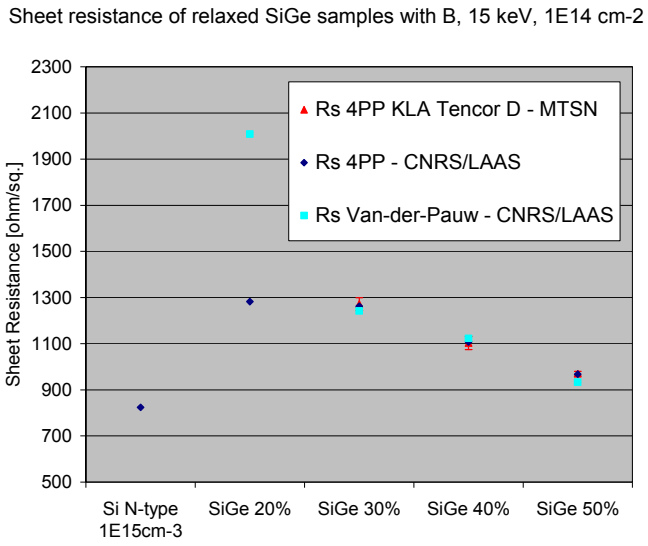

Figure 13: Comparison of sheet resistance of different measurement methods of relaxed SiGe samples with B, 15 keV, 1×10^{14} cm^{-2} implant

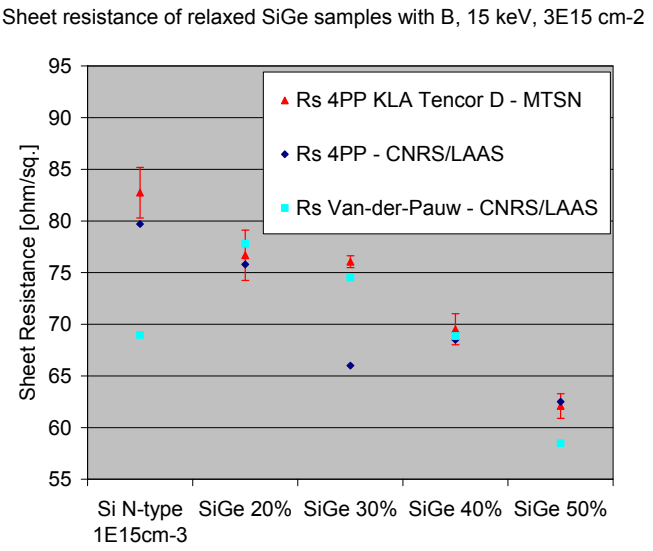

Figure 14: Comparison of sheet resistance of different measurement methods of relaxed SiGe samples with B, 15 keV, 3×10^{15} cm^{-2} implant

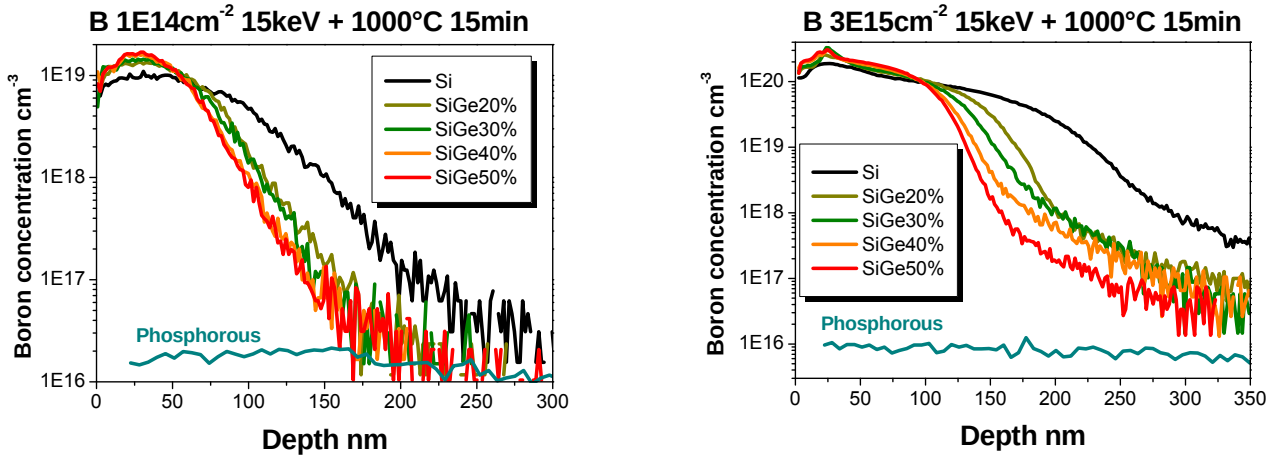

Figure 15: SIMS profiles of relaxed SiGe samples with B, 15 keV, 1×10^{14} cm^{-2} implant (left) and B, 15 keV, 3×10^{15} cm^{-2} implant (right), both after annealing at 1000 °C for 15 min.

The set of wafers prepared by IHP with strained silicon, strained SiGe and relaxed SiGe layers were annealed with temperatures between 700 °C and 1000 °C and for times ranging from a spike anneal to 1000 s steady state time.

These wafers were implanted with As (1 keV, 1×10^{15} cm^{-2}) or B (500 eV, 1×10^{15} cm^{-2}) in contrast to the samples provided by CNRS/LAAS with a B implant of 15 keV, the latter resulting in a junction depth between 100 nm and 250 nm, depending on dose and Ge content of the sample.

Good agreement between 4PP sheet resistance (KLA Tencor Type D) and VDP sheet resistance measurements were achieved with the As (1 keV, 1×10^{15} cm^{-2}) implanted strained SiGe wafers (see Figure 16). But the B (500 eV, 1×10^{15} cm^{-2}) implanted strained SiGe wafers could not be measured reliably with our standard 4PP tool and the KLA Tencor Type D probe. We experienced severe measurement problems also with a Jandel probe with 60 g probe load. VDP sheet resistance measurement resulted in consistent sheet resistance measurement results.

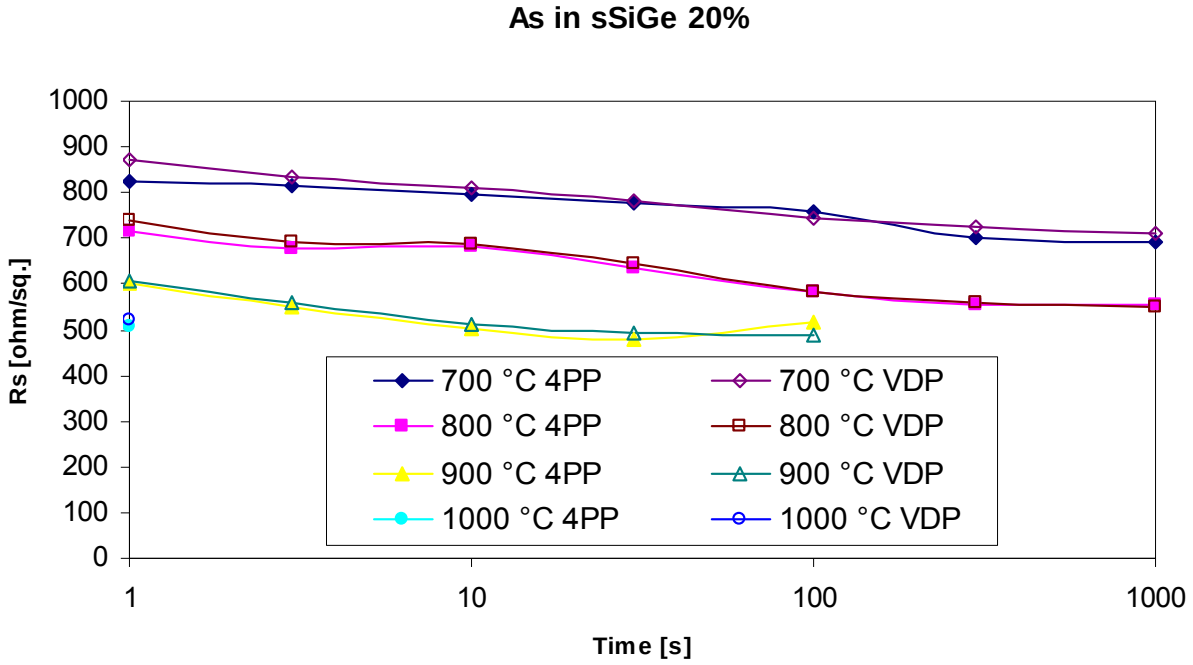

Figure 16: Comparison of sheet resistance of 4PP and VDP measurement of strained SiGe samples with As, 1 keV, 1×10^{15} cm^{-2} implant in dependence of annealing temperature and time

Similar measurement issues were also seen with relaxed SiGe and strained silicon wafers. There it looks like the Rs measurements show the background doping level of the wafer instead of the junction sheet resistance. With VDP consistent sheet resistance measurement results are achieved.

A possible explanation of the difficulties in sheet resistance measurement with sSi and relaxed SiGe wafers are rough surfaces of these wafers. AFM measurements done by IHP indicate that the relaxed SiGe wafers and the strained Si wafers show an average arithmetic roughness R_a between 1 nm and 2 nm, which is more then ten times higher than the roughness of the strained SiGe layers (see Table 2). The maximum roughness of the strained SiGe wafers is between 1.3 nm and 1.9 nm whereas the relaxed SiGe and the strained Si wafers show a maximum roughness between 14 nm and 24 nm. This high roughness is in the same order of magnitude as the as-implanted junction depth of the implanted layer which may lead to a penetration of the junction by the probe and hence only the background doping of the wafer is measured.

Table 2: Results of AFM measurements by IHP

Sample	Layer Structure	R_a [nm]	R_{max} [nm]
SHZ285-01	20 nm sSiGe 20%, As, 1 keV 1×10^{15} cm^{-2}	0.0956	1.86
SHZ285-03	15 nm sSiGe 20%, As, 1 keV 1×10^{15} cm^{-2}	0.0969	1.7
SHZ285-05	400 nm SiGe 20%, As, 1 keV 1×10^{15} cm^{-2}	1.32	17.9
SHZ285-07	20 nm sSi, As, 1 keV 1×10^{15} cm^{-2}	1.41	17.6
SHZ285-09	20 nm sSiGe 20%, B, 500 eV 1×10^{15} cm^{-2}	0.0985	1.27
SHZ285-11	15 nm sSiGe 20%, B, 500 eV 1×10^{15} cm^{-2}	0.097	1.27
SHZ285-13	400 nm SiGe 20%, B, 500 eV 1×10^{15} cm^{-2}	1.99	24
SHZ285-15	20 nm sSi, B, 500 eV 1×10^{15} cm^{-2}	1.18	14

2.4 4PP-imprint results

The surface of a silicon wafer is so hard, that the ball shaped probe tips can not leave a ball shaped imprint on the wafer surface. Instead there is a planar contact area between the probe tip and the wafer surface. This contact area gets smaller with smaller tip radius. Within this contact area, spikes of the probe tips micro-roughness penetrate the wafer surface and contact the USJ layer under the native oxide.

The imprints of the different probes used to characterize implanted wafers and epi-layers were evaluated with different measurement tools like Interferometry and Atomic Force Microscopy (AFM). To get an overview on the position of the different probe imprints the wafer was measured with a SP1 from KLA Tencor.

The imprints were evaluated on a 200 mm p-type wafer implanted with As, 20 keV, 1×10^{16} cm^{-2} which was spike annealed with a peak temperature of 1050 °C in an ambient of 10% O_2 in N_2 prior to sheet resistance measurement. The tested probes were four different D-type probes from Jandel with 100 g, 60 g, 30 g and 10 g probe load as well as probes from KLA Tencor "D new" (a newly bought probe), "D old" (a worn out probe with measurement problems) and an "A" probe. The geometrical data of these probes are summarized in Table 3.

Table 3: Geometrical data of tested probes

Probe Type	Tip Radius [mm]	Spacing [mm]
Jandel D 100 g	0.508	1.016
Jandel D 60 g		
Jandel D 30 g		
Jandel D 10 g		
KLA Tencor D new		
KLA Tencor D old		
KLA Tencor A	0.0406	

Light point defect measurements were run on a KLA Tencor SP1 at Mattson Thermal Products. AFM measurements were conducted at FhG IISB on a Dimension 5000 Scanning Probe Microscope, operated in tapping mode which has a limitation in max. lateral scan width of 50 µm.

The AFM topography picture and the line scan of the, Jandel 30 g probe is shown in Figure 17 below. The Jandel 10 g probe could not be measured with AFM as the imprints were not visible and could not be found. The other probes show only spikes of the probe tips micro-roughness.

The AFM measurements showed a polynomial dependence of 2nd order of the probe penetration with probe weight (Figure 18). I.e. that for a probe weight of 30 g to 100 g the penetration depth varies only between 2 nm and 4 nm. The average probe penetration depth of the used Jandel probes and the Tencor D new probe is smaller than 5 nm indicating that they do not punch through the implanted or epi-layers and are suited for sheet resistance measurements of shallow layers.

2.5 Conclusions

Different methods were compared to characterize sheet doping and doping profiles on shallow implanted as well as grown epi-layers with p- and n-type junctions.

On shallow $^{11}B^+$, $^{49}BF_2^+$ and $^{75}As^+$ implanted layers sheet resistance measurements with four point probe (4PP) were performed with a state of the art KLA Tencor RS100 with different probe loads on shallow n- and p-type doped wafers that were spike and flash annealed. In general spike or flash annealed standard B, BF_2 and As shallow implants can be measured with four point probes with weights from 100 g down to 30 g without any measurement issues. Also few measurement problems are seen with the use of a deep p^+p respectively n^+n implantation. The spike annealed arsenic implants can not be

measured with a 10 g probe due to the oxide layer formed during annealing in an ambient with 10% O_2 in N_2.

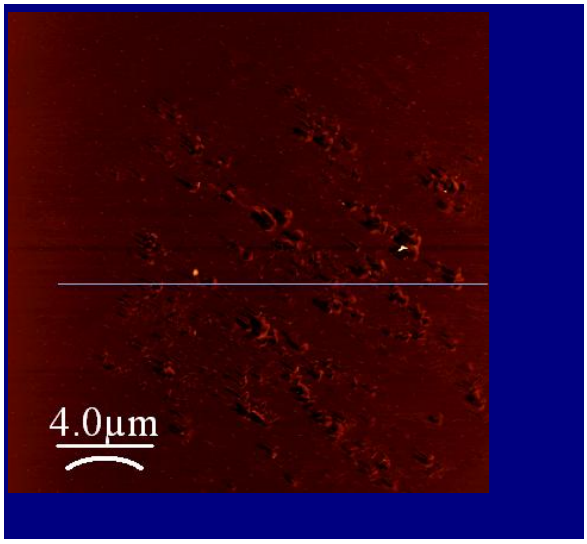

Figure 17: AFM topography of Jandel 30 g probe

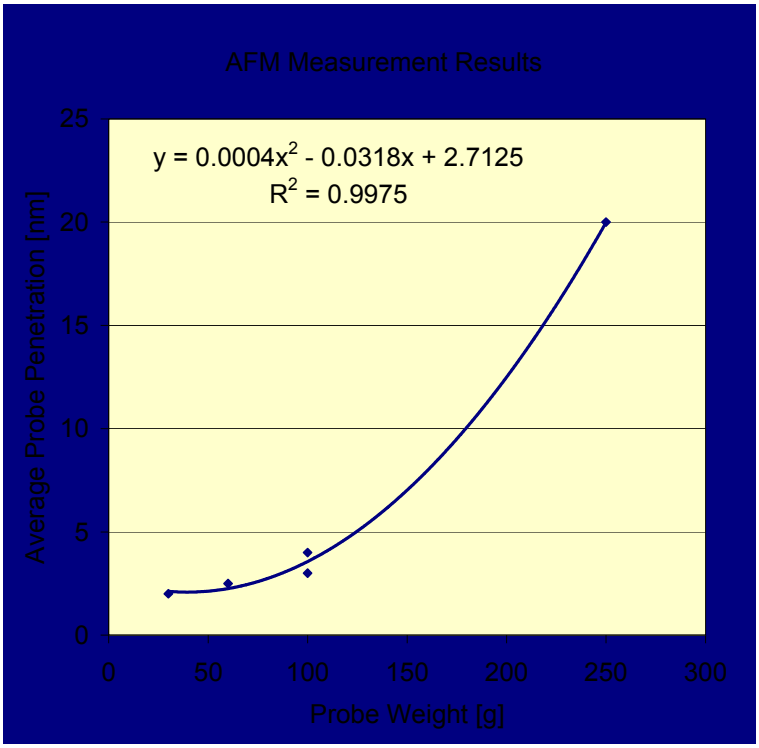

Figure 18: Summary of AFM measurement results showing probe penetration versus probe weight

For further tests boron and arsenic epi-layers were chosen because of their flexibility to produce junctions with defined depths. SIMS measurements on the as-grown B- and As-epitaxial layers showed that the layers are not always matching the requested target thickness. Sheet resistance measurements on B- and As-epitaxial layers with the different probes show that reliable measurements of shallow B-epi layers down to 35 nm (nominal layer thickness 25 nm) are possible with all probe loads. Shallower layers should be measured with a probe load smaller than 60 g. For As-epi layers reliable measurements are possible down to 30 nm layer thickness (nominal 10 nm) with probe loads from 100 g down to 30 g. Only shallower layers should be measured with the 60 g or 30 g probe. Good agreement (below 10% standard deviation) of Hall-effect and sheet resistance measurements has been already shown by several authors.

In collaboration with CAPRES some wafers were measured for their sheet resistance using a micro-4PP tool (µRSP). In general we see good agreement (~10%) between 4PP, Hall-effect and µRSP measurement results. µRSP measurements usually show a higher sheet resistance value than the other methods.

Hall-effect measurements (done at CNRS/LAAS) of the boron doped epitaxial layers showed that with the exception of the thickest layer (100 nm), all the as-grown samples were not fully electrically active and exhibited a degradation of the drift mobility possibly due to the presence of boron interstitial clusters (BICs). In all cases, the maximum active dopant concentration, C_{el}, was found to be close to the boron solid solubility at the growth temperature. In the annealed samples, it was also found that C_{el} is located in correspondence of the “kink” position (when visible) in the SIMS profiles. The post-annealing

steps (either 1050 °C spike or 1300 °C flash) improve the activation level of all the investigated samples, and induce a corresponding improvement of the carrier mobility.

4PP measurements done on sSiGe, relaxed SiGe and strained silicon layers often show no reasonable measurement results. Only relatively deep (150-250 nm) B-doped (15 keV, 3×10^{15} cm^{-2}) relaxed SiGe layers as well as shallow As-doped (1 keV, 1×10^{15} cm^{-2}) sSiGe layers (not shown here) could be reliably measured with a KLA Tencor Type D probe. Van der Pauw measurements of sSiGe, relaxed SiGe and strained silicon layers are an alternative way, although much more complex, to measure the sheet resistance of such layers.

From all the different wafers investigated within this work, ranging from shallow boron and arsenic implanted silicon wafers over doped epi-layers as well as sSiGe, relaxed SiGe and strained silicon layers, a recommendation regarding sheet resistance measurement with 4PP is drawn and shown in Table 4.

The imprints of probes with different probe loads (100 g, 60 g, 30 g and 10 g) used to characterize implanted wafers and epi-layers were evaluated. The wafer was then sent to IISB for atomic force microscopy (AFM) measurements. The AFM measurements showed a polynomial dependence of 2nd order of the probe penetration with probe weight. I.e. that for a probe weight of 30 g to 100 g the penetration depth varies between 2 nm and 4 nm explaining the fact that we can reliably measure the sheet resistance of very shallow doped layers independently if they are implanted or grown.

Table 4: Recommendations for sheet resistance measurement with 4PP

		X_J @ 1×10^{18} cm^{-3} [nm]	**100 g**	**60 g**	**30 g**	**10 g**
Implantation	B, 500 eV, 1×10^{15} cm^{-2}	~30	✓	✓	✓	✓
	BF_2, 1.1 keV, 1×10^{15} cm^{-2}	~17	✓	✓	✓	
	As, 500 eV, 1×10^{15} cm^{-2}	~14	✓	✓	✓	
Epi-layer	B, 5 nm	~8		✓	✓	✓
	B, 10 nm	~13		✓	✓	✓
	B, 25 nm	~39	✓	✓	✓	✓
	B, 100 nm	~135	✓	✓	✓	✓
	As, 5 nm	~14		✓	✓	
	As, 10 nm	~32	✓	✓	✓	
	As, 25 nm	~42	✓	✓	✓	
	As, 100 nm	~91	✓	✓	✓	
Strained Si	B, 500 eV, 1×10^{15} cm^{-2}		no reasonable measurement possible			
	As, 1 keV, 1×10^{15} cm^{-2}					
Strained SiGe	B, 500 eV, 1×10^{15} cm^{-2}					
	As, 1 keV, 1×10^{15} cm^{-2}		✓			
Relaxed SiGe	B, 500 eV, 1×10^{15} cm^{-2}		no reasonable measurement possible			
	As, 1 keV, 1×10^{15} cm^{-2}					
	B, 15 keV, 3×10^{15} cm^{-2}	150 – 250	✓			

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3 Arsenic segregation at the Si/SiO_2 interface

Due to the continuous shrinking of the dimensions of semiconductor devices and the corresponding increase of the dopant concentration, dopant activation becomes one of the dominant problems. One of its limiting factors is the segregation and pile-up of dopants at the SiO_2/Si interface. Experimental results have shown that the piled-up dopants are immobile [8,9] and can be removed by a dip in hydrofluoric acid [10]. It was also found that the segregation occurs on the silicon side of the interface [11,12,13] in a region larger than 1 nm [12,13]. Since the work of Sai-Halasz *et al.* [8], it was believed that the segregated arsenic atoms are electrically inactive. Only recently, Frühauf [14] suggested that 10–20% of the segregated arsenic atoms are electrically active. To extend the experimental information available, the pile-up of arsenic at the Si/SiO_2 interface after As implantation and annealing was investigated by high resolution *Z*-contrast imaging, electron energy-loss spectroscopy (EELS), grazing incidence x-ray fluorescence spectroscopy (GI-XRF), secondary ion mass spectrometry, x-ray photoelectron spectroscopy, Rutherford backscattering spectrometry, as well as Hall mobility and four-point probe resistivity measurements [15]. After properly taking into account their respective artefacts, the results of all methods are compatible with each other, with EELS and GI-XRF combined with etching providing similar spatial resolution on the nanometer scale for the dopant profile. The GI-XRF method in combination with etching and electrical measurements allowed to investigate the interface segregation of arsenic over a wide range of concentrations [16].

The experimental methods mentioned above allowed the characterization of arsenic profiles at the interface. Figure 19 shows the profiles after implantation with arsenic doses of 10^{15} and 10^{16} cm^{-2} and annealing for sufficiently long times to bring the concentration at the interface into steady state with the electrically active arsenic concentration in the bulk. The inserts indicate the etching steps after which the residual dose was characterized by GI-XRF. Within the accuracy of the method, the reconstructed profile corresponds to the profile found from EELS measurements.

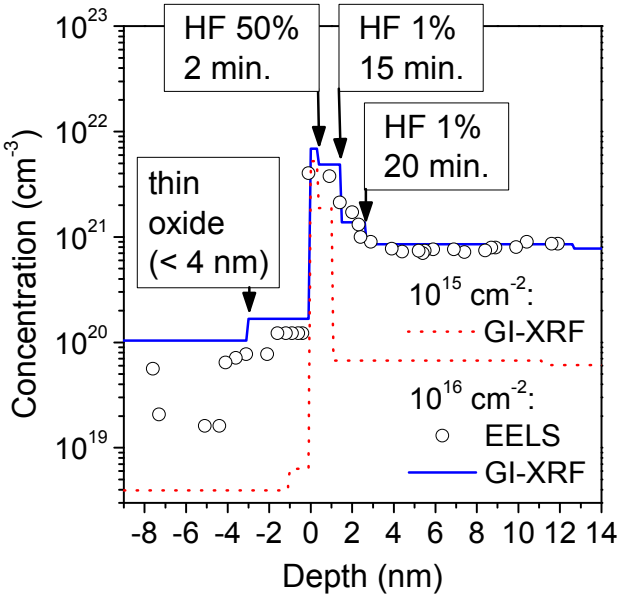

Figure 19: Concentration profile of arsenic at the interface determined by combining the results from the step height measurements and GI-XRF measurements for samples implanted with doses of 1×10^{15} and 1×10^{16} cm^{-2} before annealing them at 900 °C for 360 min and 1000 °C for 30 min, respectively. Also shown are the results from EELS measurements for the sample implanted with a dose of 1×10^{16} cm^{-2} and annealed for 360 min at 900 °C.

From the profiles shown it becomes apparent that the thickness of the pile-up layer increases with the sheet concentration of arsenic segregated at the interface, which itself is a monotonically increasing function of the substitutional arsenic concentration. After annealing at 900 °C for 360 min, the pile-up extended to a depth of about 2.7 nm for an implant dose of 1×10^{16} cm^{-2}, and to about 1.1 nm in a sample implanted with a dose of 1×10^{15} cm^{-2} and annealed at 1000 °C for 30 min. For an arsenic dose of 1×10^{14} cm^{-2} annealed at 1000 °C for 30 min, the segregation layer was estimated to be thinner than 0.5 nm.

By varying the annealing time, it was verified that the pile-up at the interface reflects a steady-state condition. Additional experiments were carried out to confirm that the pile-up was an intrinsic property of the interface. Hydrogen was not found to affect the pile-up under the conditions studied. Similarly, an oversaturation of self-interstitials by 1 order of magnitude induced by an oxidation process was not found to have a significant influence.

The relationship between the corrected sheet concentration of piled-up arsenic atoms and the background concentration of substitutional, active arsenic atoms is shown in Figure 20. It is approximately linear below a background concentration of about 5×10^{18} cm^{-3}. For higher concentrations, until a sheet concentration of segregated arsenic atoms of about 2×10^{14} cm^{-2} is reached, the increase is approximately quadratic. For even higher background concentrations, a reduction of the slope and finally a saturation become apparent.

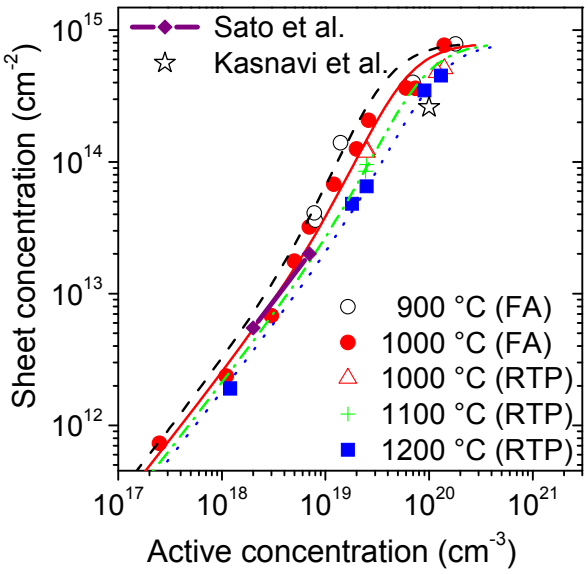

Figure 20: Sheet concentration of piled-up arsenic as a function of the arsenic concentration below the pile-up region. The lines correspond to model predictions

Experimental data summarized previously by Dabrowski *et al.* [17] for phosphorus showed a similar linear/quadratic behaviour, which was explained by trapping of dopants and the formation of dopant pairs at the interface. At least for our data, we suggest a simpler mechanism based on the assumption that the segregated arsenic atoms are deep donors. The electrical data allow a reasonable assumption that the majority of the segregated atoms are electrically neutral for substitutional arsenic concentrations up to about 3×10^{20} cm^{-3}. These defects As^0_{seg} can be thought to result from the reaction

$$As_s^+ + e^- \leftrightarrow As^0_{seg}$$

between positively charged substitutional arsenic atoms As_s^+ and free electrons e^-. In steady state, the concentration of segregated arsenic atoms in the interface layer

$$C_{As_{seg}} \approx C_{As^0_{seg}} \propto C_{As_s^+} \times n$$

is then approximately equal to the concentration of neutral segregated arsenic atoms, which, in turn, is proportional to the product of the substitutional concentration of arsenic atoms $C_{As_s^+}$ and the electron concentration n. The latter can be approximately calculated from the assumption of charge neutrality and is then given by

$$n = C_{As_s^+}/2 + \sqrt{\left(C_{As_s^+}/2\right)^2 + n_i^2}$$

For substitutional arsenic concentrations below n_i, the electron concentration equals approximately n_i ($n \approx n_i$) and the concentration of segregated atoms increases linearly with the substitutional arsenic concentration. When the substitutional arsenic concentration exceeds the intrinsic carrier concentration significantly, the electron concentration approaches the concentration of substitutional atoms $n \approx C_{As_s^+}$ so that the concentration of segregated atoms increases quadratically with the substitutional arsenic concentration. At substitutional concentrations for which the segregated sheet concentration exceeds a level of about 2×10^{14} cm^{-2}, a reduction of the slope and finally a saturation is apparent in Figure 20. While the mechanism behind this saturation is not yet identified, it was found that it correlates for the 1000 °C data with an increase of the electrical activity of the segregated arsenic atoms from low to full electrical activity.

For an implementation into existing process simulation programs like Sentaurus Process, the three-phase model suggested first by Lau et al. [18] and Orlowski [19] can be adapted. It considers the trapping of atoms to and their emission from an interface layer with a maximum sheet concentration of sites that can be occupied. This maximum sheet concentration can be used to pragmatically model the saturation observed. The model was parameterized for the *ThreePhaseSegregation* model of Sentaurus Process and is able to predict the segregation of arsenic to the silicon/silicon dioxide interface in steady state within a wide range of experimental conditions.

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4 Arsenic activation and deactivation

In the wake of the continuing miniaturization of devices, there is a more and more pressing need towards shallower and steeper junctions with higher levels of activation to reduce short-channel effects. This is reflected on the one hand by a reduction of implant energies which are now in the sub-1 keV regime. On the other hand, to reduce diffusive broadening, the process times of source/drain annealings and source/drain extension annealings have reduced drastically from soak annealing for several seconds via high ramp-up spike rapid thermal annealing (RTA) to millisecond annealing (MSA). At the same time, increasing peak temperatures were used to raise the dopant activation.

We have investigated conventional annealing schemes (RTA, Spike) and MSA via flash lamp annealing. In our experiments, 200 mm (100) p-type Czochralski Si wafers were used. They were implanted with arsenic for three different combinations of energy and dose: 1 keV and 1×10^{15} cm^{-2}, 20 keV and 1×10^{15} cm^{-2}, as well as 20 keV and 1×10^{16} cm^{-2}.

In Figure 21 the measured temperature time profiles of the spike and flash annealing processes used in this investigation are shown.

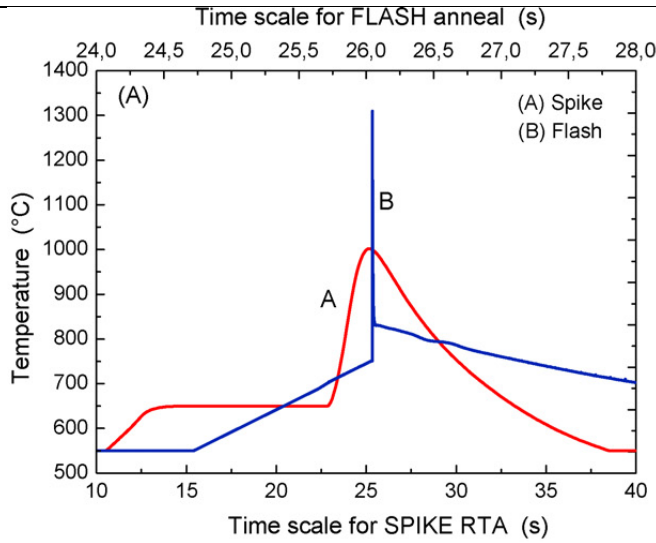

Figure 21: Measured temperature profile for spike and flash annealing

4.1 Conventional annealing

In order to investigate the deactivation and eventually reactivation processes in detail, the following annealing strategy was used: The procedure consisted of two annealing steps for each small sample. The first one (activation annealing) was either a spike annealing step or a short-time low-temperature annealing step to achieve full recrystallization (SPER) of the sample. The second steps (post-activation annealing) were isothermal and isochronal annealing series for temperatures between 700 °C and 900 °C and times up to 60 min in argon.

The evolution of the sheet resistance during post-activation annealing for the probes implanted with 20 keV and isothermally processed after SPER at 650 °C (a) and after 1050 °C spike annealing (b) is shown in Figure 22 (20 keV, 1×10^{15} cm^{-2}) and Figure 23 (20 keV, 1×10^{16} cm^{-2}).

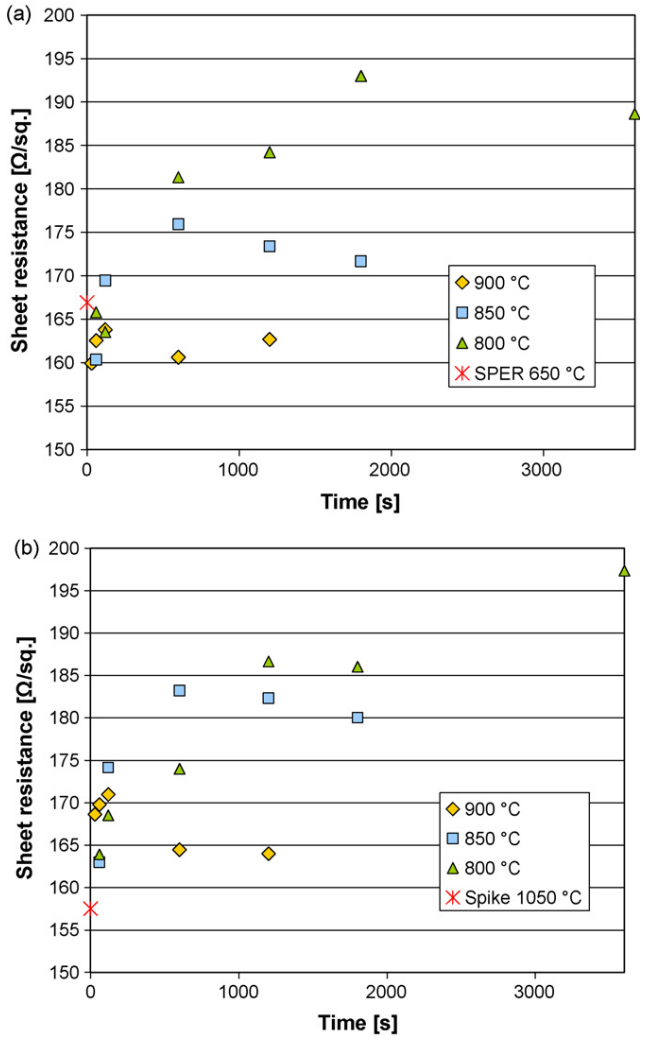

Figure 22: Sheet resistance vs. post-activation annealing time for 20 keV, 1×10^{15} cm^{-2} implantations, SPER (a) and spike (b) activation and isothermal post-activation annealing for different temperatures and times

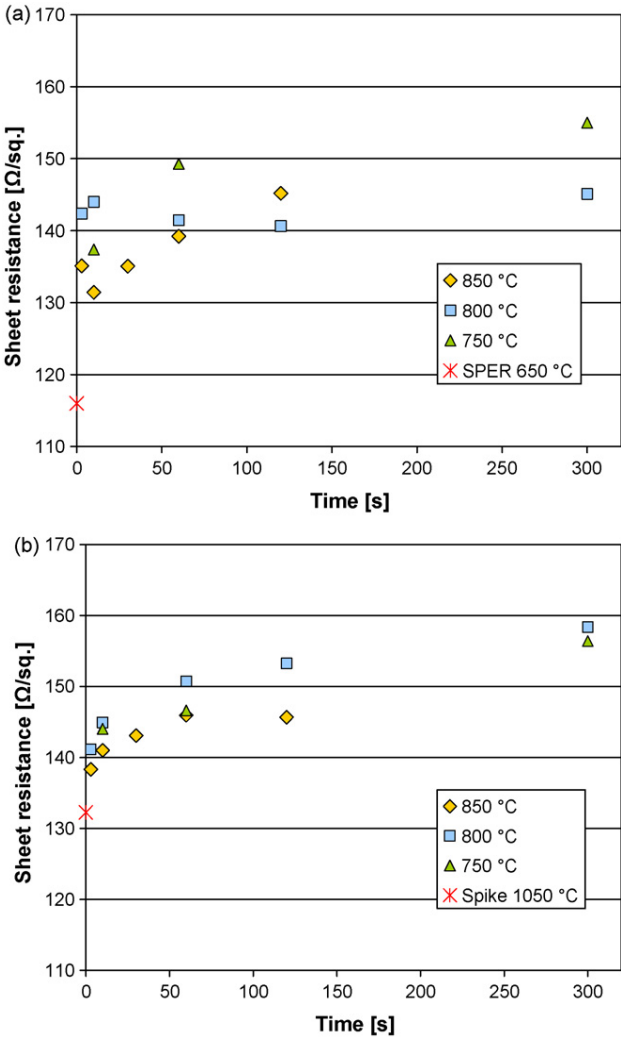

Figure 23: Sheet resistance vs. post-activation annealing time for 20 keV, 1×10^{16} cm^{-2} implantation, SPER (a) and spike (b) activation and isothermal post-activation annealing for different temperatures and times.

In general, a relatively low sheet resistance is obtained after the activation anneal. For highly doped samples, the electrically active concentration may even exceed the active solubility at the beginning of a post-activation annealing by far. Then, the sheet resistance is expected to increase due to deactivation during the initial phase of post-activation annealing. Eventually, for high thermal budgets, the sheet resistance decreases again when the total electrically active sheet concentration and the mobility increase due to the broadening of the profile.

Comparing the sheet resistances of the probes annealed under the same conditions after SPER and spike annealing, and taking in account the measurement errors (between 0.5 and 4.0%), no significant advantage of one of the two activation methods can be found for an implantation energy of 20 keV. For deep implants, no annealing scheme appears to be a better option than the others. Therefore it can be adapted to the process needs.

Contrary to case of deep implants are the results for the activation of the shallow implants. Figure 24 shows the evolution of the sheet resistance after activation and post-activation annealing at two different temperatures of our samples compared with results obtained previously for flash-activated samples with a similar post-activation annealing treatment [20].

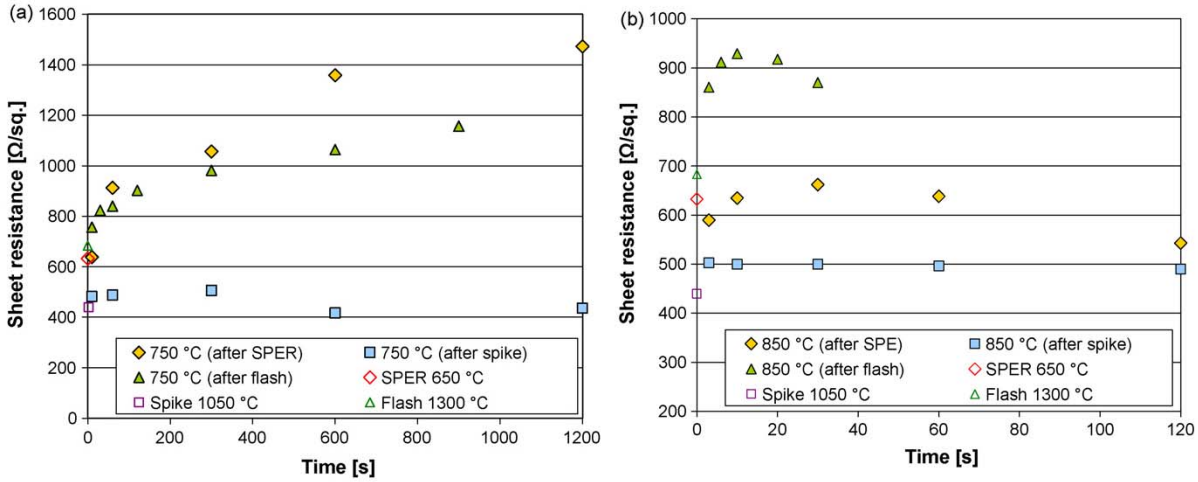

Figure 24: Sheet resistance vs. post-activation annealing time for 1 keV, 1×10^{15} cm^{-2} implantation, SPER, spike or flash-annealing activation, and isothermal postactivation annealing at 750 °C (a) and 850 °C (b) for different times.

It is apparent that spike-activated samples show the best results after post-activation annealing with very stable sheet resistances well below the ones of samples activated by SPER or flash annealing. At first sight, spike annealing would be the immediate choice for the activation of shallow implants, but there is a trade off between the sheet resistance and the junction depth using this type of annealing.

For shallow implants, SPE and flash annealing are the best option, because of the trade-off between activation and profile broadening with spike annealing.

4.2 Flash annealing

Different annealing schemes based on flash lamp MSA were evaluated to understand the activation mechanisms as well as the evolution of extended defects, with samples implanted with 1 keV arsenic, with a dose of 1×10^{15} cm^{-2}.

The as-implanted profile is shown in Figure 25a, together with the profiles after single and multiple-flash annealing processes with a peak temperature of 1300 °C. In all flash-annealed profiles, a dominant peak can be observed which originates from interface segregation. The first flash anneal induces significantly more diffusion than the second and third one. The sheet resistance is reduced by approximately 19% after a triple flash anneal in comparison to a single flash anneal. No extended defects were observed in a single flash-annealed sample, as shown in the TEM micrograph of Figure 25b. Considering the imaging conditions used here, this result means that defects, if they exist in such samples, are either too small (<2 nm) or have a too low density ($<10^{6}$ cm^{-2}) to be observable.

A graphical summary of the observed sheet resistance values after single and multiple flash annealings of arsenic implanted samples is given in Figure 26. The shown Hall-effect data for arsenic from 1300 °C flash-annealed samples are in good agreement (<<5%) to 4PP data.

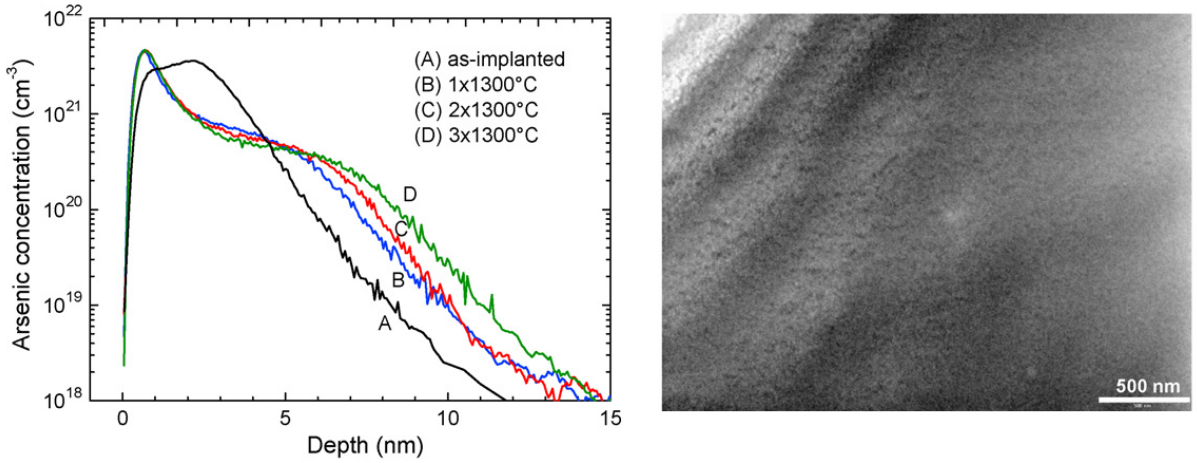

Figure 25: (a) SIMS profiles of as-implanted 1 keV arsenic (1×10^{15} cm^{-2}) in crystalline silicon (A) as well as of single (B), double (C), and triple (D) flash-annealed samples, (b)Weak beam dark field plan-view micrograph of flash-annealed arsenic-doped sample to study the effects of advanced temperature profiles on the evolution of defects (imaging conditions: WBDF, g=<422>, s<0). All defects in the sample are below the WBDF detection limit of $<10^6$ cm^{-2}.

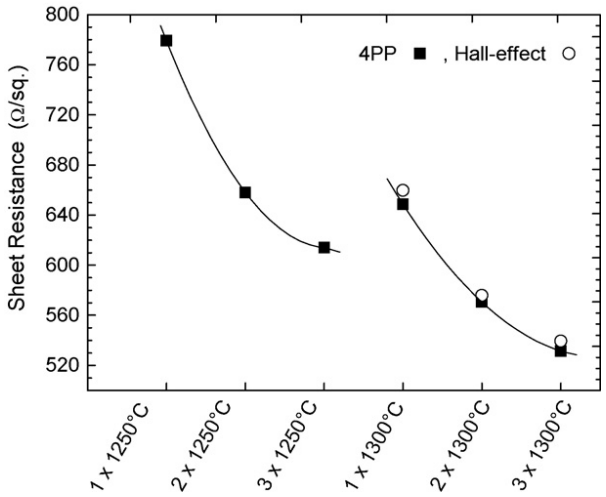

Figure 26: Data summary and comparison of sheet resistance values for1 keV arsenic (1×1015 cm−2) in crystalline silicon after a single, double, or triple flash anneal. The lines are to guide the eye.

Figure 27 shows the profile evolution for arsenic due to various advanced annealing schemes. Table 5 shows the sheet resistance measured with 4PP and Hall-effect.

The peak temperature of the MSA for this family of curves is 1300 °C. The shallowest junction results from the flash anneal only, followed by the spike RTA and flash annealing combination, the high intermediate flash anneal, and the flash annealing and spike RTA combination.

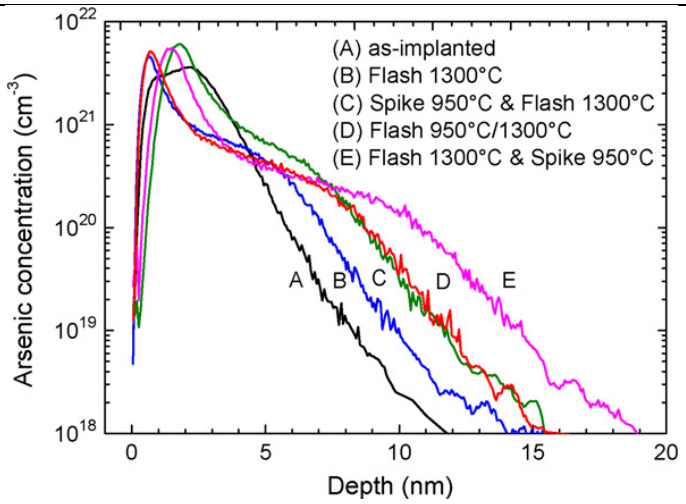

Figure 27: SIMS profiles of as-implanted 1 keV arsenic (1×1015 cm−2) in crystalline silicon (A) as well as after flash (750 °C/1300 °C) annealing (B), spike (950 °C) RTA and flash (750 °C/1300 °C) annealing (C), flash annealing with high intermediate temperature 950 °C/1300 °C (D), and flash (750 °C/1300 °C) annealing and spike (950 °C) RTA (E) are shown. The gaseous ambient for all thermal processes was 100 ppm of oxygen in nitrogen. Profile D has around 20% less retained dose compared to C

Table 5: Measured sheet resistance with 4PP and Hall-effect for advanced annealing schemes

Anneal	4PP (Ω/sq)	Hall-effect(Ω/sq)
Flash 1300 °C	648	660
Spike 950 °C & Flash 1300 °C	591	
Flash 950 °C/1300 °C	693	690
Flash 1300 °C & Spike 950 °C	694	722

The optimum activation with the lowest sheet resistance of 591 Ω/sq is achieved with the spike RTA and flash annealing combination, due to the thin protective oxide layer grown during the spike RTA prior to the flash annealing [21,22]. For concentrations of 2×10^{20} cm^{-3} and below the dopant profile after a high intermediate flash anneal is very similar to the profile after the spike RTA and flash annealing combination. However, the peak of the profile is much closer to the surface. For the flash annealing and spike RTA profile, the junction is much deeper than for the other processes. Subsequent to flash annealing, temperature rises to 800 °C and above in the form of soak or even spike anneals lead to considerable immediate and abrupt increases in sheet resistance (deactivation) [22].

There is a strong dependence of the sheet resistance increase on temperature, which indicates that the process responsible for the deactivation is thermally activated. It is usually associated with formation of SiAs precipitates as well as with the formation of small arsenic vacancy clusters [23]. In the experiments of Rousseau et al. [24], the involvement of vacancies in the arsenic cluster formation was observed especially for the deactivation of surface-near arsenic doped layers.

Assuming that a vacancy-arsenic complex is responsible for the deactivation, we can conclude from our measurements that its formation occurs very rapidly (within less than a second at 950 °C and above) although there should be an abundance of self-interstitials from the implantation process. For spike temperatures above 850 °C, the immediately and abruptly increased sheet resistance (by AsV pair formation [22]) starts to decrease monotonically. Below 850 °C, the sheet resistance increased with

annealing time (deactivation) followed by a drop in sheet resistance [22]. The slower reactivation is associated at least in part by profile broadening.

Repeated flash annealing allows reducing sheet resistance, but entails profile broadening. The results of the deactivation behaviour with several combinations of spike and flash annealing are compatible with a deactivation mechanism involving vacancy-arsenic complex. Furthermore no extended defects are observed after flash annealing.

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5 Antimony activation and deactivation

Antimony could be a better option than arsenic to achieve the goals of the International Technology Roadmap for Semiconductors, as shown in [25] and [26]. The three key requirements for future devices are: reducing junction depth, increasing junction steepness, and maintaining a low sheet resistance. We have made experiments with SPE and Spike annealing, followed by a deactivation annealing, to investigate the diffusion and activation/deactivation behaviour of antimony.

In particular, the following annealing strategy was used, which consisted of two annealing steps for each sample. The first one (activation annealing) was either a spike annealing step or a short-time low-temperature annealing step to achieve full recrystallization (SPER) of the sample. The second steps (post-activation annealing) were isothermal and isochronal annealing series for temperatures between 750 °C and 900 °C and times up to 60 min in argon.

5.1 Deep implants

The evolution of the sheet resistance during post-activation annealing for the probes implanted with 20 keV, 1×10^{15} cm^{-2}.and isothermally processed after SPER at 650 °C is shown on Figure 28. The evolution after 1050 °C spike annealing is shown on Figure 29.

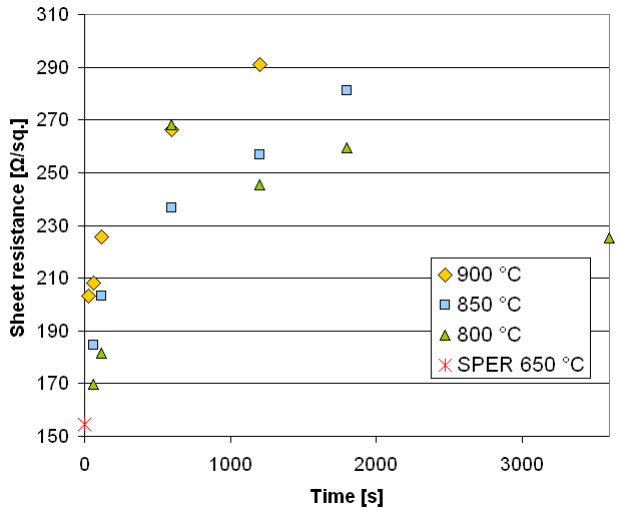

Figure 28: Sheet resistances measured with 4PP after SPE activation and post-activation annealing, for the Sb 20 keV 1×10^{15} cm^{-2} implantation.

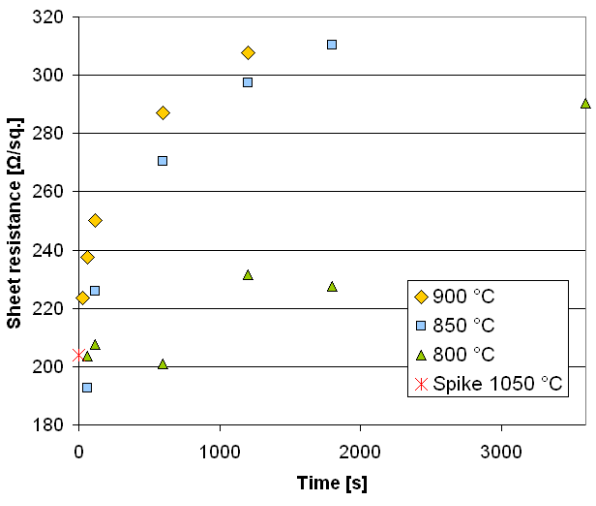

Figure 29: Sheet resistances measured with 4PP after Spike activation and post-activation annealing, for the Sb 20 keV 1×10^{15} cm^{-2} implantation.

The lowest sheet resistance is obtained before SPE or Spike annealing, and it then always increases with post-activation annealing time.

Figure 30 presents the SIMS results obtained for the SPE activation annealing and Figure 31 the results for the Spike activation annealing.

Directly after SPE there is no apparent dopant shift toward the surface due to solid phase epitaxy, the peak of the profile remains unchanged. After 900 °C, 120 s post-annealing, there is no visible diffusion in the tail of the profile, however the peak concentration has been lowered and a peak is visible at the surface. When the thermal budget is increased with 1200 s post-activation annealing, the profile broadens. After the spike annealing there is only little diffusion in the tail of the profile, but the peak observed in the SPE case is directly observable. When the thermal budget is increased the profile then broadens.

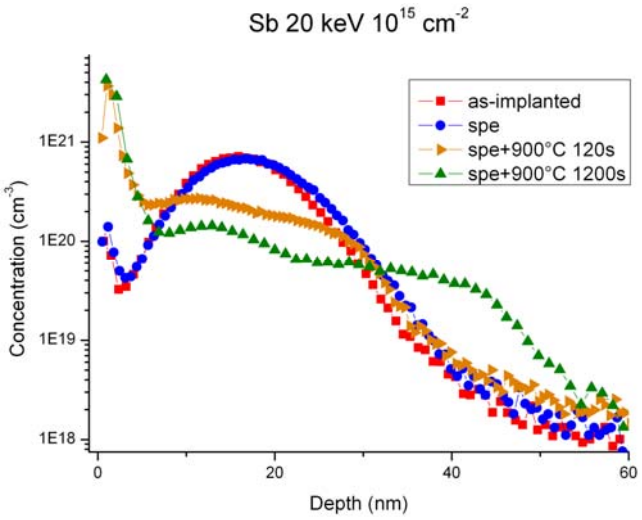

Figure 30: SIMS profiles measured after SPE activation and post-activation annealing, for the Sb 20 keV 1×10^{15} cm^{-2} implantation.

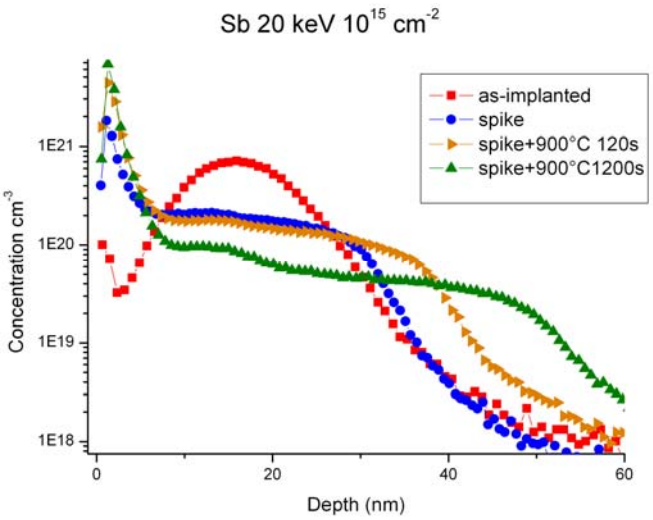

Figure 31: SIMS profiles measured after Spike activation and post-activation annealing, for the Sb 20 keV 1×10^{15} cm^{-2} implantation.

In order to investigate the peak visible on the SIMS profile, a TEM observation was made on an annealed sample. The result can be seen on Figure 32.

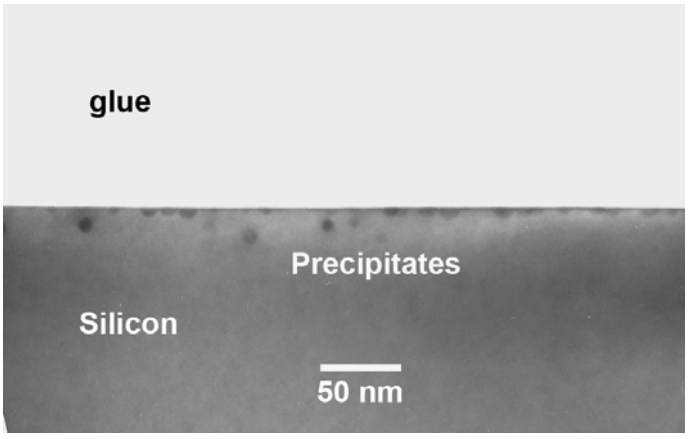

Figure 32: Image of surface near precipitates in Silicon implanted with 20 keV, 10^{15} cm^{-2} Sb, with spike activation annealing and 800 °C 120 s post-activation annealing.

Clusters are visible in an area extending to 10 nm under the surface. Keeping the peak observed at the surface on the SIMS profiles in mind the clusters can be thought to be made of antimony atoms. This phenomenon of antimony pile up and clustering under the surface has already been reported in [27,28,29].

With these results it is possible to propose an explanation for the higher sheet resistance obtained in the Spike case: after the Spike annealing step, antimony atoms pile up at the surface and become inactive, which explains the higher sheet resistance obtained in this case.

A higher dose was studied with a 20 keV, 1×10^{16} cm^{-2} implantation, to see whether more antimony atoms can be substitutionaly incorporated in silicon. Figure 33 and Figure 34 present the corresponding sheet resistance measurements.

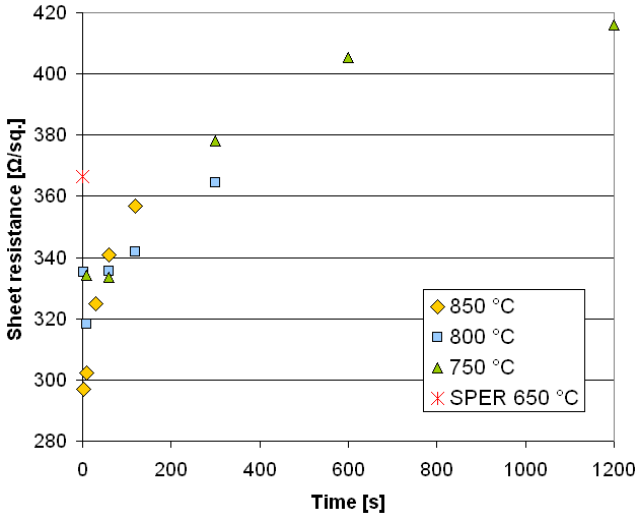

Figure 33: Sheet resistances measured with 4PP after SPE activation and post-activation annealing, for the Sb 20 keV 1×10^{16} cm^{-2} implantation.

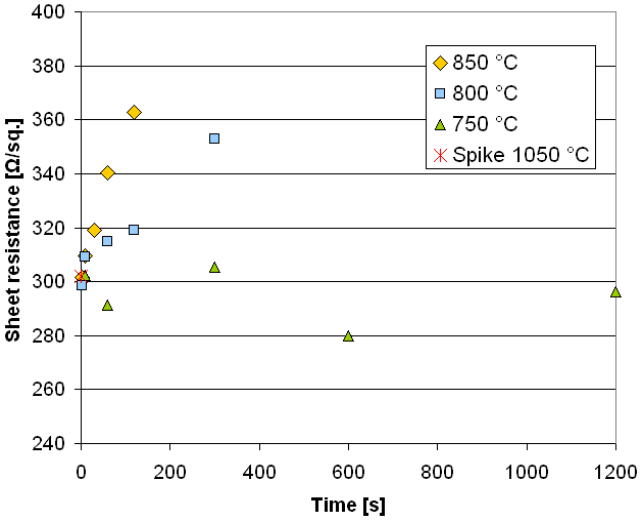

Figure 34: Sheet resistances measured with 4PP after Spike activation and post-activation annealing, for the Sb 20 keV 1×10^{16} cm^{-2} implantation.

The sheet resistance measured after the SPE activation step is noticeably higher than for the lower dose, and decreases during post-activation annealing This is probably due to the fact that with 10^{16} cm^{-2}, the amorphized depth is larger and the SPE annealing step is not sufficient to fully recrystallize the amorphous material. Recrystallization is then achieved during post-activation annealing, and the sheet resistance decreases. As observed before, the sheet resistance increases monotically with the post-activation annealing time.

The same trend is observed in the Spike case, except in the 750 °C case. This could be due to the fact that, contrary to the SPE case, there is already a number of antimony atoms trapped in clusters under the surface after the Spike activation step, and the thermal budget at 750 °C is not enough the cause more deactivation.

For deep implants it is not possible to get more substitutional antimony atoms by increasing the implanted dose, and post-activation annealing increases the sheet resistance. This is to be taken into account in the design of new processes, if antimony doping is followed by other steps. A clustering phenomenon is observable under the surface too, which is probably responsible for dopant deactivation.

5.2 Shallow implants

The same annealing procedure was applied for shallow implants. Figure 37 and Figure 38 show the sheet resistance measurements obtained for 3 keV, 1×10^{14} cm^{-2}, and Figure 39 and Figure 40 the for the 3 keV, 1×10^{15} cm^{-2}.

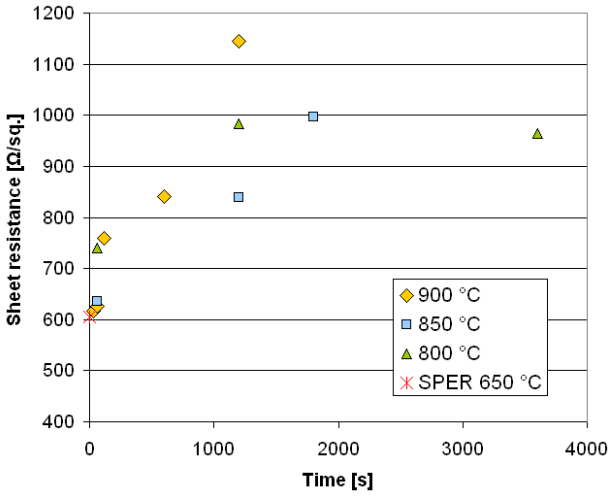

Figure 35: Sheet resistances measured with 4PP after SPE activation and post-activation annealing, for the Sb 3 keV 1×10^{14} cm^{-2} implantation.

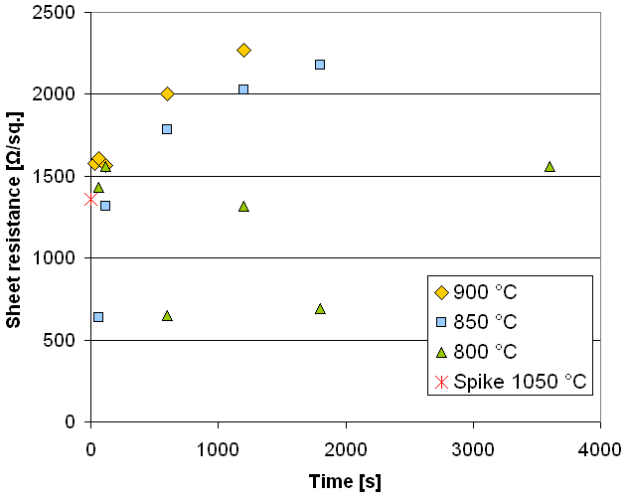

Figure 36: Sheet resistances measured with 4PP after Sike activation and post-activation annealing, for the Sb 3 keV 1×10^{14} cm^{-2} implantation.

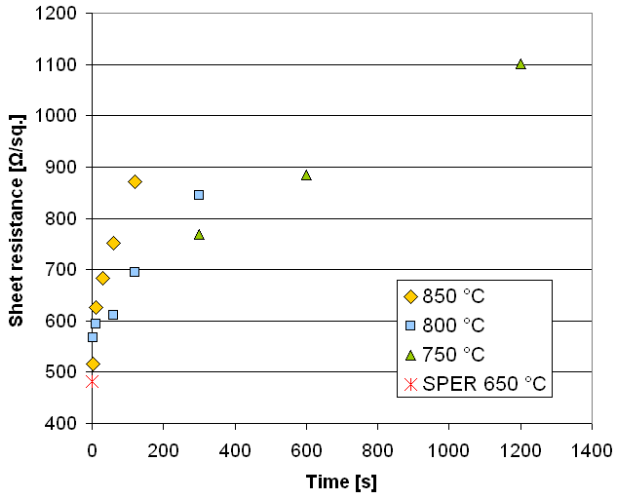

Figure 37: Sheet resistances measured with 4PP after SPE activation and post-activation annealing, for the Sb 3 keV 1×10^{15} cm^{-2} implantation.

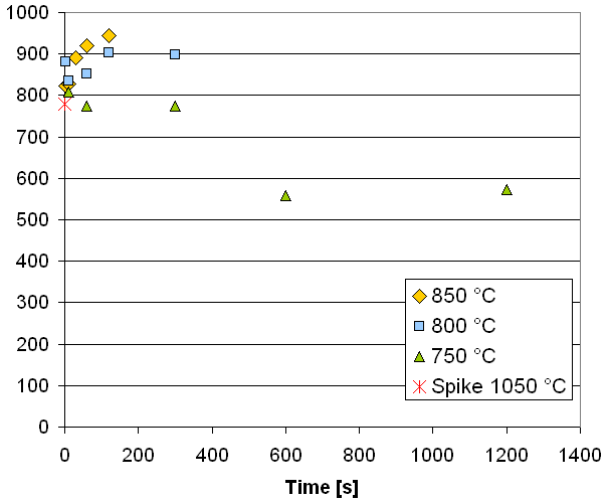

Figure 38: Sheet resistances measured with 4PP after Spike activation and post-activation annealing, for the Sb 3 keV 1×10^{15} cm^{-2} implantation.

In the SPE activation annealing case, the trend is essentially the same as for deep implants. The lower sheet resistance is obtained directly after the SPE step, and then increases with post-activation annealing time. The lowest sheet resistance is obtained with the higher 1×10^{15} cm^{-2} dose.

For the Spike case after some of the lowest thermal budget post-activation annealings it is possible to reduce the sheet resistance. The lowest attainable sheet resistance is almost the same for the two doses, with a value approaching 500 Ω/sq.

Figure 39 and Figure 40 show the SIMS results obtained for the 3 keV, 1×10^{15} cm^{-2} implantation.

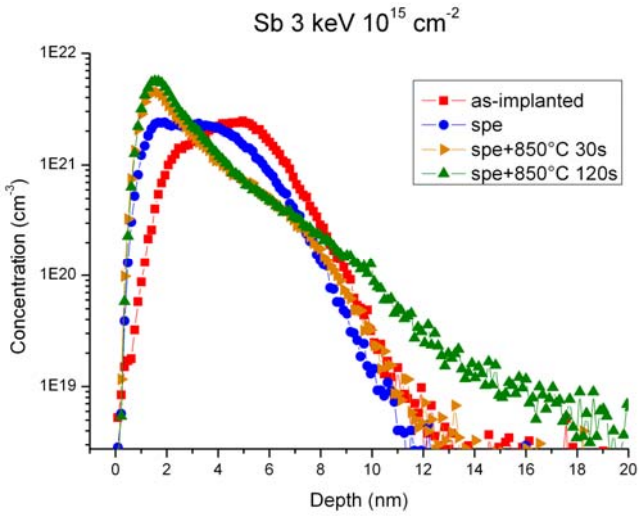

Figure 39: SIMS profiles measured after SPE activation and post-activation annealing, for the Sb 3 keV 1×10^{15} cm^{-2} implantation.

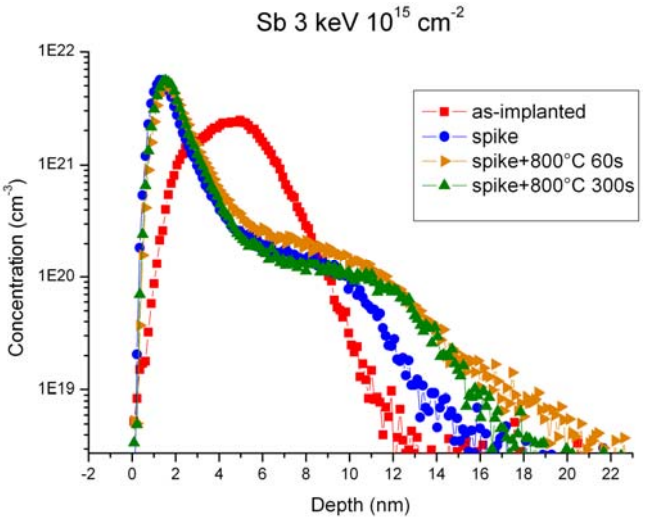

Figure 40: SIMS profiles measured after Spike activation and post-activation annealing, for the Sb 3 keV 1×10^{15} cm^{-2} implantation.

As for the 20 keV implantation, a peak is visible near the surface, which forms directly after Spike but not directly after SPE. If the thermal budget for activation is low enough, it is possible to avoid a too large broadening of the profiles.

For shallow implants, contrary to deeper implants, the higher dose allowed to achieve a lower sheet resistance. It appears too that post-activation annealing can be adapted in order to reduce dopant deactivation.

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6 Model development for vacancy engineering

A high level of electrical activation of dopants is essential for formation of low resistance contact doping in silicon based devices. High-dose co-implantation of non-dopant ions such as Si can be used to create separated vacancy-rich and interstitial-rich crystalline silicon regions – the vacancy-rich region near the surface and the interstitial-rich region deeper in the silicon – in order to modify the activation and diffusion behaviour of a subsequently implanted dopant. This approach can be beneficial for enhancing boron activation in ultra shallow junctions, since the excess of vacancies close to the entry surface of the Si ion beam acts to control transient enhanced diffusion and clustering of boron ions implanted after the Si implant step [30].

During annealing, the evolution of the excess vacancies and interstitials governs the dopant diffusion and activation. Vacancies aggregate into clusters and also diffuse into the substrate and to nearby interfaces. Interstitials behave in a similar way, and the two species interact with each other through diffusion and recombination. Vacancies and interstitials also interact with dopant atoms according to the diffusion mechanism of each particular dopant species. While the details of interstitial cluster evolution have been well established, modelled and calibrated, only limited vacancy cluster models have been reported. Previously reported theoretical studies on vacancy clustering [31,32] are limited to V cluster formation and evolution without interactions with other dopants or defects. This limits the accuracy of predictions of optimised vacancy engineering conditions, since the magnitude and time evolution of excess vacancy concentrations and their interaction with dopant diffusion cannot be reliably simulated. To our knowledge, the present study is the first attempt that has been made to model the combined impact of I- and V-clustering on dopant diffusion and activation.

6.1 Vacancy and interstitial cluster modelling

In the present study we have investigated the effect of Si co-implantation on B diffusion and activation with the help of a newly developed vacancy cluster model together with the existing interstitial cluster model available in Sentaurus Process. Only small V_n clusters with $n = 2-10$ are included in our analysis since a relatively low energy Si implant was used compared to other experiments and no large voids were observed after annealing. The V_n structures included in the model are those which act as precursor defects for the most stable octahedral void and this sequence is shown in Figure 41 [33].

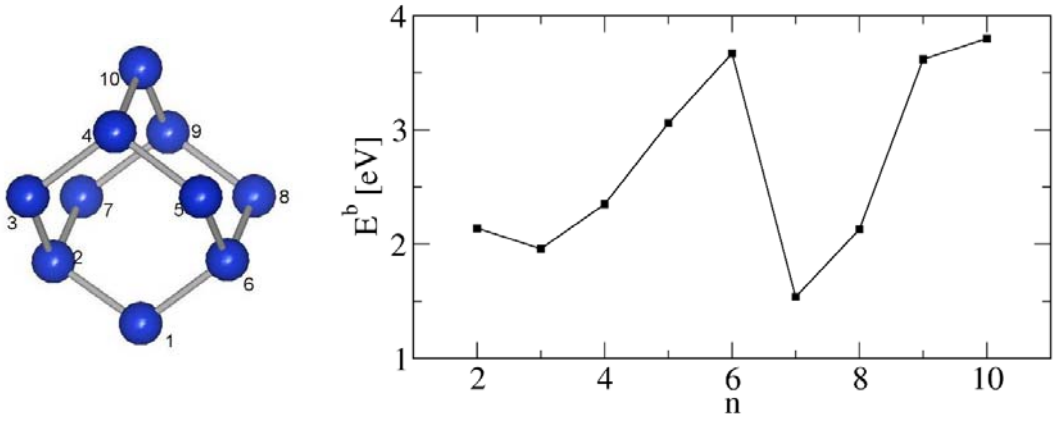

Figure 41: Vacancy cluster structures and the corresponding binding energies. The binding energy increases whenever the added V completes an additional hexagonal ring.

In the simulation, the following reactions are added to the default I cluster reactions:

$$V_n + V \leftrightarrow V_{n+1}, \quad V_n + I \leftrightarrow V_{n-1}, \quad I_n + V \leftrightarrow I_{n-1} \qquad \textbf{Eq. 1}$$

The corresponding reaction rate equations are given by

$$4\pi a_{V_n} D_V C_{V_n} C_V - k_r C_{V_{n+1}},$$

$$4\pi a_{V_n} D_I C_{V_n} C_I - k_r' C_{V_{n-1}},$$

$$4\pi a_{I_n} D_V C_{I_n} C_V - k_r' C_{I_{n-1}},$$

where a_{V_n} (a_{I_n}) is the capture radius of V_n (I_n), D_V (D_I) is the diffusivity of the vacancy (interstitial), C_{V_n} (C_{I_n}) is the V_n (I_n) concentration, and C_V (C_I) is the vacancy (interstitial) concentration. The reverse reaction coefficients are determined by the binding energies and Frenkel pair generation energies: $k_r = A\exp(-E_n^b / kT)$ and $k_r' = B\exp(-E_{FP}^f / kT)$, where A and B are calibration parameters. Considering nearly spherical shape of the voids, the V cluster capture radius was estimated to be $0.236n^{1/3}$ nm. In addition to the above reactions, the reaction $V_2 + BI \leftrightarrow BV$ is also included to enable interactions between vacancy clusters and mobile BI. The rate for this reaction is given by

$$4\pi a_{V_2} D_{BI} C_{V_2} C_{BI} - k_r' C_{BV}.$$

For V clustering reactions (Eq. 1), the binding energy was calculated using density functional theory (DFT) using the code VASP [34,35] with Eq. 2 and summarized in the Table 6.

$$E_{V_n}^b = E_{V_{n-1}}^f + E_V^f - E_{V_n}^f, \qquad \textbf{Eq. 2}$$

where $E_{V_n}^f = E_{V_n}^{Total} - \frac{(N_L - n)}{n} E_{Si}$ is the formation energy of the V_n cluster, $E_{V_n}^{Total}$ is the total energy of the supercell including the V_n cluster, N_L is the number of lattice sites in the supercell, and E_{Si} is the

energy of the perfect Si supercell. We used a 216 atom supercell with 2^3 *k*-points and a relatively high-energy cut-off of 340 eV.

V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}
2.14	1.96	2.35	3.06	3.67	1.54	2.13	3.62	3.80

Table 6: Vacancy cluster binding energies (eV)

6.2 Implanted V/I distributions

V/I distributions after Si co-implantation have been extensively investigated by Smith [30]. Based on his work, the initial V concentrations can be approximated by an analytic equation:

$$C_V = \frac{10^{21}}{x+0.1} \times \frac{co-implant\ dose}{7\times10^{14}}\ [cm^{-3}],$$

where x is the depth in nm. In our experiments, three different co-implant doses were used: 7×10^{14} cm^{-2}, 5×10^{14} cm^{-2}, and 3×10^{14} cm^{-2}. I concentrations are generated by scaling Smith's Monte Carlo result (Figure 5.2a in [30]) proportional to co-implant dose.

At high Si implant doses a buried amorphous layer is formed, as can be directly observed by TEM (Figure 42 top) and Rutherford back scattering (RBS) measurements. This amorphous layer regrows epitaxially upon annealing – the upper amorphous/crystalline (a/c) interface propagating downwards into the silicon and the lower a/c interface propagating upwards, until the two interfaces meet and form a sharp band of misfit defects mid-way between the initial a/c interface positions (Figure 42 bottom). As a result the generated V/I profiles inside the buried amorphous layer are eliminated, and the misfit defects evolve during annealing, partially blocking the outflow of interstitials to the surface.

In our present model the evolution of interstitials from the deeper part of the silicon is relatively unimportant and we have therefore chosen not to model the evolution of the misfit defect band in detail. Instead the blocking effect of the misfit defects is emulated by down-scaling the concentration of interstitial defects beyond the misfit band by a factor of ~0.15. Although RBS data indicates no buried amorphous layer for 3×10^{14} cm^{-2} dose co-implant, we find empirically that such scaling is still necessary to fit the diffused B profiles in the low-dose case. The initial V/I profiles used in this work are shown in Figure 43.

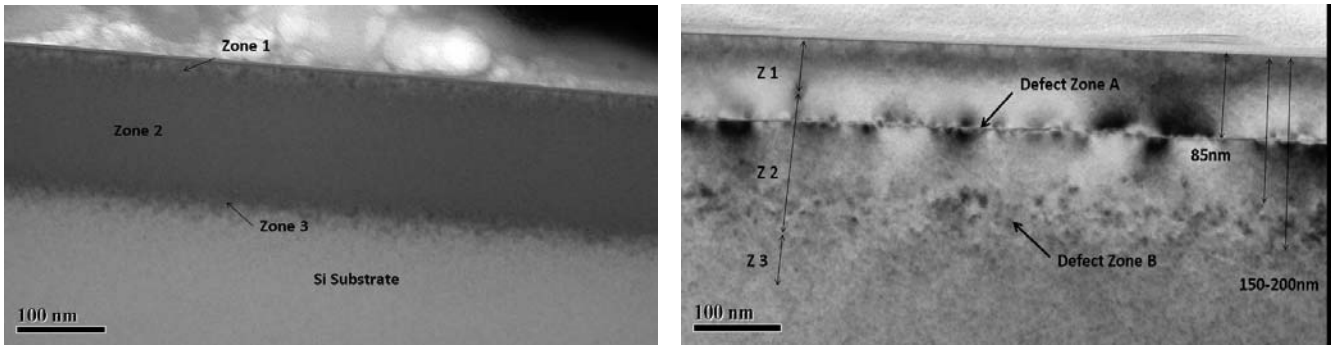

Figure 42: TEM cross-sectional images of samples implanted with 7×10^{14} cm^{-2} Si ions, before (left) and after (right) SPER for 100 s at 700 °C

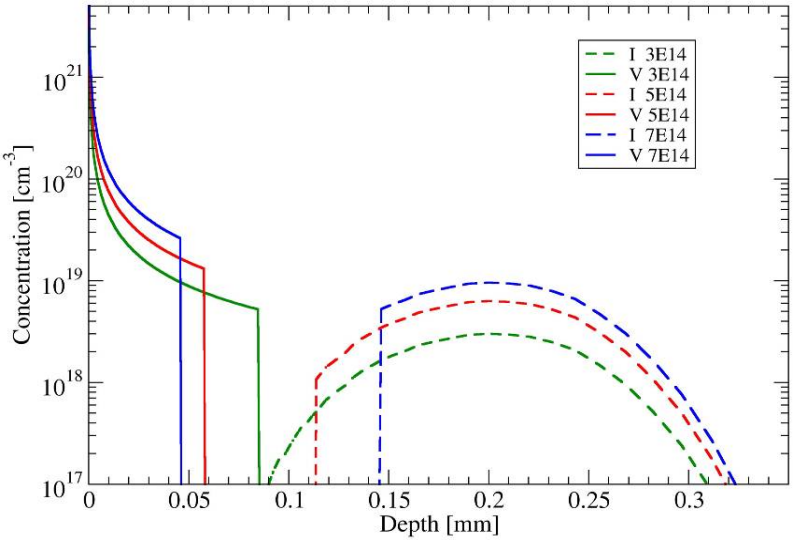

Figure 43: Initial excess I and V concentration profiles for the range of Si implantation doses considered in this study

6.3 B implant and initial conditions

Si co-implantation creates a high level of damage in the substrate, which reduces channelling during B implantation. To take this effect into account, as-implanted B profiles were read from SIMS data since the 'implant' command could not reproduce the trend with complete accuracy.

In our model, the first 3×10^{18} cm^{-3} B atoms in a given spatial volume are allocated at substitutional sites and the rest are placed at interstitial sites. All remaining (self) interstitials and vacancies are assumed to be fully recombined before diffusion process starts, leaving a net local excess of either vacancies or interstitials. Finally, substitutional B atoms at concentrations above a certain level are allocated as B_2 cluster, in order to avoid unphysically high activation near the surface. In amorphised or highly damaged samples, the clustering onset level (*AmInit*) is orders of magnitude higher than that in crystalline samples (*AcInit*). Combined with high level of V concentrations, the highly disordered structures observed by RBS measurement can justify our initial B and B_2 allocation. The initial dopant/defect distribution used for this modelling is illustrated in Figure 44.

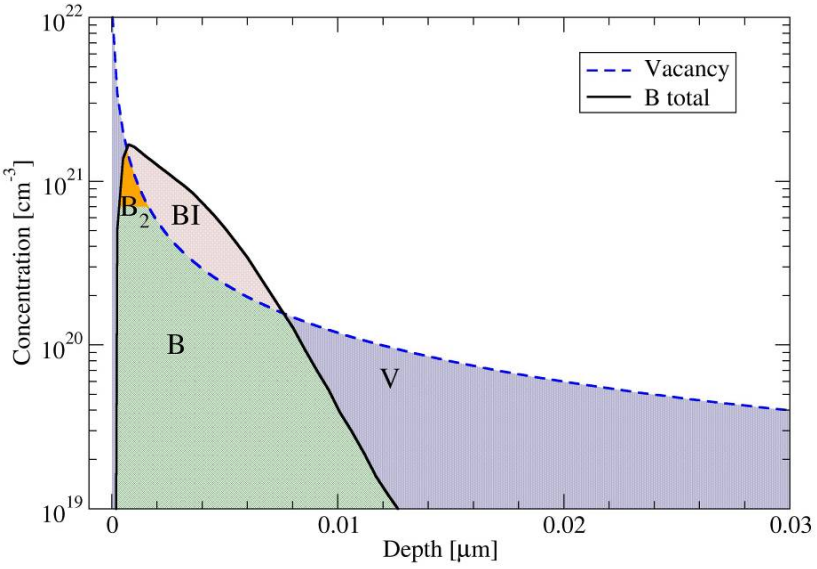

Figure 44: B distribution after implantation. The B_2 level varies depending on damage level and vacancy concentrations.

6.4 B diffusion

Numerous theoretical and experimental analyses have shown that B diffuses exclusively by an interstitial mechanism. To satisfy this, BV diffusion parameters are chosen to suppress vacancy-mediated diffusion almost completely. For the dominant interstitial component of B diffusion we used the BI diffusivity reported by Pichler [36]. The prefactors were modified to fit B profiles in control samples without co-implantation and the diffusivity used in the simulation is

$$D_{BI} = 0.123\exp(-3.566/kT) + 7\exp(-3.671/kT)\frac{p}{n_i} + 139.8\exp(-4.373/kT)\frac{p^2}{n_i^2}$$

$$D_{BV} = 0.00009\exp(-4.5/kT) + 0.00054\exp(-4.5/kT)\frac{p}{n_i}.$$

During B diffusion, excess B atoms above the activation limit tend to form boron interstitial clusters (BICs). In the simulation, this phenomenon was modelled using the *ChargedCluster* model in Sentaurus Process, which includes B_2, B_2I, B_2I_2, B_3I, B_3I_2 and B_3I_3. The formation energy of BICs was calibrated to fit the kink position of the diffused B profiles at 900 °C by varying the formation energy in proportion to the co-implant dose and the induced strains of the BICs within a range of 0.1 eV, to take into account stress-dependent BIC formation. This effect is important because, within the range of several nm from the surface where BIC formation is dominant, the high V concentration results in an internal tensile stress field which interacts with the induced strain due to BICs. The induced strains for the relevant BICs used in the simulation are listed in Table 7. Boron dose loss was also calibrated by adjusting the trap states at the oxide/silicon interface.

B	B_2	B_2I	B_2I_2	B_3I	B_3I_2	B_3I_3
-0.30	-0.44	-0.03	0.31	-0.29	0.12	0.19

Table 7: Induced strain due to BICs

6.5 Vacancy engineering: modelling results and discussion

The simulated profiles are compared with SIMS data in Figure 45. The most attractive feature of vacancy engineering, the high B activation, is well reproduced. The model shows that V clusters survive up to 800 °C annealing during the time range investigated in our study. Above this temperature V clusters rapidly dissociate, and thus vacancy engineering is most effective at 800 °C and below. In this temperature range, our model predicts the observed incremental trend of the kink concentration at 800 °C and below. Interestingly, our model reproduces the fast rising B active profiles above the solubility limit near the surface, reported experimentally by Smith [30]. This feature originates from the initial recombination between vacancies and BI.

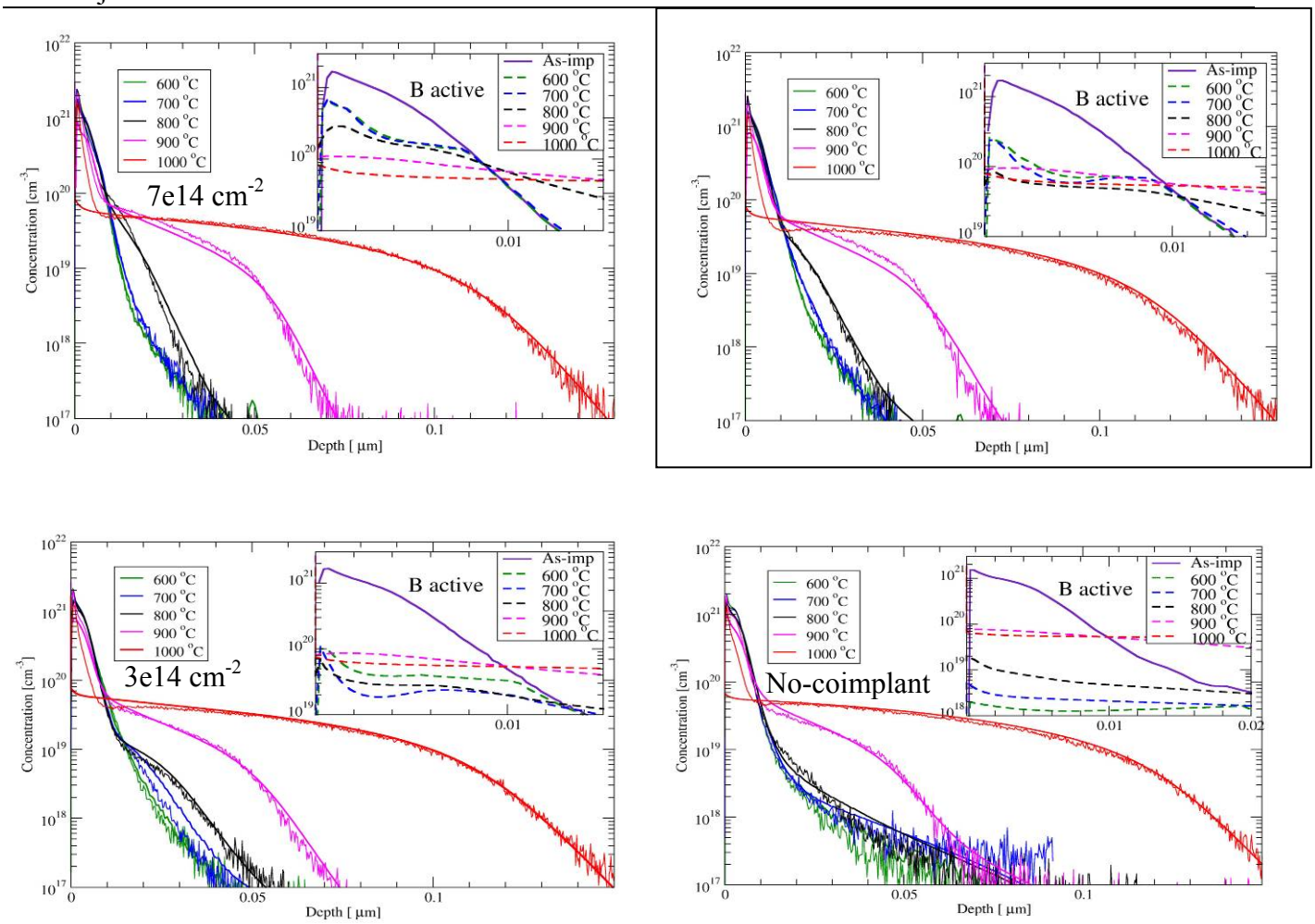

Figure 45: Simulated total B profile and its comparison to SIMS data for different co-implant doses. Inset shows the active B profiles near the surface.

The importance of modelling V cluster evolution is illustrated in Figure 46, where we present modelling results with and without the inclusion of V clusters. In the absence of V clusters, the effect of the initially implanted vacancies rapidly disappears, so that an initial high level of activation rapidly collapses, leading to a high concentration of clustered B after annealing at low temperature. The effect persists up to temperatures in the range 800-900°C, where V clusters dissolve significantly and the activation level approaches thermodynamic equilibrium.

Figure 47 shows a comparison between modelled sheet activation and experimental measurements obtained by the Hall method. Although agreement is not perfect the trend of the data is well described – particularly the slight deactivation which occurs during V cluster ripening and the recovery of activation arising from the diffusion of B into the wafer accompanied by BIC dissolution. Taking together the rather accurate modelling of B diffusion profiles and the reasonable estimates obtained for the corresponding time-dependent activation, the model provides a useful predictive approach to the modelling of vacancy engineering.

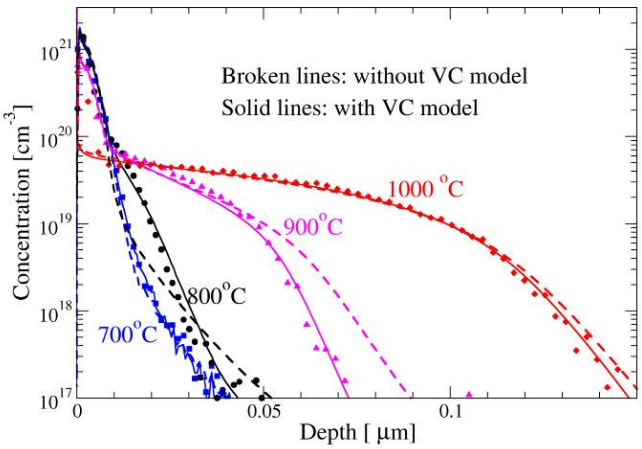

Figure 46: Simulation results with (solid lines) and without (broken lines) the use of the vacancy cluster model. Symbols represent SIMS data. Activation at low temperature is strongly underestimated, and diffusion is overestimated, when V clusters are not modelled

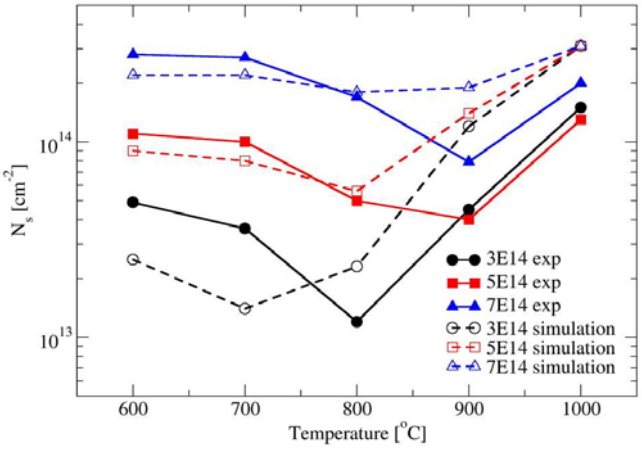

Figure 47: Comparison of active sheet doping data from Hall measurements with simulations using the V cluster model.

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7 Overlayer stress effects on doping processes in Si and Ge

Stress influences point defect generation, dopant diffusion and activation during nanoelectronic device processing. In current TCAD models such effects occur through direct effects of bulk stress within the semiconductor. However, a theoretical paper in 2007 showed that, even in the absence of significant stresses in the semiconductor, stresses in overlying layers can influence point defect formation and thus diffusion in the semiconductor [37]. The effect arises through the generation of a point-defect supersaturation at the interface between the stressed overlayer and the semiconductor. Point defect concentrations in the semiconductor are modified as the semiconductor/overlayer system moves to reduce strain energy in the overlayer, leading to a supersaturation at the position $\underline{r_0}$ where the point defect is generated,

$$S(\underline{r_0}) = \exp(\sigma(\underline{r_0}).\boldsymbol{V_f}/kT$$

where $\sigma(\underline{r_0})$ is the stress in the overlayer immediately overlying the generation point, and $\boldsymbol{V_f}$ is the formation volume of the point defect, equal to one atomic volume of the semiconductor lattice.

In ATOMICS we have conducted experiments to test this idea. First we look at previously published work relating to the effects of stress in overlayers. Zaitsu *et al*. [38] explored the effect of tensile strained nitride overlayers on the diffusion of implanted B in a silicon substrate during furnace annealing. B diffusion was found to be strongly retarded at low diffusion temperatures, but relatively weakly retarded at high temperatures, apparently suggesting a large change in diffusion prefactor and activation energy as a function of stress. It was suggested that the effect might be a result of stress induced in the silicon substrate, however the calculated stress values, in the range of MPa, are much smaller than the range (>300 MPa) normally expected to produce significant effects on diffusion.

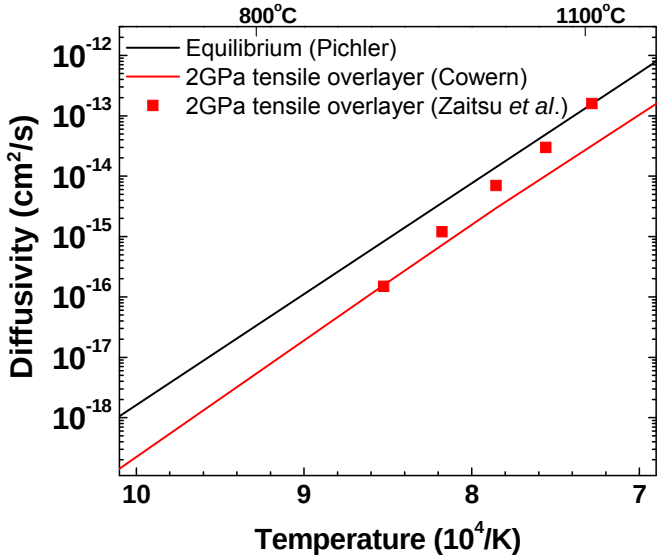

Figure 48: Arrhenius plot showing the equilibrium diffusivity estimated by Pichler [39], a theoretical prediction based on Ref. [37], and the experimental results of Zaitsu et al. [38]

Figure 48 shows a comparison between the data of Ref. 38 and theory [37]. The theoretical values are based on ~2 GPa stress in the nitride as quoted in Ref. 38. Theory and experiment agree well at low temperatures but disagree at high temperature, where the diffusivity under nitride converges towards equilibrium values. Various explanations for this are possible – e.g. an interfacial oxide layer might form during the long thermal anneals used in their work, or the nitride/silicon interface might begin to relax, altering the interface chemistry or reducing the effective level of strain that controls the interstitial formation energy. To resolve these issues we performed experiments at lower thermal budgets to minimize interfacial changes during annealing.

A good way to conduct such experiments is to use epitaxial silicon containing narrow dopant markers, enabling detection of small amounts of diffusion during low thermal-budget anneals that do not cause relaxation of the nitride/silicon interface.

7.1 Experiments

Experiments were devised to test the effects of strained overlayers on B marker layer diffusion in Si. Test structures were created using two identical Si wafers on which Si epitaxial layers were grown by chemical vapour deposition (CVD). The one micron-thick CVD layer contained three B marker layers incorporated with a spacing of about 300nm, to study their diffusion and check for any depth-dependent effects. The first of these wafers was kept as a reference sample. A tensile strained silicon nitride layer of approximately 100 nm thickness, with negligible hydrogen content and a strain of approximately +960 MPa, was deposited on the second wafer. The wafers were diced into a set of samples which were annealed in nitrogen ambient in the 700-1100°C temperature range, at 50°C intervals, and in the 10-7200s time range at regular (logarithmic) intervals, using a Mattson 3000 Plus annealing system. After annealing, overlayers were removed from the samples in preparation for boron depth

profile measurements using the secondary-ion mass spectrometry (SIMS) technique.

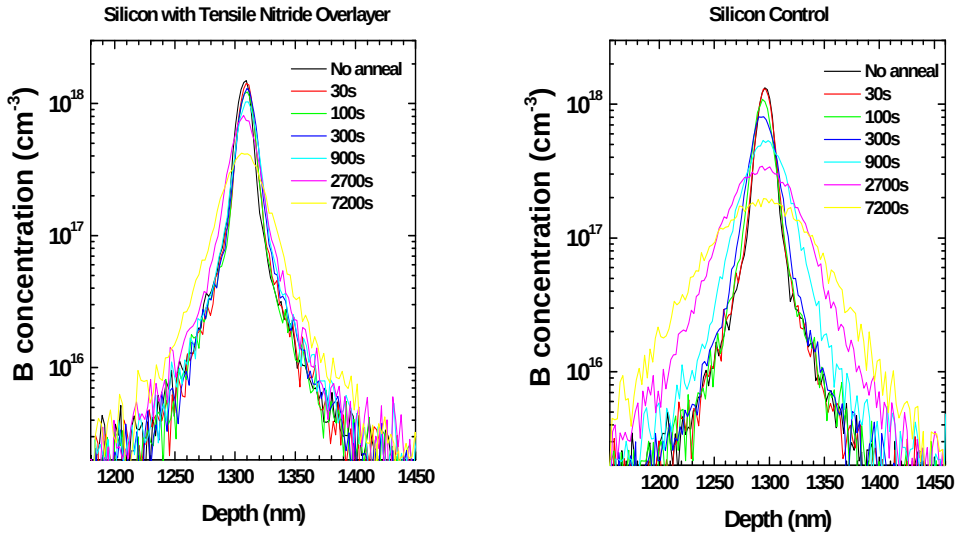

Figure 49: SIMS profiles showing B diffusion in Si at 900oC for various annealing times. In (a) diffusion is retarded by the tensile overlayer relative to (b), equilibrium diffusion.

7.2 Experimental results and analysis

Figure 49 shows an example of SIMS profiles through the deepest of the three B marker layers following 900°C annealing for a series of different times. In the upper plot of Figure 49, diffusion is clearly retarded by the presence of the tensile nitride overlayer relative to the lower plot, the case where no overlayer is present.

SIMS measurements were carried out for samples covering the full annealing matrix for both the nitride covered wafer and the control wafer.

Information from the SIMS profiles was used to extract B diffusivity information. By extracting the diffusivity for samples with overlayers, relative to the diffusivity in control samples, we obtain an effective diffusion 'supersaturation' factor, as outlined for example in Refs. [40,41]. The supersaturation is extracted as follows for each annealing condition: The as-grown SIMS profile is convolved with the 'universal function' for intrinsic B diffusion described in [42] and fitted to the measured diffused profile to extract the diffusive broadening. The average diffusivity over the increment of annealing time between successive thermal anneals is obtained from the relations in [43], and finally a supersaturation is extracted from the ratio of the experimental diffusivity and that from the equilibrium regression curve of Pichler [39].

Convolution and diffusivity extraction is carried out using a nonlinear least-squares fitting program that models the amount of profile broadening as a function of the interstitial supersaturation. Firstly fitting was carried out using a single fitting function to simultaneously fit all three marker layers. Subsequently additional fitting was carried out to fit each peak individually to check for consistency in the diffusion of all three markers. This analysis was performed for all temperatures and times investigated in this work and showed that the diffusion in all three markers was the same within errors, thus eliminating the possibility of systematic error in determining the supersaturation created by the presence of the overlayer..

At 900°C the analysis yields supersaturation values of $0.855D_0$ in the control samples and $0.114D_0$ in samples with tensile strained nitride overlayer, thus almost a 10× reduction in diffusion under the strained overlayer. The supersaturation is also extracted for annealing temperatures in the range from 750 to 1100°C, using the same approach.

Before presenting and interpreting the full set of temperature dependent results we first estimate the stress in the nitride layer during annealing. This will allow an approximate estimate of the expected supersaturation of interstitials for comparison with our actual diffusion data. The stress at the diffusion temperature is determined by several factors:

(i) the 'intrinsic stress' present after initial growth of the samples

(ii) the differential expansion of the nitride layer with respect to the silicon substrate, arising from the increase in temperature from initial room temperature to the annealing temperature

(iii) structural or compositional changes potentially causing variations in stress, elasticity and/or expansion coefficient, during the annealing process.

In nitride films with a substantial H content, the third factor tends to be dominant as discussed in detail by Hughey and Cook [44] and by Saito *et al.* [45]. The key effect for such films is the evolution of H and consequent densification of the films during annealing. However, in the present samples H content is low and we expect that only the first two factors – intrinsic stress and differential thermal expansion – are significant.

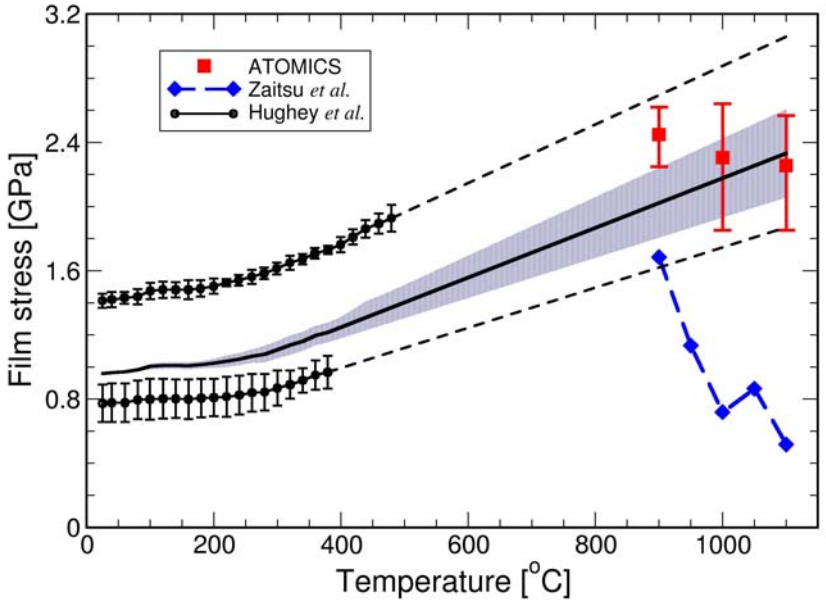

Figure 50: Temperature dependent stress curves for PECVD nitride films with three values of intrinsic stress. Open symbols: data from Ref. 44 for films with two different values of intrinsic stress. Dashed curves: high temperature extrapolations from the data of Ref. 44. Solid curve: interpolation to obtain the stress curve for this study, which used films with an intrinsic stress of 0.96 GPa. The shaded area indicates the range of results using different interpolation approaches, as explained in the text. Symbols labelled 'ATOMICS' and 'Zaitsu et al.' in the legend are stresses inferred from interstitial supersaturation data taken from this work, and from Ref. 38, respectively.

Published experimental data showing the increase in PECVD nitride stress as a function of temperature, based on two different intrinsic stress values [44], are presented in Figure 50. The data were obtained during cooling from higher temperatures at which H had been purged from the films, the intrinsic stress value being the stress reached when the samples cooled to room temperature. Curves are drawn through the data and extrapolated to obtain approximate estimates of expected stresses at higher temperatures, assuming no further evolution of hydrogen. The solid curve, starting from an intrinsic stress of 0.96 GPa, is an estimate of the temperature dependence for the hydrogen-free films used in our study, obtained by interpolating between the above curves. The upper limit of the shaded area corresponds to adopting the temperature dependence of the upper set of data from Ref. 44 and shifting the curve

downward to match the intrinsic stress of 0.96 GPa in our experiment. The lower limit corresponds to adopting the temperature dependence of the lower data set.

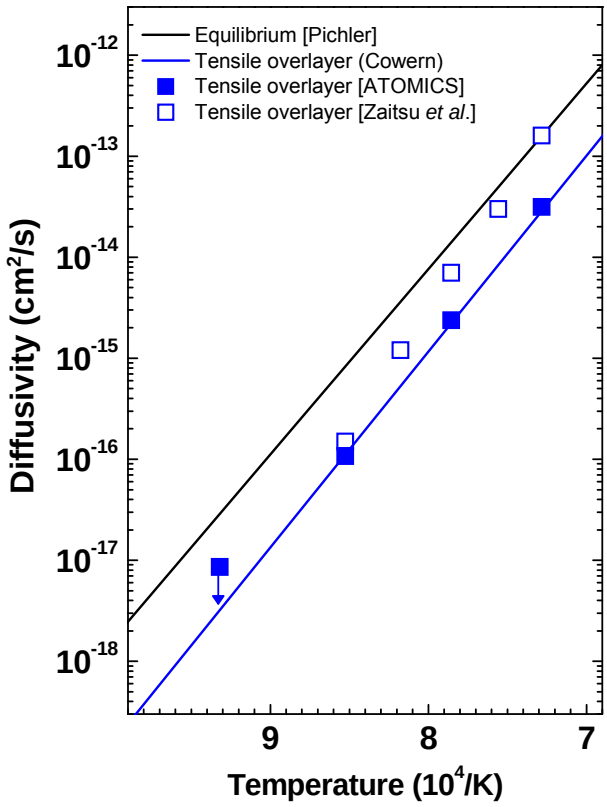

Figure 51: Comparison of measured diffusivities with theory. Upper line: Pichler's estimate of the equilibrium diffusivity of B in Si [39]. Lower line: calculated diffusivity under tensile strained nitride, assuming a strain value of 2.4 GPa. Open symbols: experimental data of Zaitsu et al [38]. Solid symbols: experimental data from this work.

7.3 Discussion

It is interesting to compare results from the present study with those from the experiment of Zaitsu *et al*. [38], both shown in Figure 51. Our results give lower supersaturations (i.e. a stronger undersaturation) than was found in Ref. 38, and this trend gains strength towards higher temperature. Moreover, the results of Zaitsu *et al*. show a very large difference in diffusion activation energy between nitride covered samples and control samples, whereas we find an activation energy only slightly different from that in control samples.. A likely explanation for this disagreement is that the interface partially relaxes during the long anneals used in the work of Zaitsu *et al*., whereas such relaxation is much reduced under the lower thermal-budget conditions used in our study. This explanation in terms of interface relaxation seems plausible because the temperature range of both Zaitsu *et al*'s and our experiments is at the top end of the elasticity regime for silicon nitride, approaching the temperature range at which crystallisation begins to occur [46]. However, our results at 900°C show no significant changes in supersaturation over the time scale from 30s to 7200s, indicating that the interface does not significantly change its effect on the supersaturation during this range of annealing times at this temperature.

The experimental results in Figure 51 are also compared with theoretical estimates based on the theory developed in Ref. 37, assuming a nitride stress value of 2.4 GPa during the anneals used in this study. The curve is in good agreement with our experimental observations, and the assumed stress value agrees quite well with the expected values for 900-1100°C shown in Figure 50.

Finally, it is interesting to estimate the strain values needed, according to the theory, to explain the undersaturations observed in our experiment ('ATOMICS') and those reported by Zaitsu *et al*. These are shown in Figure 50 along with the estimated temperature dependent stress values for our nitride films. The results are consistent with each other within the experimental uncertainties. This outcome is consistent with the view that our nitride films did not significantly relax during the low thermal budget anneals used in our experiment. It also provides strong support for the theoretically predicted effect of overlayer stress on diffusion.

Stressed overlayers may have a range of interesting applications in the field of point-defect engineering. One case of particular interest is the control of dopant diffusion and activation in Ge. In that system almost all common dopant impurities, with the exception of B, tend to diffuse with, and form clusters with, vacancies [47,48]. By applying a compressively strained overlayer the energy cost of vacancy formation may be increased, giving rise to an undersaturation of vacancies, thereby retarding diffusion and also potentially enhancing the level of dopant activation. This would be a significant advantage for n-type dopants in Ge, most of which are relatively fast diffusers, and all of which have relatively low electrical solubility as a result of dopant-vacancy cluster formation. Engineering such an effect in the case of Ge may be difficult since the deformation stress for Ge is relatively low, however the use of suitably thin compressive films may provide a solution.

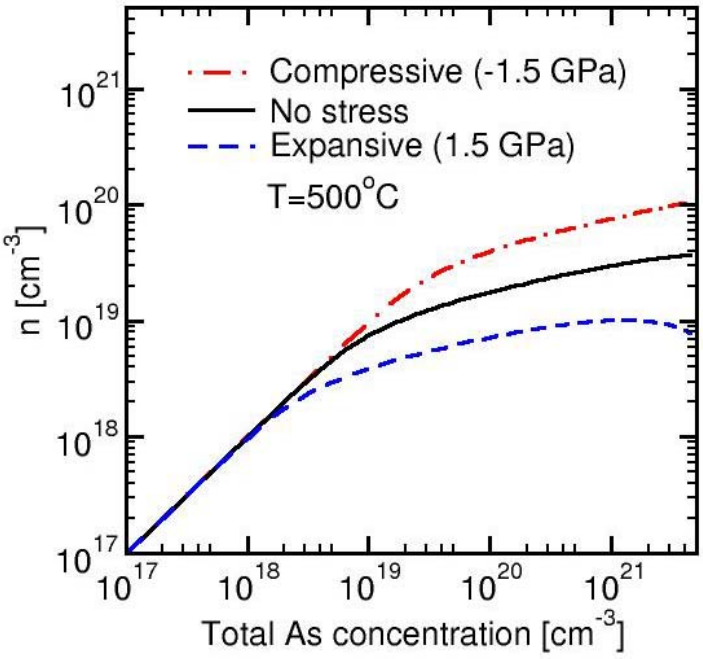

Figure 52: Calculated impact of overlayer stress on equilibrium As activation in Ge, plotted as a function of total As concentration.

As illustration, Figure 52 shows the predicted impact of overlayer stress on the equilibrium activation level of As in Ge. The effect on As activation was calculated using similar methods to those described in Ref. [49]. However, in contrast to Ref. [49], the As_nV formation energy is modified by a term $\sigma(r_0).V_f$ due to the strained overlayer. This leads to a change in activation level by a factor of 3-4 as a result of 1.5 GPa stress in the overlayer. While it is difficult to predict accurately the absolute activation level, the substantial effect of stress on activation shows the potential for the use of strained overlayers for engineering improved doping properties in Ge.

7.4 Conclusion

The effect of tensile strained nitride overlayers on the supersaturation of interstitial point defects in silicon has been investigated experimentally. The results presented in this work support recent theoretical predictions on the effect of overlayer stress on point defect supersaturations and impurity diffusion. Consequently the phenomenon has potential for controlling point defect concentrations in semiconductor materials – for example controlling the negative effects of vacancy-type defects on doping in germanium. It may also provide a much needed method of manipulating point-defect concentrations in studies aimed at understanding diffusion and activation mechanisms in Ge. This report reproduces part of a paper presented at the European Materials Research Society Spring Meeting 2009.

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8 Stress and Ge composition effects on dopant activation

Early theoretical work on the impact of stress on dopant solubility in Si and SiGe shows inconsistency or lack of general validity [50, 51, 52, 53, 54]. In the ATOMICS project, we developed a generalized theoretical model for the equilibrium (or surface controlled) dopant solubility [55], which was also extended to be applied to the non-equilibrium (or bulk-controlled) system. To describe the systems at non-equilibrium correctly, the net changes of the induced strain in each reaction equation (dissociation rate factor), the stress dependent microscopic diffusivity of dopant-defect pair (forward reaction rate factor), and stress dependent $D_I C_I$ or $D_V C_V$ should be considered. For the B activation model, comprehensive induced strain data for various structures including BICs and B-defect pairs is presented for the first time. Induced strains of various dopant-defect pairs at transition states are also reported, which can be used to simulate the stress effects on diffusion of common dopants in Si. Based on the induced strains, we present suggested model parameters for Sprocess implementations. The observed negligible Ge composition effects on B activation were also explained using ab-initio calculations.

8.1 Stress effects on dopants solubility

Stress effects on dopants solubility were modeled based on the induced strains due to dopants generated by ab-initio calculations. The model equation is given by

$$\frac{C_{SS}(\vec{\sigma})}{C_{SS}(0)} = \exp\left(-\frac{\Delta E^f(\vec{\sigma})}{kT}\right),$$

$$\Delta E^f(\vec{\sigma}) = -V_0 \Delta\vec{\varepsilon}\cdot\vec{\sigma},$$

where V_0 is a lattice site volume, $\Delta\vec{\varepsilon} = (\Delta\varepsilon, \Delta\varepsilon, \Delta\varepsilon)$ is the induced strain, and $\vec{\sigma}$ is the stress. The induced strain is equivalent to the volume expansion coefficient (β) via $\Delta\varepsilon = 3\beta \times 5 \times 10^{22}$, and also can be measured X-ray. Table 8 lists the induced strain due to various dopants.

Table 8: Induced strains due to dopants at substitutional sites.

	B	Ga	In	P	As	Sb	Bi
Ab-initio	-0.30	0.066	0.21	-0.084	0.013	0.16	0.23
Experiment	-0.315 [Ref. 56]			-0.095 [Ref. 57]	-0.02 [Ref. 58]		

The equilibrium solubility equations are applicable to the systems where the dopant activation is surface- or interface- controlled (e.g, solid phase epitaxial regrowth). In this case, the formation energy of dopants in reservoir or dopant source is nearly stress independent and thus the formation energy of substitutional dopant is deterministic. In bulk controlled systems, point defects are super/under saturated and drive the formation/dissociation of dopant-defect clusters. This introduces an additional term $\Delta\mu(\vec{\varepsilon})$, which is the change in the formation energy of dopants in clusters and is negligible for the surface-controlled case. Especially for B, $\Delta\mu(\vec{\varepsilon})$ is important because diverse boron interstitial clusters form during annealing. For the transient model in Sprocess, $\Delta\mu^{eff}(\sigma) = -V_0 \Delta\vec{\varepsilon}_{BIC}^{eff} \cdot \vec{\sigma}$ may be estimated to represent the averaged stress effects on the cluster formation where $\Delta\vec{\varepsilon}_{BIC}^{eff}$ is the effective induced strain due to BICs and the point defect supersaturation. Although determining $\Delta\vec{\varepsilon}_{BIC}^{eff}$ requires extensive sample data and calibration work, Figure 53 can provide a good guidance for estimating the values in a given system.

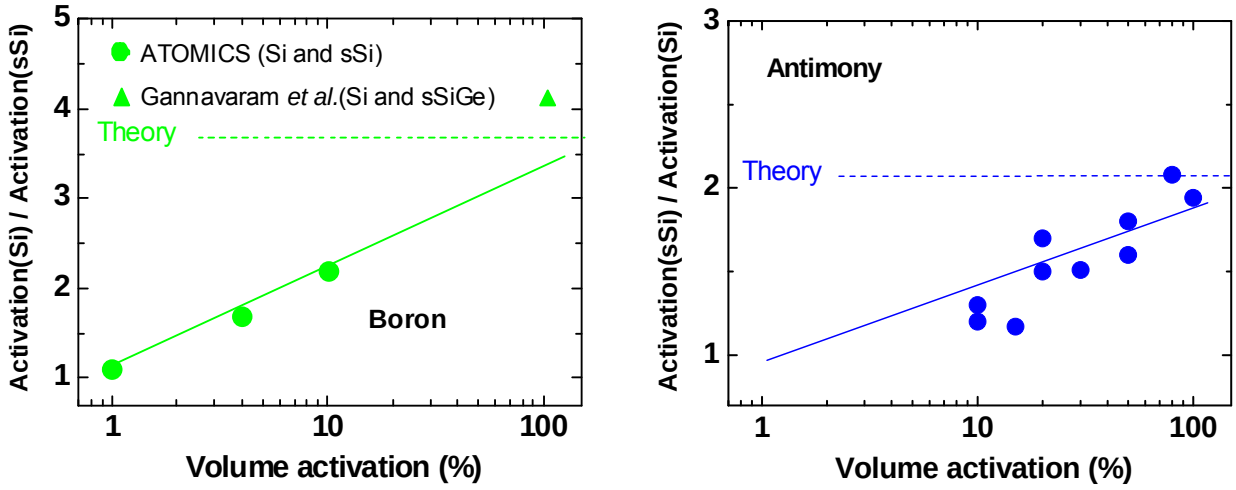

Figure 53. Activation enhancement factor plotted as a function of volume activation in the peak of the doping profile for (left) B and (right) Sb (Gannavaram et al., Ref. [59]).

Sprocess model calibration has not yet been done, but the solubility factor can be modified as

$$\frac{C_{SS}(\vec{\sigma})}{C_{SS}(0)} = \exp\left(-\frac{\Delta E^f(\vec{\sigma}) - \Delta\mu_{BIC}^{eff}(\vec{\sigma})}{kT}\right) = \exp\left(\frac{V_0(\Delta\vec{\varepsilon} - \Delta\vec{\varepsilon}_{BIC}^{eff}) \cdot \vec{\sigma}}{kT}\right),$$

where $\Delta\vec{\varepsilon}_{BIC}^{eff}$ needs to be calibrated appropriately.

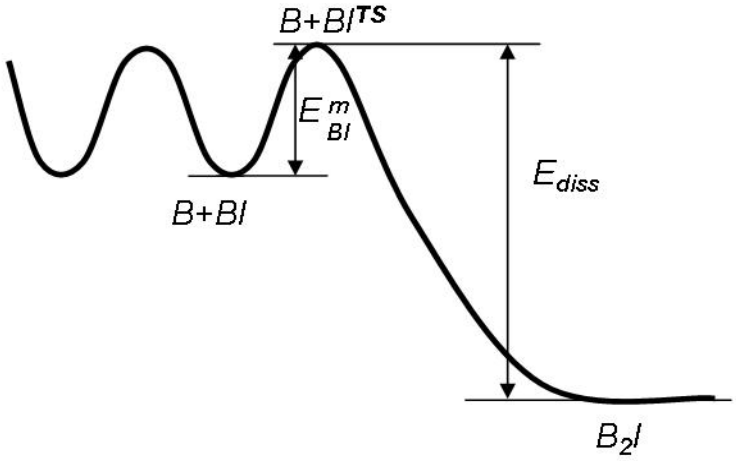

Figure 54: Schematic energy diagram for B+BI ↔B_2I. E_{BI}^{m} determines the forward rate and E_{diss} the reverse rate, which are stress dependent. The superscript TS refers to the transition state between B+BI and B_2I.

For the charged cluster model, individual BIC reactions are taken into account. As a model example, for the reaction B+BI <->B_2I, the forward reaction rate should be modified by adjusting the BI diffusivity (BorontIntDiffFactor) and the reverse rate should be modified by the cluster dissociation factor (B2IDissFactor for the given reaction). The forward rate is modified by the change in the migration barrier, which is $\exp(V_0(\Delta\vec{\varepsilon}_{BI^{TS}} - \Delta\vec{\varepsilon}_{BI})\cdot\vec{\sigma}/kT)$. The BI diffusivity stress factor is different from the equilibrium diffusivity factor which includes the stress effect on BI formation. The equilibrium diffusivity factor is explained in the next section (Stress effects on dopant diffusion). The dissociation stress factor is given by

$$\frac{k^r_{B_2I}(\vec{\sigma})}{k^r_{B_2I}(0)} = \exp\left(\frac{V_0(\Delta\vec{\varepsilon} + \Delta\vec{\varepsilon}^{TS}_{BI} - \Delta\vec{\varepsilon}_{B_2I})\cdot\vec{\sigma}}{kT}\right),$$

where $\Delta\vec{\varepsilon}^{TS}_{BI}$ is the induced strain due to BI at the transition state of which numerical value is presented in Table 11. When biaxial stress is applied, the corresponding Sprocess parameters can be defined as

term name=BoronIntDiffFactor store add Si eqn = "exp($Vti*(StressKK_y/10.0)*2.8e-11)"

term name=B2IDissFactor Si eqn = "exp(($\Delta\varepsilon_{B_2I} - \Delta\varepsilon - \Delta\varepsilon^{TS}_{BI}$)*2*1.27e-10*[simDelayDouble Diffuse Vti]*(StressKK_y/10))"

For accurate calculations, $\Delta\vec{\varepsilon}^{TS}_{BI}$ should be treated as a tensor, but averaging diagonal elements will also give reasonable results. In addition, D_IC_I is also changed by the external stress.

$$\frac{D_IC_I(\vec{\sigma})}{D_IC_I(0)} = \exp\left(\frac{V_0\Delta\vec{\varepsilon}^{TS}_{I}\cdot\vec{\sigma}}{kT}\right),$$

where $\Delta\vec{\varepsilon}^{TS}_{I}$ is the induced strain due to self-interstitial at the transition state. In a similar way, D_VC_V can be modified. The stress dependent D_IC_I and D_VC_V factor will be included in the next release of Sprocess.

Table 9: Induced strain due to B and B-defect pairs. Note that the value of BI^{TS} is an average of the three components listed in Table 11. These results have not yet been applied to model the activation data shown in Figure 53 above.

	B	BI	BI^{TS}	BV	B_2	B_2I	B_2I_2	B_3I	B_3I_2	B_3I_3
$\Delta\varepsilon$	-0.30	-0.09	0.073	-0.36	-0.44	-0.03	0.31	-0.29	0.12	0.19

8.2 Ge composition effects on B solubility

The solubility of B in strained-SiGe was compared with that in relaxed-SiGe. Negligible composition effects were found from the comparison, which is also supported by ab-initio calculations showing B-Ge binding energy is less than 15 meV. Therefore no corresponding Sprocess modelling has been done.

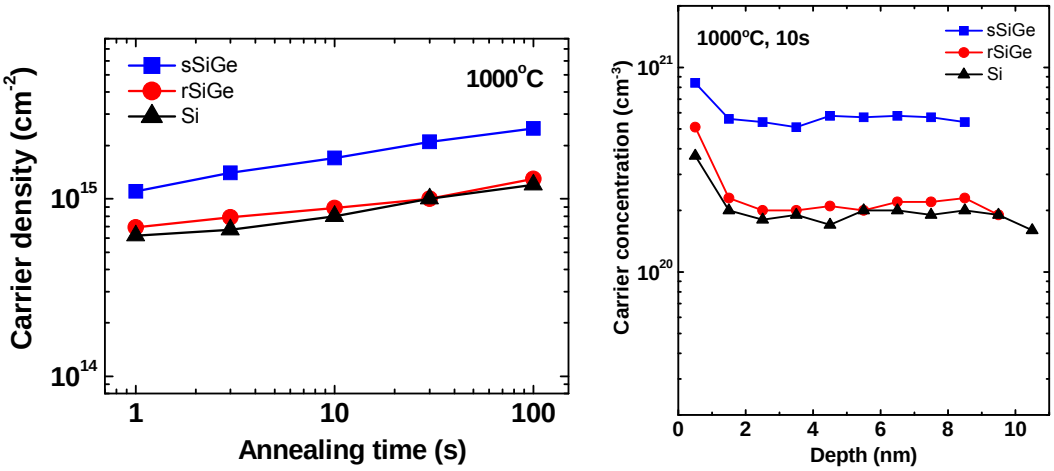

Figure 55: Comparison of dopant activation as a function of annealing time for B-doped Si, relaxed $Si_{0.8}Ge_{0.2}$ (SiGe) and strained $Si_{0.8}Ge_{0.2}$ (sSiGe) measured using the Hall effect. Right: Volume B activation in Si, SiGe and sSiGe using the differential Hall technique.

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9 Stress and Ge composition effects on dopant diffusion

The impact of stress and composition on the equilibrium dopant diffusivity has been investigated by many authors both experimentally [60,61,62,63,64] and theoretically [65,66,67,68]. Although there is a consensus for the general trend of combined effects, the relative strength between stress and composition effect is not agreeable. Among many theoretical calculations, Diebel's method has an advantage in that it provides the induced strain tensor that can be used for arbitrary stress conditions [66]. Ahn et al. expanded the Diebel's method to predict Ge composition effects using extensive ab-initio calculations and KLMC and concluded stronger stress effects than composition effects. Ahn's model prediction for the overall B diffusion in strained SiGe shows good agreement with Moriya et al. [62] and Fang et al [63]. However, other results do not agree with the theoretical prediction. Among many factors (e.g., doping concentrations, layer structure and the quality of samples), the doping concentration seems to cause the discrepancy. Although Kuo et al.[60], and Zangenberg et al[61]. assumed that the initial concentrations were below the intrinsic carrier concentration, they were comparable to the intrinsic carrier concentration as shown in Figure 56 (Ref. [69]). At this intermediate doping concentration, the Fermi level effect is expected at the early stage of the diffusion process, which in turn makes the bandgap narrowing effect play an important role and analysis complicated. The bandgap narrowing can explain the weaker tensile stress effect than compressive stress effect observed

by Kuo et al. and Portavoce et al.[64] In the Fermi level dependent diffusivity term $\frac{p}{n_i}D^+$, n_i increases under both types of strain, while the activation energy of D^+ increases (decreases) under compressive (tensile) strain. Therefore, the bandgap narrowing somewhat compensates the effect from the lowered activation energy for the tensile case. In the experiment by Portavoce et al., much higher doping concentration was used without the correction to get the intrinsic diffusivity and thus their diffusivity in the unstrained sample was considerably different from others.

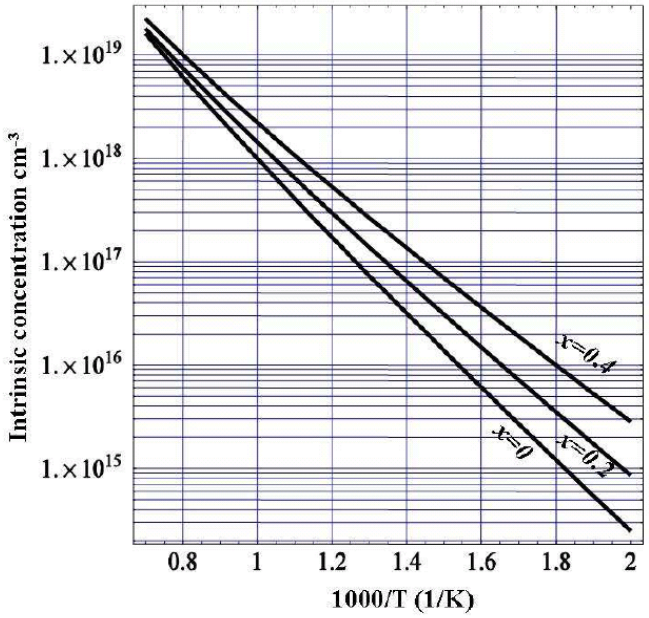

Figure 56: Intrinsic carrier concentration in strained $Si_{1-x}Ge_x$.

Table **10** summarizes the experimental conditions and the results of previous experiments. To separate the individual effects mentioned above, a more careful experimental set up or more comprehensive process simulation is required. In the ATOMICS project, Sprocess simulations were performed to include the high concentration effects and the bandgap narrowing effect based on ab-initio calculations, as well as smaller but still significant defect coupling effects on B diffusion.

Table 10: Summary of previous experiments on the impact of stress and Ge composition on B diffusivity.

	Moriya	Fang	Kuo	Zangenberg	Portavoce
Diffusion layer thickness (nm)	15	20-60	60	155	100
Ge fraction	0.1-0.5	0.2	0.1-0.2	0.12-0.24	0.09-0.18
Critical epi-layer thickness (nm) [Ref. 16]	30-4	13	20-13	26-10	32-14
Peak concentration	$>1.5\times10^{19}$	$\sim1\times10^{18}$	$\sim2\times10^{18}$	$\sim3\times10^{18}$	$\sim2\times10^{19}$
Temperature (^{o}C)	975	850	800	800-925	900
Capping layer	50 nm Si	120 nm Si	40 nm $Si_{1-y}Ge_y$	100 nm SiO_2 and Si_2N_3 on top of 100 nm $Si_{1-y}Ge_y$	20 nm Si only for compressive
Stress effects: comparison to theoretical model O: good, Δ: comparable but some data are off the trend, X: generally off					
compressive strain	O	O	Δ	Δ	X(stronger)
Tensile strain			X (weaker)	Δ	Δ
Comments	Extrinsic doping, correction applied to get intrinsic diffusivity	Intrinsic doping	Intermediate doping	Intermediate doping	Extrinsic doping, no correction for the intrinsic value

9.1 Stress effects

Stress effect on dopant (A) diffusivity can be modeled in a similar way to that on dopant solubility, but at equilibrium without significant BICs the description becomes simpler. The diffusivity factor becomes

$$\frac{D_{AX}^{eff}(\vec{\sigma})}{D_{AX}^{eff}(0)} = \exp\left(-\frac{\Delta E_{AX^{TS}}^{f}(\vec{\sigma})}{kT}\right),$$

$$\Delta E_{AX^{TS}}^{f}(\vec{\sigma}) = -V_0(\Delta\vec{\varepsilon}_{AX}^{TS} - \Delta\vec{\varepsilon}_{A})\cdot\vec{\sigma},$$

where the key parameter $\Delta\vec{\varepsilon}_{AX}^{TS} = (\Delta\varepsilon_x^{TS}, \Delta\varepsilon_y^{TS}, \Delta\varepsilon_z^{TS})$, which is the induced strain due to the dopant-defect pair (AX) at the transition state. $\Delta\vec{\varepsilon}_{A}$ is the induced strain due to dopant A at the substitutional site (Table 8). Since the transition state is not always symmetric, the three components of $\Delta\vec{\varepsilon}_{AX}^{TS}$ can be different, which results in anisotropic diffusion under biaxial or uniaxial stress conditions. Table 11 lists the induced strains of AX pairs at their transition states.

Table 11: The induced strains due to B, P, As and Sb dopant-defect pairs at the transition state. Note that P diffusion path requires two distinct transition states for long range diffusion and the difference $\Delta\vec{\varepsilon}_{AV}^{TS} - \Delta\vec{\varepsilon}_{A}$ is very similar despite the large difference in the induced strain of vacancy transition states.

	Si	B	P	As	Sb
$\Delta\vec{\varepsilon}_{AI}^{TS}$	(0.54, 0.026, 0.11)	(0.29,-0.036, 0.036)	(-0.05, 0.05, 1.0) (0.27, 0.27, 0.25)	(0.31, 0.31,0.31)	
$\Delta\vec{\varepsilon}_{AV}^{TS}$	-(0.42, 0.42, 0.42)		-(0.42,0.42,0.42)	-(0.38, 0.38, 0.38)	-(0.23, 0.23, 0.23)

In a biaxially strained layer, B diffusion is anisotropic due to the asymmetric induced strain at the transition state. In Ref. [66], the detailed calculation is provided. Considering all possible 72 hopping directions, analytic calculations were performed and the result was approximated to a single Arrhenius curve.

$$\frac{D_{BI}^{eff}(\sigma)}{D_{BI}^{eff}(0)} = \exp\left(\frac{8.2\times10^{-11}\sigma}{kT}\right) \text{ - out-of-plane}$$

$$\frac{D_{BI}^{eff}(\sigma)}{D_{BI}^{eff}(0)} = \exp\left(\frac{1.1\times10^{-10}\sigma}{kT}\right) \text{ in-plane.}$$

The equations above include overall effects and thus are useful to predict the effective diffusivity experimentally observed. In Sprocess simulation, turning on the stress effects modifies many parameters (e.g., equilibrium I/V concentration, band gap, intrinsic carrier concentrations), which affect dopant diffusion via indirect ways. Thus the proper way to simulate the stress effects on the dopant diffusivity is modifying the microscopic dopant-defect pair diffusivity. Then the diffusivity factor is determined by the stress energy difference between the BI ground state and BI transition state.

$$\frac{d_{BI}(\sigma)}{d_{BI}(0)} = \exp\left(\frac{2.8\times10^{-11}\sigma}{kT}\right) \text{ - out-of-plane}$$

$$\frac{d_{BI}(\sigma)}{d_{BI}(0)} = \exp\left(\frac{5.6\times10^{-11}\sigma}{kT}\right) \text{ - in-plane}$$

The current version of Sprocess calculates the stress level correctly up to factor 10 only when ‘Anisotropic’ mechanics is turned on as follows.

pdbSet Silicon Mechanics Anisotropic 1

In the ATOMICS project, the out-of-plane stress factor is implemented and tested by modifying ‘BoronIntDiffFactor’.

term name=BoronIntDiffFactor store add Si eqn = "exp($Vti*StressKK_y/10*2.8e-11)"

The simulated result shows a good agreement with experiments, although it may need additional calibration after other stress dependent parameters (e.g, I/V activation volumes, intrinsic carrier densities) are recalibrated, which is in progress by Synopsys.

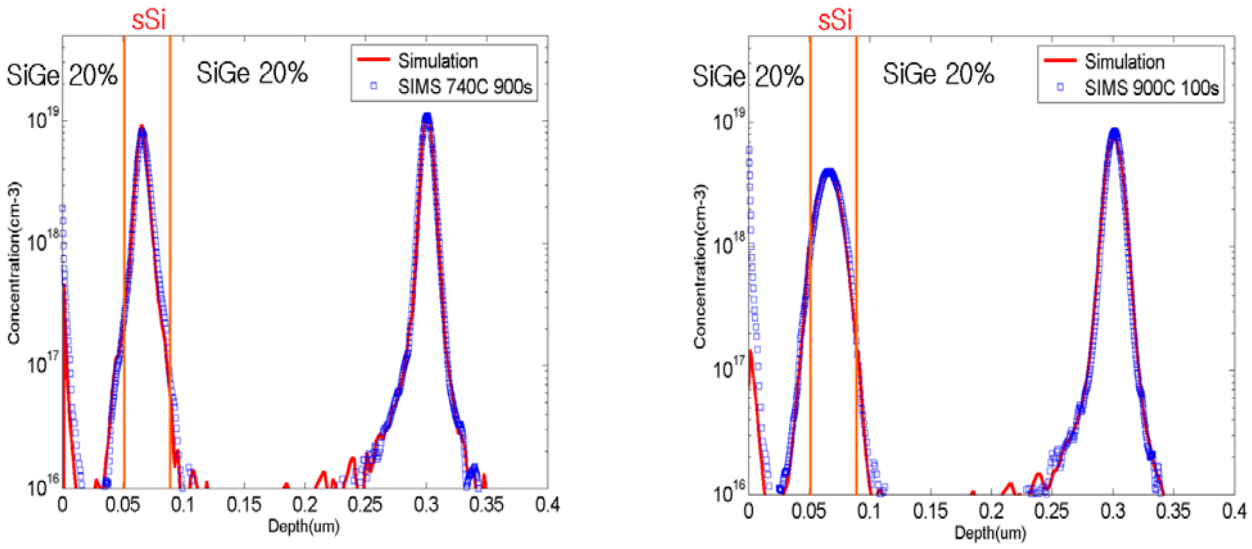

Figure 57: A comparison of B SIMS profiles in sSi and SiGe (20%) with simulated data, (left) 740°C for 900s and (right) 900°C for 100s.

9.2 Composition effects

The presence of Ge in SiGe grown epitaxially on an unstrained Si lattice substrate leads to both global and local strains. The former was taken into account as global stress effects as explained in the previous section, and the latter as local Ge composition effects. Ge composition effects were modeled using a combination of extensive ab-initio calculations and KLMC [65]. For the various key Ge configurations, the change in the BI formation energy at the transition states was tabulated and used as input to KLMC type calculations. Figure 58 shows the predicted in-plane and out-of-plane B diffusivity and the comparison between model and previous experiments. The in-plane diffusion is predicted to be stronger than out-of-plane diffusion. The figure (right) also shows the stress factor and the composition factor separately. The stress factor is stronger than the composition factor.

Although the composition factor is slightly curved, it was also approximated by an Arrhenius equation, which was implemented in Sprocess simulations. The stress effect and the composition effect are multiplied together to predict the total Ge effects on B diffusion in strained SiGe.

term name=BoronIntDiffFactor store add Si eqn = "exp($Vti*(StressKK_y/10.0)*2.8e-11)*exp(-0.227*$Vti * (Germanium/5e22))"

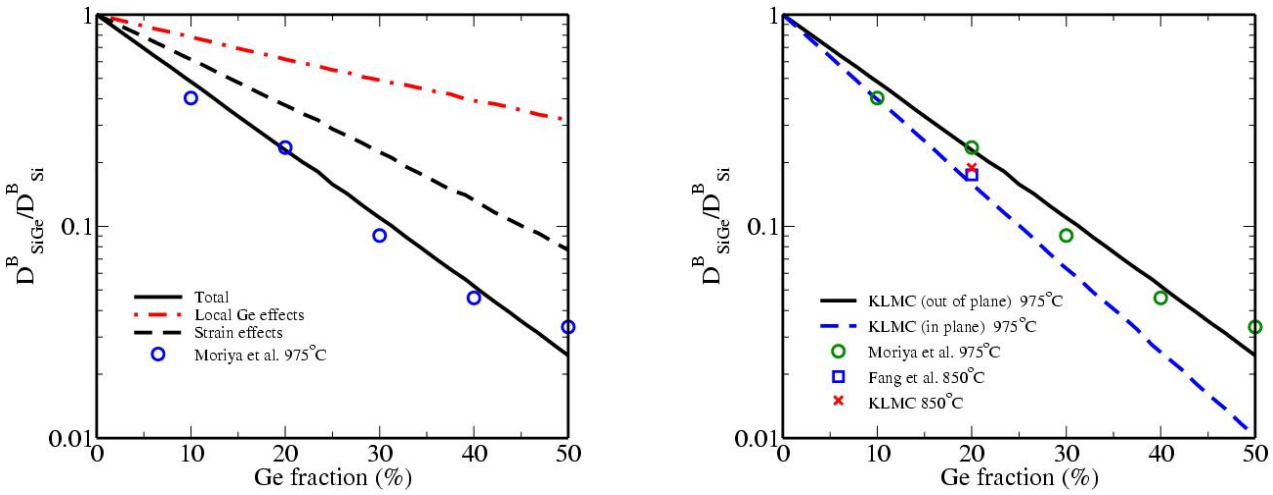

Figure 58: Retarded diffusivity of B in strained-SiGe, modelled including both composition and strain effects. Left: Simulations showing in-plane and out-of-plane components of diffusion, and experimental data on out-of-plane diffusion. Right: Simulation results showing the composition and strain factor contributing to retarded diffusion of B in strained SiGe.

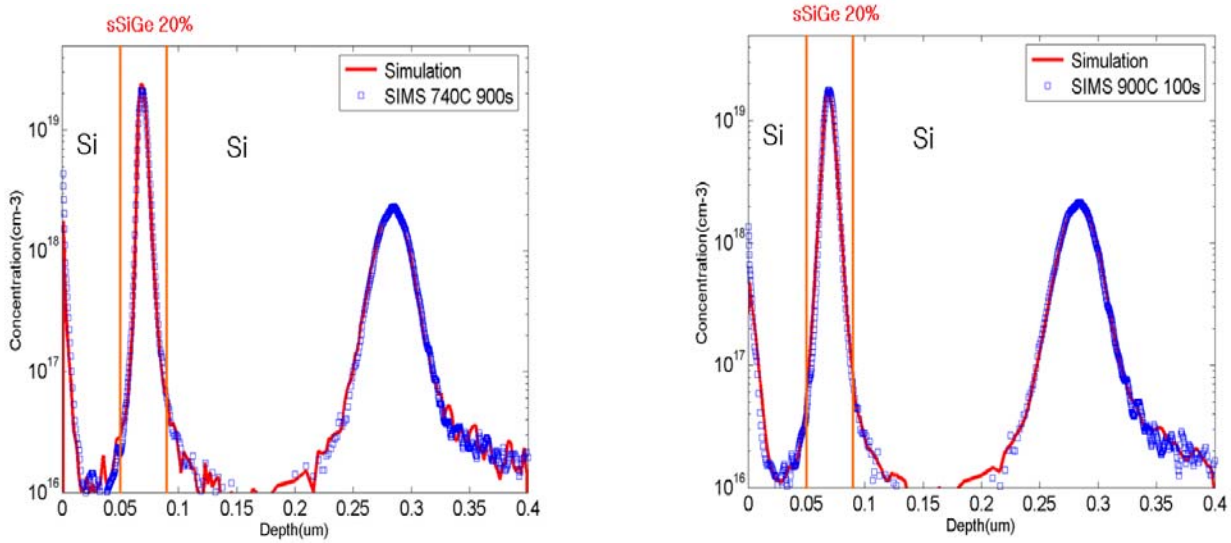

Figure 59: A comparison of B SIMS profiles in sSiGe (20%) and Si with simulated data, (left) 740°C for 900s and (right) 900°C for 100s.

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10 Effect of germanium content and strain on the formation of extended defects in ion implanted silicon/germanium alloys

The fabrication of pseudomorphic SiGe source/drain regions on Si substrates has attracted more and more attention over the last years due to the possibility of inducing tensile strain in Si MOSFETs to enhance carrier mobility in the channel [70]. The optimization of the performances of these devices relies on the capability to accurately model implantation and diffusion phenomena in the SiGe regions, which are strongly related to the evolution of implantation-induced extended defects [71,72]. The effects

of Germanium composition on the evolution of extended defects in Si-Ge layers has already been reported in literature by several publications [73,74,75]. Fedina et al. [75] showed that differently from silicon, the formation of dislocation loops in electron irradiated strained SiGe layers was favoured in comparison with planar {311} defects, due to the presence of strain in the SiGe layer. A similar effect has lately been reported in the case of extended defects formed by ion implantation in unstrained SiGe layer [74], where it is shown that the concentration of Ge in the alloy not only affects the {311}/Dislocation Loops density ratio but also the ripening of these two kinds of defects.

To be able to disentangle the different mechanisms contributing to the modification of defect evolution in SiGe epitaxial layers, the "chemical" contribution due to the presence of Ge and the contribution due to the presence of strain must be studied separately, and in easily comparable structures. For this reason, we have investigated by TEM a large set specifically designed test-structures, including both strained and unstrained Si and SiGe layers of different compositions, to investigate the evolution of extended defects after an amorphising implant.

For the compositional effect study, three wafers containing relaxed SiGe alloy layers with various Ge contents (20, 35 and 50 at. %) were grown by CVD on graded SiGe virtual substrates. For the study of strain effects, two more wafers were fabricated. In the first, a 40 nm tensely strained Si layer was grown on relaxed $Si_{0.8}Ge_{0.2}$ layer, which was followed by the deposition of a 50 nm $Si_{0.8}Ge_{0.2}$ capping layer. In the second, a 40 nm compressively strained $Si_{0.8}Ge_{0.2}$ layer was directly grown on top of a Si substrate, followed by a 50 nm Si capping layer. All wafers were amorphised to a depth of about 60 nm (35 keV Ge^{+} 1×10^{15} cm^{-2}). 2×2 cm^{2} pieces were then cut from each wafer and annealed at different temperatures ranging from 680°C to 800°C.

First, the depth of the EOR defects formed after the amorphising implant and anneal was measured for all the investigated structures and found to be equal to ~65 nm, independently of the Ge content or the strain in the layer. An example is shown in Figure 60 for the reference Si wafer (a), the relaxed $Si_{0.5}Ge_{0.5}$ (b) and the strained $Si_{0.8}Ge_{0.2}$ wafer (c).

Figure 61 shows a visual summary of the evolution of extended defects in the three relaxed SiGe structures after anneal at 800°C for 30 s . The WBDF image taken from the Si specimen (Figure 61a) shows that the majority of defects are {311}s appearing as rod-like bright-contrast lines. Some Faulted Dislocation Loops (FDL) are also visible and appear in the image as elliptical non-uniform bright regions on a dark background (cf. arrows in Figure 61a). In the x=20% relaxed SiGe structure (Figure 61b), the two types of defects are still visible but the size and density of {311}s has decreased, while the density of FDLs has increased. This effect is more pronounced in the 35% (Figure 61c) and the 50% case (not shown), where the totality of defects consist of FDLs. It is important to note that when the apparent defect size is small, the rod-like shape of {311} defects is difficult to detect and it is necessary to apply the TEM visibility criteria on several WBDF images obtained using different diffracting vectors ([220], [400] and [422]) in order to determine their nature.

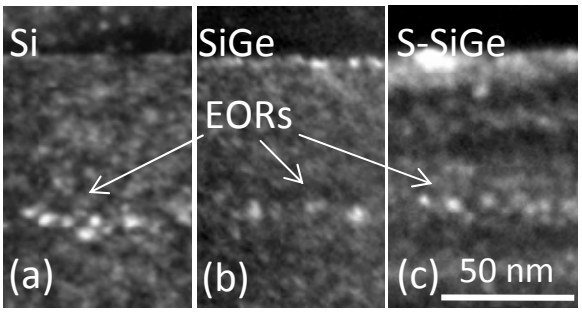

Figure 60 : Cross-section WBDF images of various samples showing the position of the EOR defects after implantation with 35 keV Ge+ 1×1015cm-2 and annealing at 680°C. (a) Bulk Si. (b) Relaxed Si0.5Ge0.5 wafer. (c) Compressively strained Si0.8Ge0.2 wafer.

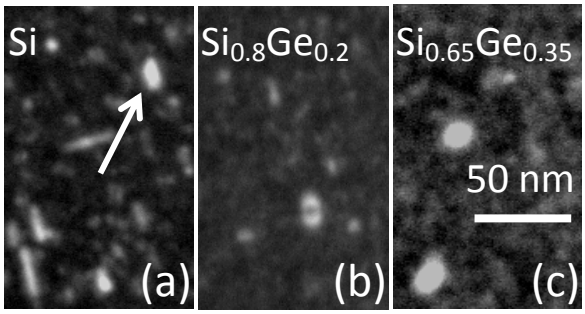

Figure 61 : Plan-view WBDF images of various samples showing the nature and density of EOR defects in relaxed structures with different Ge content after implantation with 35 keV Ge+ 1×1015cm-2 and annealing at 800°C for 30 s. (a) bulk Si; (b) Si0.2Ge0.2 ; (c) Si0.35Ge0.35.

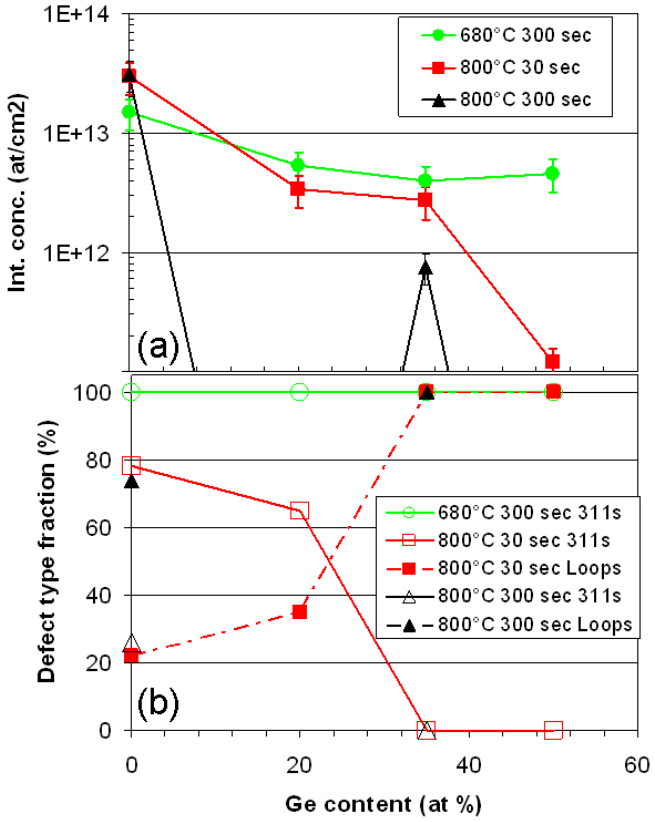

Figure 62: Total density of interstitials contained in all extended defect families (a) and corresponding fractions contained in {311} defects and loops (b) as a function of Ge content in relaxed SiGe structures after implantation with 35 keV Ge^+ $1\times10^{15}cm^{-2}$ and various annealing conditions.

Figure 62 reports the corresponding quantitative analysis of these samples (red squares), as well as of those annealed at 680°C for 300 s (green circles) and at 800°C for 300 s (black triangles). The total density of interstitials trapped in all extended defects is reported on the upper plot as a function of the Ge content in the alloy. When complete defect dissolution has been achieved, i.e. no defects were observed in the microscope, interstitial density value is estimated at ~1×10^8 cm^{-2} (i.e. equal to the TEM detection limit). In the lower plot of Figure 62, the fractions of interstitials contained in each defect type is reported: {311} defects (empty symbols) and Loops (filled symbols). For an annealing at 680°C, {311} defects only are observed in all SiGe structures (empty circles in Figure 62b), which trap a continuously decreasing density of interstitials when the Ge content increases (green circles in Figure 62a), suggesting that in such case {311} defects become more unstable. This effect is enhanced after a 800°C 30 s anneal, where the total density of interstitials in the defects decreases of about 2 orders of magnitude from bulk Si to $Si_{0.5}Ge_{0.5}$ (cf. red squares in Figure 62a). In addition, after such a higher thermal budget anneal, both {311} defects and dislocation loops are observed in the reference bulk Si specimen. In this case, it is found that increasing the Ge content in the alloy leads to an enhanced transformation of {311} defects into dislocation loops (cf. red squares in Figure 62b). When the thermal budget is further increased (800°C 300 s, black triangles in Figure 62), a faster kinetics of both effects due to increased Ge content (lower defect stability and enhanced {311}-to-loop transformation) is expected. The first effect leads to a faster dissolution of all defects while, considering that loops are known to be energetically more stable than {311} defects, the second effect is expected to slow down the dissolution process. The combined effect of both phenomena can therefore explain the apparently puzzling results obtained for this annealing condition: for a 20% SiGe alloy, the density of interstitials contained in loops was only 35% of the total after 30 s. In this case, a longer anneal (300 s) leads to

complete defect dissolution. Instead, for a Ge content of 35%, the defect population entirely consists of loops already after 30 s (filled squares in Figure 62b) which can therefore "survive" to the longer 300 s anneal. Finally, for a $Si_{0.5}Ge_{0.5}$ alloy, the total density of interstitials in the defects is already very low after 30 s at 800°C, so that in this case a longer anneal inevitably leads to a full defect dissolution.

Figure 63 shows a visual summary of the evolution of extended defects in the strained Si and SiGe structures after anneal at 740°C for 900 s. It is found that the {311} defects exhibit a smaller size and a slightly higher density in the strained Si sample (Figure 63a) compared to the reference one (Figure 63c). In addition, while {311}s represent the totality of the defect population in the strained sample, a small fraction of loops is present in the reference unstrained one (cf. arrow in Figure 63a). These results suggest that the Ostwald ripening of {311} defects is somehow weakly "retarded" by tensile strain, which is also responsible for a less effective {311}-to-loops transformation. The opposite behaviour is observed in the case of compressive strain introduced in SiGe layers: while some {311}s are still present in the relaxed SiGe structure (cf. arrow in Figure 63b), the compressively strained SiGe sample only contains loops. As in the previous case, the overall defect stability is not strongly altered, with the total density of interstitials contained in the defects being comparable in the two structures.

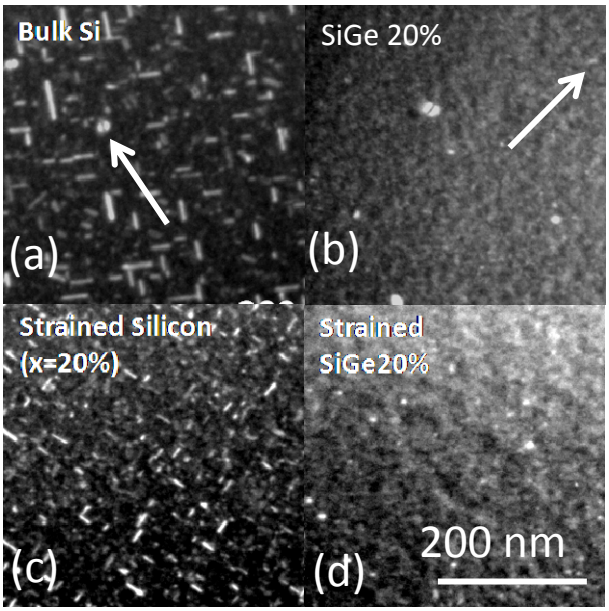

Figure 63 : Plan-view WBDF images of various samples showing the nature and density of EOR defects in relaxed and strained structures with different Ge content after implantation with 35 keV Ge+ 1×1015cm-2 and annealing at 740°C for 900 s. (a) Bulk Si. (b) Relaxed Si0.2Ge0.2. (c) Strained silcon (tensile). (d) strained Si0.2Ge0.2 (compressive).

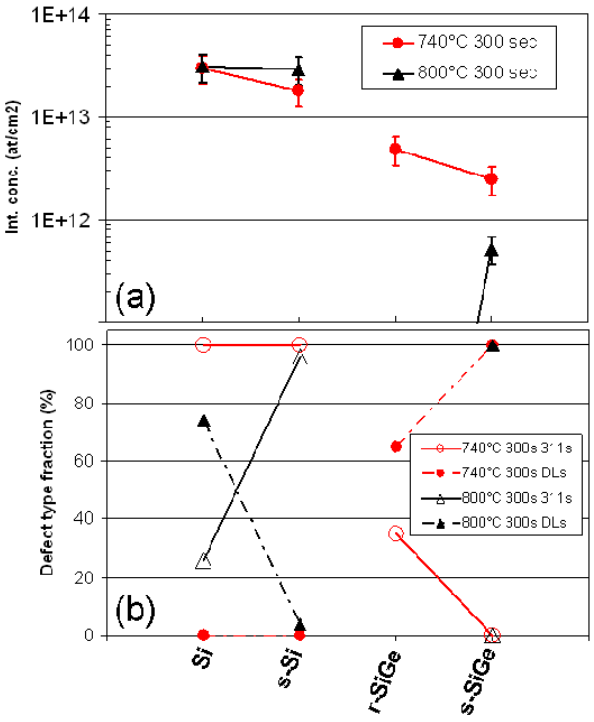

Figure 64 : Total density of interstitials contained in all extended defect families (a) and corresponding fractions contained in {311} defects and loops (b) for various relaxed and strained structures with different Ge content after implantation with 35 keV Ge+ 1×1015cm-2 and different annealing conditions.

The quantitative analysis of the investigated samples confirms this behaviour. Figure 64 reports the data relative to the samples annealed for 300 s at 740°C (red circles) and 800°C (black triangles). It is found that the major impact of tensile strain in Si is to slow down the transformation of {311}s into loops (the fraction of interstitials in loops goes from 75% in Si down to ~5% in sSi at 800°C, cf. filled triangles in Figure 64b), while the total density of interstitials in the defects in not strongly affected (cf. Figure 64a). In contrast, compressive strain in SiGe favours the formation of loops (from 65% to 100% at 740°C, cf. filled circles in Figure 64b), with, again, a weak impact on the total density of interstitials in the defects.

The evolution of an implantation-induced defect population during annealing is the result of several concomitant mechanisms, which in most cases are thermally activated, such as the diffusion of the free interstitials that compose the defects (D_i), the interstitial capture from a given defect (related to the interstitial supersaturation, C_i/C_i^*), the emission of interstitials from a defect (related to its formation energy, E_f), the transformation of {113} defects into dislocation loops (associated to an energy barrier that limits the transformation) and the recombination of interstitials, diffusing out of the defect region, at the wafer surface. A satisfactory explanation of the impact of Ge content (in relaxed SiGe structures) and strain on the defect evolution requires a detailed study of the modification of each one of these mechanisms in strained and relaxed SiGe alloys. While a complete picture is still missing, we tentatively suggest that the modification of the interstitial diffusivity is the most critical parameter to explain the Ge composition effects observed in relaxed SiGe alloys. Indeed, several studies [76,77,78] indicate that both Ge and Si self-diffusivities in relaxed SiGe strongly increase with Ge content (i.e. by a factor of ~300 from Si to $Si_{0.5}Ge_{0.5}$ at 900°C). This leads to an enhanced interstitial recombination at the surface during defect evolution and to an accelerated defect growth. In the case of {311} defects, this also implies that the critical size for transformation into loops [79] is reached more quickly in SiGe alloys than in Si. These modifications are in agreement with both observed effects in relaxed SiGe structures: *(i)* an overall decrease of the defect stability (i.e. a decrease in the total density of interstitials contained in the defects) and *(ii)* an enhanced {311}-to-loops transformation. On the other hand, concerning the effect of strain, theoretical studies [80] indicate that biaxial tensile (compressive) strain in Si induces an increase (decrease) of the interstitial diffusivity. This is apparently in contrast with the observed effects in tensely strained Si, where the "slower" defect ripening with respect to unstrained Si (higher {311}s density and smaller size) is rather in agreement with a lower interstitial diffusivity. A more complex scenario is therefore required to fully explain these results, possibly including the strain effects on both interstitial equilibrium concentration and defect formation energy.

In summary, we have studied the evolution of extended defects in relaxed and strained Si and SiGe structures after an amorphising implant, in order to separately investigate composition and strain effects on defect ripening. The general conclusions of this study can be summarised as follows:

- composition effects: the increase of Ge concentration in relaxed SiGe structures leads to *(i)* an overall decrease of the defect stability (i.e. a decrease in the total density of interstitials contained in the defects) and to *(ii)* an enhanced {311}-to-loops transformation.

- Strain effects: *(i)* Tensile strain (in Si) retards the transformation of {311} defects into loops; *(ii)* compressive strain (in SiGe) enhances the transformation of {311}s into loops; *(iii)* in all cases, the overall defect stability is not strongly modified in the presence of strain.

We suggest that the increase of the interstitial diffusivity in SiGe (compared to Si) is the main mechanism responsible for the observed effects in relaxed SiGe. A more complex scenario, taking into account several contributing mechanisms, is instead needed to fully explain the observed effects in strained Si and SiGe structures, possibly including the strain effects on both interstitial equilibrium concentration and defect formation energy.

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11 Stress and Ge composition effects on extended defect formation and evolution from *ab-initio* calcluations

When point defects are supersaturated – at higher (or lower) concentrations than would occur under thermal equilibrium – the diffusion of dopants changes in proportion to the supersaturation, and prediction of the impact of stress and composition on the time evolution of dopant profiles becomes quite complicated. In tensile strained Si, a weaker but longer lasting transient enhanced diffusion (TED)

is expected because the induced strain of larger size defect clusters ({113}) is larger than that of small interstitial clusters and thus stress energy is released more efficiently by larger clusters [81]. The trend is reversed for even larger size defect clusters (dislocation loops) of which induced strain is slightly smaller than that of {113}. Considering the relative difference of the induced strains, Trzynadlowski et al. predicts that the critical defect cluster size at which the transformation from {113} to dislocation loops occurs becomes lager under tensile stress and vice versa under compressive stress [82]. Recently, it was observed that smaller size {113} defects are favored under tensile stress[83], which implies the average {113} cluster size decreases under tensile stress.

In this work we present stress dependent supersaturations and defect cluster formation energies as a function of cluster size based on an Ostwald ripening model analysis and supportive first principles density function theory (DFT) calculations.

11.1 Point defect supersaturation and defect evolution

In the ATOMICS project the supersaturation of interstitial point defects as a function of annealing temperature and time following amorphizing Ge implantation has been analysed in a zero-dimensional mean-field Ostwald ripening model to extract the interstitial self-diffusion product $D_I C_I^*$ and the differential formation energies $E_f(n)$ of a discrete set of interstitial clusters/defects $\{n\}$. The capture radius is modelled as $a_c = a_0 \gamma n^{1/3}$ where $a_0 = 0.38$ nm, n is the number of self interstitials in the defect, and γ is a numerical enhancement factor fitted to the sizes of larger clusters measured by quantitative TEM. For n < 20, $\gamma = 1$; for n > 30, $\gamma = \gamma_{max}$, and for $20 \le n \le 30$, $\gamma = 1 + (\gamma_{max} - 1)(n/10 - 2)$. The fitted value of $\gamma_{max} = 8$. As an example the extracted cluster energies for unstrained Si, expressed as average formation energies per interstitial, are shown in Figure 65.

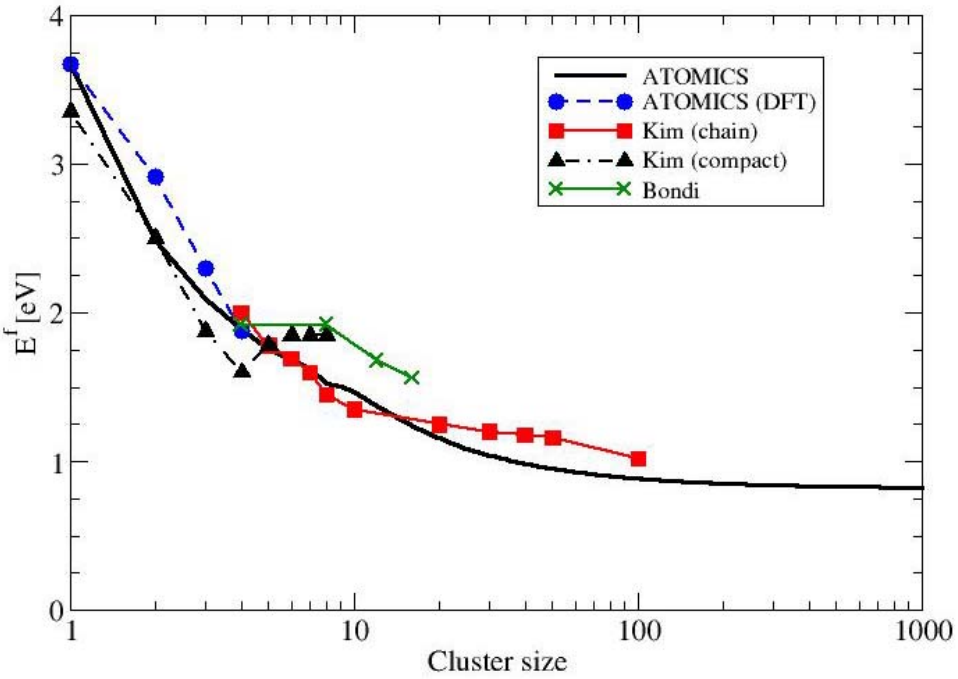

Figure 65: Formation energy per interstitial as a function of cluster size, for unstrained Si. Solid black curve: values extracted the ATOMICS experiments. Black triangles: DFT calculation by Kim *et al.* [84] for small compact interstitial clusters in the size range 2 to 8. Blue filled circles: DFT calculation by Ahn (this work). Red filled squares: DFT results from Ref. [84] for the case of {113} interstitial chains. Green crosses: DFT results for I_4, I_8, I_{12}, and I_{16}, from Bondi *et al.* [85].

The results (solid black curve) are in close agreement with DFT calculations of average formation energies for small interstitial clusters of sizes n=2,3,4 (Kim et al. – black triangles, ATOMICS – blue filled circles), and for larger interstitial chains [84], but does not show the substantial upturn in formation energy suggested by the DFT calculations of Kim et al. for larger compact clusters (n=6,7,8). Improving on the results in Ref. [84], recent DFT calculations have identified configurations at size 12 and 16 which are 0.2 to 0.4 eV more stable than I_4 [85] and somewhat closer to the trend we observe experimentally. However, the calculated energies (green crosses in Figure 65) are still too high and the cluster size dependence too weak to match with experiment. More accurate DFT calculations will probably require significantly larger supercell sizes, achievable in the near future with emerging codes [Briddon et al., Phys. Rev. B (in press)].

11.2 Stress effects on point defect supersaturation and defect evolution

The extracted formation energy values for Si and for strained Si on 20%Ge are shown in Figure 66(a) (average formation energy per interstitial) and Figure 66(b) (differential formation energies). In the case of the average formation energy a theoretical value is needed for the formation energy of the mono-interstitial, since this is not determined from the Ostwald ripening analysis. We take this value from calculations using the DFT code VASP for the cases of unstrained and strained Si.

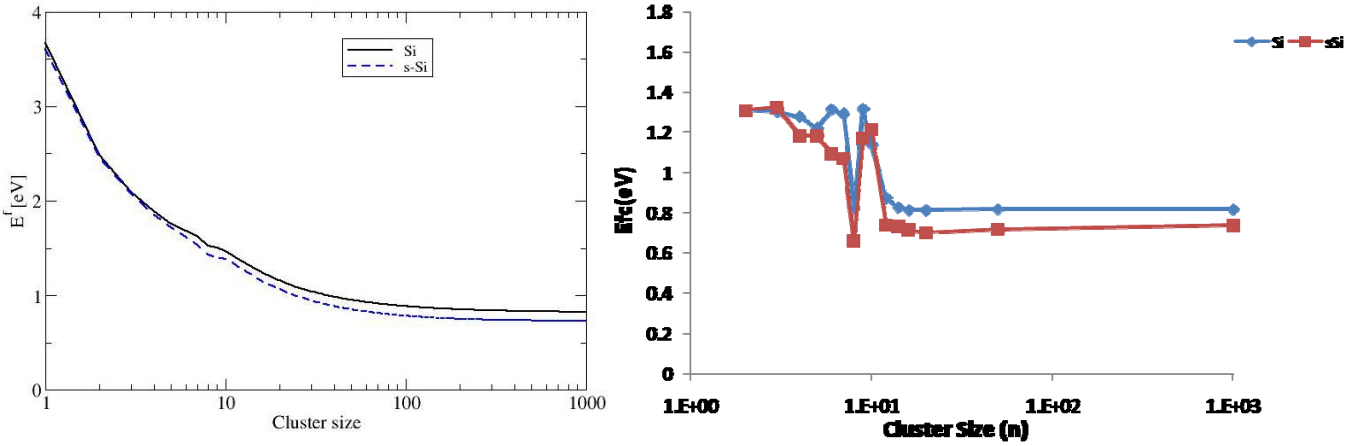

Figure 66: Cluster formation energies for Si and strained Si on 20%Ge, expressed as (a) average energy per interstitial, (b) differential formation energy.

The average formation energy per interstitial shows a deceptively smooth decrease as a function of cluster size. However, the differential result show a strong 'dip' at a cluster size of 8, as previously observed in Ref. [86] and consistent with the trend from recent DFT results predicting the existence of relatively stable clusters with sizes of 8, 12 and 16 [85]. In strained Si on 20% Ge, both the average and differential formation energies for almost all cluster sizes >3 are lowered by an amount of the order of 0.1 eV relative to unstrained Si, which agrees with the calculated stress energy due to the induced strain of {311} defects. Using the full tensor representation of the induced strain due to several types of {311} defects the stress energy per interstitial in strained Si on top of $Si_{0.8}Ge_{0.2}$ is calculated. Figure 67a shows three different {311} structure used to calculate the stress energy. The induced strain of corresponding {311} defects and the stress energies are given by

$$\Delta E_{113}^{in(out)}(\vec{\sigma}) = -V_0 \Delta \vec{\varepsilon}_{113}^{in(out)} \cdot \vec{\sigma}$$

$$\Delta \vec{\varepsilon}_{113\_1chain}^{in} = \begin{pmatrix} 0.174 & -0.060 & 0.382 \\ -0.060 & 0.174 & 0.382 \\ 0.382 & 0.382 & 1.01 \end{pmatrix}, \quad \Delta \vec{\varepsilon}_{113\_1chain}^{out} = \begin{pmatrix} 1.01 & 0.382 & 0.382 \\ 0.382 & 0.174 & -0.060 \\ 0.382 & -0.060 & 0.174 \end{pmatrix}, \quad \Delta E_{113}^{f} = -0.19 eV,$$

$$\Delta \vec{\varepsilon}_{113\_2chain}^{in} = \begin{pmatrix} 0.229 & 0.075 & 0.214 \\ 0.075 & 0.229 & 0.214 \\ 0.214 & 0.214 & 0.804 \end{pmatrix}, \quad \Delta \vec{\varepsilon}_{113\_2chain}^{out} = \begin{pmatrix} 0.804 & 0.214 & 0.214 \\ 0.214 & 0.229 & 0.075 \\ 0.214 & 0.075 & 0.229 \end{pmatrix}, \quad \Delta E_{113}^{f} = -0.16 eV,$$

$$\Delta \vec{\varepsilon}_{113\_plane}^{in} = \begin{pmatrix} 0.304 & 0.085 & 0.078 \\ 0.085 & 0.304 & 0.078 \\ 0.078 & 0.078 & 0.570 \end{pmatrix}, \quad \Delta \vec{\varepsilon}_{113\_plane}^{out} = \begin{pmatrix} 0.570 & 0.078 & 0.078 \\ 0.078 & 0.304 & 0.085 \\ 0.078 & 0.085 & 0.304 \end{pmatrix}, \quad \Delta E_{113}^{f} = -0.13 eV.$$

The presented stress energies are the thermodynamic average at 600°C. The result implies that the stress energy increases as the {311} size decreases, which in turn predicts smaller size {311} defects are favoured under tensile stress – consistent with the TEM observations.

The induced strain of dislocation loops was also calculated using a semi-infinite stacking fault included in a 252-atom supercell. The stress energy of the stacking fault is slightly less than that of {311} (-0.11 eV), which would lead to weaker stress effects if the defect population were dominated by loops. For completeness we note that the induced strained of the dislocation loop is

$$\Delta \vec{\varepsilon}_{DL} = \begin{pmatrix} 0.349 & 0.353 & 0.348 \\ 0.353 & 0.349 & 0.348 \\ 0.348 & 0.348 & 0.355 \end{pmatrix}.$$

The strain-induced change in cluster formation energy, determined by comparing the results for strained and unstrained Si, is shown in Figure 68. Also shown in the left-hand plot are scaled values from first principles calculations for I_4, I_8, I_{12} and I_{16} by Bondi et al. [85]. The scaling procedure normalizes the DFT values for unstrained Si in Ref. [85] to the corresponding experimental values for unstrained Si in Figure 65, and applies the same normalisation factor to the strain induced change in formation energy

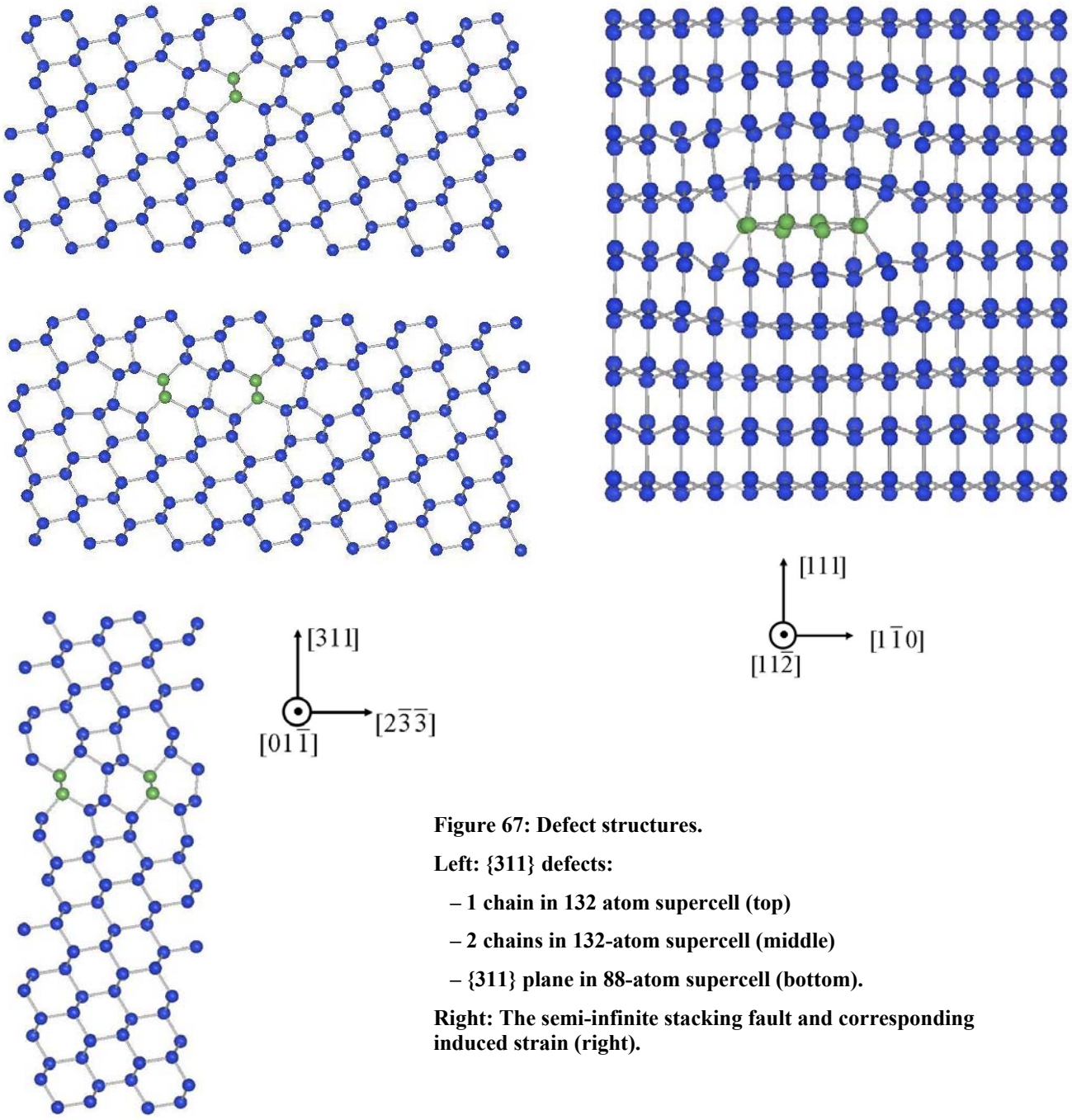

Figure 67: Defect structures.

Left: {311} defects:

- **1 chain in 132 atom supercell (top)**
- **2 chains in 132-atom supercell (middle)**
- **{311} plane in 88-atom supercell (bottom).**

Right: The semi-infinite stacking fault and corresponding induced strain (right).

.

The results are in close agreement with the predicted energies for the favoured defect orientation of I_8, I_{12}, I_{16}. However, a significant discrepancy is found for the case of I_4 despite the expected similarity in behaviour of I_4 and I_8 [85]. We suspect this discrepancy may arise from cluster aggregation effects (occurring via migration of I_2 and perhaps I_3) which are not included in our experimental analysis. Such effects may prevent direct observation of the true I_4 defect energy. This interpretation is supported by the absence of an energy minimum at I_4 in the present study, as compared to the results of earlier experiments with much lower defect densities, which did show such a minimum [86].

This is probably the first, albeit indirect, evidence for a breakdown in mean-field Ostwald ripening behaviour during evolution of implantation damage. It occurs only during nucleation of the smallest interstitial clusters – by the time the mean cluster size reaches ~8, aggregation via small mobile clusters has become negligible and Ostwald ripening is the dominant evolution mechanism.

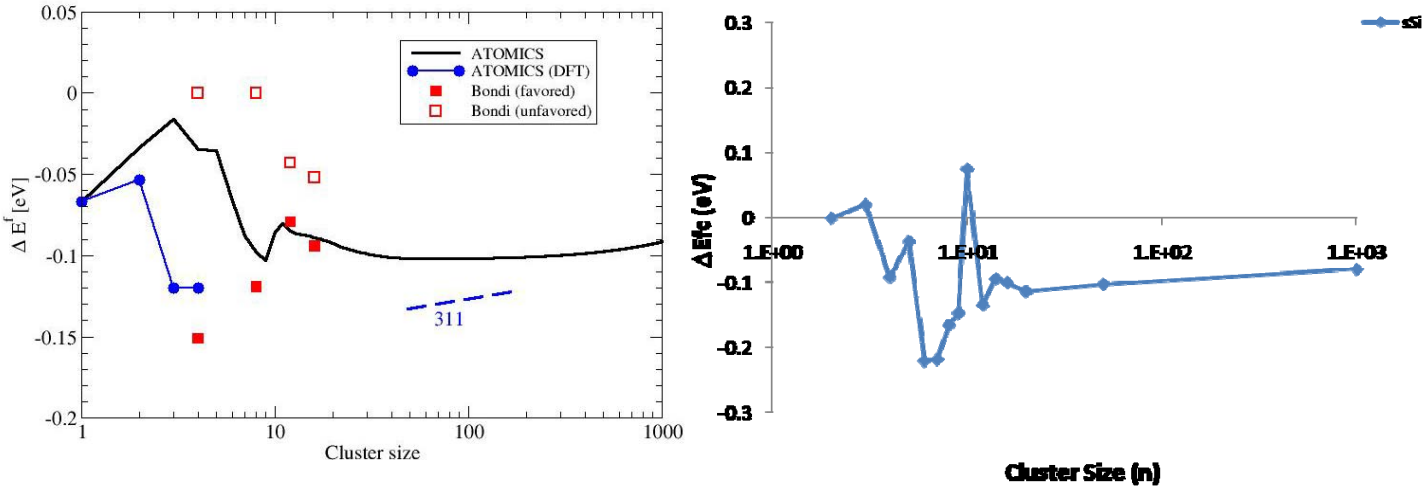

Figure 68: The strain-induced change in cluster formation energy for strained Si on 20%Ge, expressed as (a) average energy per interstitial, (b) differential formation energy. Also shown in (a) are scaled values from first principles calculations for I_4, I_8, I_{12} and I_{16} [85], taking either the low-energy orientation of the defect with respect to the biaxial strain field (I_n^B - open symbols) or the high-energy orientation of the same structure (I_n^A –solid symbols). The dashed blue line in (a) shows ATOMICS DFT calculations for the energy changes of {113} defects.

11.3 Composition effects on point defect supersaturation and defect evolution

The dependence of the extracted cluster energies on Ge content is shown in Figure 69. For small clusters the dependence on Ge content is weak but there is clear evidence for stability minima at multiples of 4 interstitials, at size 8 and 12. In SiGe(50%) the defect at size 12 appears to be the most stable defect in the series.

The behaviour of the extracted cluster energies becomes more complicated at larger sizes. When interpreting this it should be borne in mind that the results were derived assuming a single type of extended defect, whereas in SiGe, in particular, {113} defects typically coexist with dislocation loops. This situation leads to an initial increase in the energy of defects of intermediate size as composition rises from 0 to 20% Ge, probably caused by an increase in the formation energy of {113} defects. This effect is not sustained as composition rises from 20% to 50%, even though {113} defects probably do become less stable in SiGe (50%). The overall drop in energy occurs because at this composition all sizes of {113} defects are unstable with respect to transformation into dislocation loops.

11.4 Summary

A wealth of information on strain and composition effects on defect evolution in Si and SiGe was obtained in the ATOMICS project. The results on strain connect interestingly with fundamental calculations of defect stability in Si as a function of strain, and promise the possibility of better fundamental understanding of nanoscale defects in silicon. A particularly valuable outcome is the possibility of simulating the evolution of defects and the resultant diffusion of dopants in Si and SiGe device structures, and so improves the predictability of a wider range of semiconductor manufacturing processes

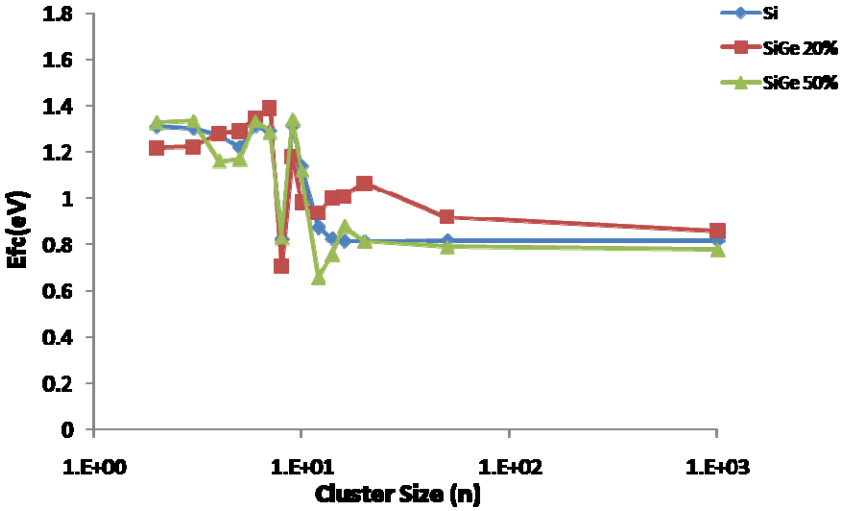

Figure 69: Differential formation energies $E_f(n)$ for Si, SiGe(20%) and SiGe(50%). Clusters sizes of 8 and 12 appear to be particularly stable. The values for SiGe(20%) at large sizes, and for SiGe(50%) at sizes > ~20, may have been significantly reduced owing to a transformation of part of the defect population into dislocation loops.

12 Modeling extended defect formation in silicon from small interstitial clusters via {311}-defects to dislocation loops

Ion implantation in silicon creates silicon self-interstitials, which enhance the point defect-mediated diffusion of dopants during successive thermal anneals. These interstitials also form immobile agglomerates that undergo an Ostwald ripening process and act as a temporary storage of interstitials. The kinetics of the point-defect cluster formation and dissolution govern the time evolution of the interstitial supersaturation and, thereby, the transient-enhanced diffusion of dopants. Different types of interstitial cluster have been reported: small irregular interstitial clusters, rod-like {311} defects, and disk-like perfect or faulted dislocation loops.

The simulation of deep-submicron silicon-device manufacturing processes relies strongly on predictive models for extended defect clusters. For submicroscopic interstitial clusters and {311}-defects, an efficient and highly accurate model for process simulation has been developed and calibrated by Synopsys before ATOMICS [87]. This model combines equations for three small interstitial clusters and two moments for {311}-defects. Within ATOMICS, Synopsys extended this model to include dislocation loops and to reproduce a greatly increased range of experimental data, including thermal annealing of end-of-range defects after amorphizing implants [88].

Only three equations representing three cluster sizes (I_2, I_3, I_4) of different binding energies are needed to simulate the regime of small interstitial clusters. The time evolution of the {311} defects is described by two equations or "moments", one for the interstitial concentration trapped in {311} defects (C_{311}) and one for the density of {311} defects (D_{311}). The concentration C_{311} increases through the capture of free interstitials I by the small cluster type I_4 and {311} defects, while it decreases through the emission of interstitials by {311} defects and the transformation of {311} defects to dislocation loops, as follows:

$$\frac{dC_{311}}{dt} = 5k_f C_I C_{I4} + k_a C_I D_{311} - k_b D_{311} - k_{311->DL} C_{311} \qquad (4)$$

C_I is the free interstitial concentration and C_{I4} is the concentration of small interstitial clusters of size 4. The density D_{311} increases only through the trapping of free interstitials I by I_4, while it decreases through the dissolution of {311} defects, which is scaled by the mean size of the {311} defects, and the transformation of {311} defects to dislocation loops, which is scaled by a factor called k_{D311}. The corresponding equation is:

$$\frac{dD_{311}}{dt} = k_f C_I C_{I4} - k_b \frac{D_{311}}{C_{311}} D_{311} - k_{311->DL} k_{D311} D_{311} \quad (5)$$

The capture of interstitials by clusters is diffusion limited; therefore, the capture rates k_f and k_a are proportional to the interstitial diffusivity D_I. The emission rate k_b depends on the average interstitial binding energy of {311} defects, which is 3.73 eV in this work. The transformation rate $k_{311->DL}$ of {311} defects to dislocation loops will be discussed later.

Analogous to the {311} defects, the dislocation loops are modeled by two fields as well: one for the concentration of interstitials trapped in the loops (C_{DL}) and one for the loop density (D_{DL}). Based on experimental observation [89], the nucleation of dislocations happens through the transformation of {311} defects into dislocation loops. According to Huang et al. [90], the growth of loops depends on the free interstitial concentration (C_I), while the dissolution is governed by the interstitial equilibrium concentration in the vicinity of the loops ($C^*_{I,DL}$). $C^*_{I,DL}$ is higher than the usual interstitial equilibrium concentration (C^*_I) due to the strain and internal energy of the loops:

$$C^*_{I,DL} = C^*_I \exp\left(\frac{\gamma\Omega}{bkT}\right)\exp\left(\frac{\mu b\Omega}{4\pi R_{DL} kT(1-\nu)}\ln\left(\frac{8R_{DL}}{b}\right)\right) \quad (6)$$

where γ is the internal energy associated with the stacking fault, Ω is the volume per silicon atom, b is the magnitude of the Burgers vector for the dislocation loop, μ is the shear modulus, and ν is the Poisson ratio. R_{DL} is the average radius of the dislocation loops defined by:

$$R_{DL} = \sqrt{\frac{C_{DL}}{\pi n_a D_{DL}}} \quad (7)$$

where n_a (1.5×10^{15} cm^{-2}) is the atomic density of silicon atoms on the {111} plane. The time evolution of the loop radius is given by:

$$\frac{dR_{DL}}{dt} = k_{DL}\left(\frac{\pi}{n_a}\right) D_I (C_I - C^*_{I,DL}) \quad (8)$$

where k_{DL} is a constant representing the reaction barrier for loop growth. The time evolution of the total concentration of interstitials in the dislocation loops can be derived using Eq. (7) and Eq. (8) as follows:

$$\frac{dC_{DL}}{dt} = k_{311->DL} C_{311} + k_{DL} 2\pi^2 R_{DL} D_I (C_I - C^*_{I,DL}) D_{DL} \quad (9)$$

The loop density only increases through the transformation of {311} defects to dislocation loops, which is scaled by the factor k_{D311}. The decrease of the loops density is due to the dissolution of dislocation loops because of interstitial emission, which depends on $C^*_{I,DL}$. This is, similar to the {311} density, scaled by the mean size of dislocation loops:

$$\frac{dD_{DL}}{dt} = k_{311->DL} k_{D311} D_{311} + k_{DL} 2\pi^2 R_{DL} D_I (-C^*_{I,DL}) \frac{D_{DL}}{C_{DL}} D_{DL} \quad (10)$$

By setting the constant k_{DL} equal to 1, the dislocation evolution is completely governed by well-known crystal and mechanics parameters of silicon. The stacking fault for silicon is approximately 70 mJ/m^2. The value for the Burgers vector of the most common end-of-range dislocation loop, the faulted Frank dislocation loop, corresponds to an extra {111} plane in the silicon crystal, that is, 1/3 a <111> = 3.13×10^{-8} cm, where a = 5.43 A is the silicon lattice parameter. The elastic constants of crystalline silicon are the Poisson ratio (0.28) and shear modulus (63.28×10^{10} dyne/cm^2).

It is assumed that a {311} defect transforms to a faulted dislocation loop, once it reaches a certain size. Therefore, the term for the {311} defect to loop transformation $k_{311->DL}$ depends on the size of the {311} defects. In addition, a strong dependency on the {311} density is somehow needed to obtain a good overall accuracy compared to experiments, which is achieved by again multiplying the term by the {311} density. Hence:

$$k_{311->DL} = k_{311} \frac{C_{311}}{D_{311}} D_{311} \qquad (11)$$

Since the transformation to dislocation loops is size dependent and affects only the bigger {311} defects, the transformation term is scaled for the defect density fields compared to the one for the concentration of interstitials in the defects. The scaling factor k_{D311} should be less than 1 and greater than 0, and is set to 0.5, meaning that the {311} defects transforming to dislocation loops have an average size that is double the mean size of all {311} defects.

The calibration of the model for extended defects is based on the interstitial supersaturation evolution data extracted from B marker layers experiments and on the data of interstitial concentration in {311}-defects/dislocation loops as well as {311}-defect/dislocation loop density extracted from TEM measurements. For experiments with relatively low interstitial dose and small thermal budget, no dislocation loops can nucleate. For higher implant doses and higher thermal budgets, dislocation loops are generated. All these effects can be simulated accurately with the proposed model, both for ion implantation with and without amorphization, as shown in Figure 70.

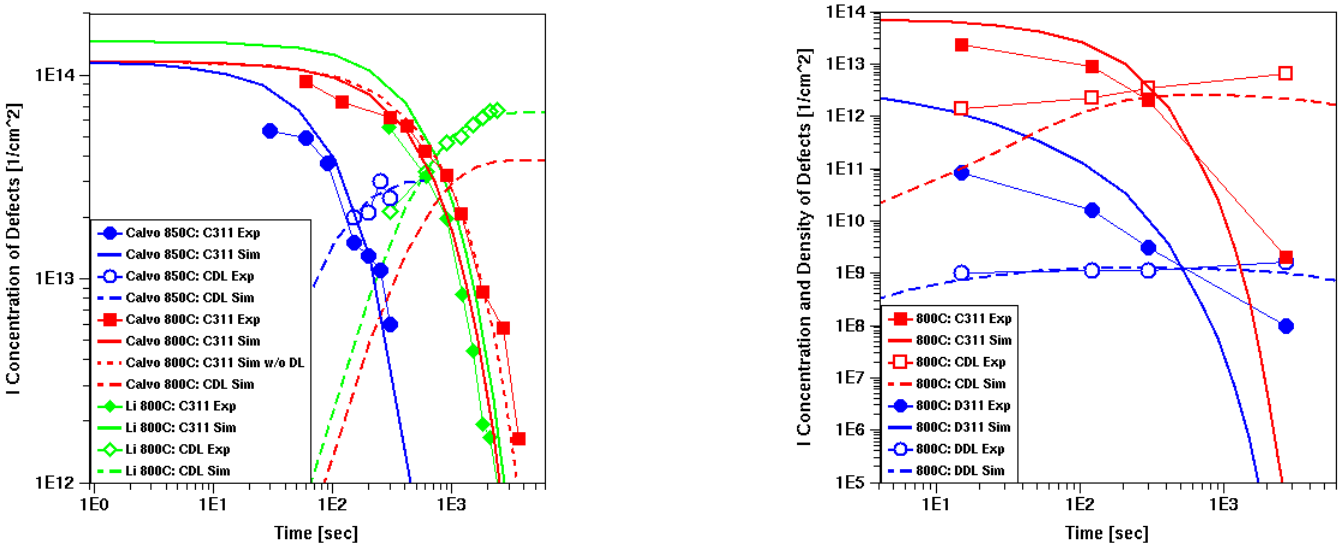

Figure 70: left picture: I concentration in {311}-defects (C311) and dislocation loops (CDL) after Si 2e14 cm^{-2} 100 keV implant. Data from Li [91] and Calvo [92]. For the simulation of Li data, the excess interstitial dose after implantation is increased by 25%. right picture: I concentration in {311}-defects (C311) and in dislocation loops (CDL), and {311} defect density (D311) and dislocation loop density (DDL) after Ge 1e15 cm^{-2} 30 keV implant. Data from Boninelli [93]

The comparison of the model with experimental data shows a good overall agreement and suggests that the underlying physics of extended defects are well described. An improvement of the model accuracy may be achieved by a temperature dependent loop nucleation scaling factor k_{D311} or loop growth reaction barrier k_{DL}. Limiting factors are the inconsistency between the data from different experimental sources and the uncertainties about the initial conditions after ion implantations. However, the advantage of being able to model end-of-range dislocation loops has clearly been demonstrated. Therefore, this comprehensive model for the kinetics of extended defects allows an accurate prediction of transient-enhanced diffusion of dopants.

The model is integrated into the commercial simulator Sentaurus Process and can be applied to one-, two-, and three-dimensional TCAD process simulations at a reasonable computational cost.

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13 Modeling of the effect of the buried Si-SiO_2 interface on transient enhanced dopant diffusion in silicon-on-insulator

The use of silicon-on-insulator (SOI) substrates provides significant advantages for the fabrication of future generations of electronic devices [94]. Reduced short channel effects, improved speed and reduced power consumption in CMOS devices are all achievable with these substrates [95]. An additional advantage of SOI consists in the possibility to reduce the number of silicon interstitials created during the source/drain implant steps, by recombining them at the buried Si-SiO_2 interface, which results in a better control of several deleterious effects, such as extended defects formation [96,97], dopant deactivation [98] and transient enhanced diffusion [99].

The behaviour of the buried Si-SiO_2 interface with respect to the implant-generated interstitial excess has been a longstanding subject of research and, with the exception of few reports suggesting that the interface has no impact at all on dopant diffusion [100] or acts has a reflective boundary for interstitials [101], the vast majority of previous reports show that it behaves as an efficient sink for interstitials [96,97,98,99,102,103,104]. Several physical phenomena have been investigated in these studies which give a more or less direct evidence of the interstitial recombination at the Si-SiO_2 interface and, in some cases, a quantitative estimation of the recombination length for interstitials at the interface, L_{int}, has been given. However, one of these studies was based on the observation of the Boron pile-up at the Si-SiO_2 interface [103], which is difficult to measure by SIMS (Secondary Ion Mass Spectroscopy) due to the change of sputtering and ionisation rate at the interface and also strongly depends on the SOI fabrication method [105]. Others were based on the investigation of boron deactivation due to silicon interstitial atoms emitted by end-of-range defects [98,104]. This requires the concomitant use of structural and electrical measurments (TEM, SIMS, Hall effect in refs.), and several strong assumptions for their quantitative modeling.

Dopant diffusion studies, especially when based on *in-situ* grown dopant marker layers, are expected to provide the most reliable estimation of L_{int}, as they only rely on SIMS measurements and dopant diffusion modeling. Indeed, these have been used in the past to show and quantify the interstitial recombination at the silicon surface [106,107,108,109]. However, when applied to SOI, this method was mainly used to study oxidation-enhanced diffusion [102], yielding L_{int} values (>1 μm above 800°C) much larger than those proposed in other SOI studies (L_{int} <10 nm [98,103,104]).

In the ATOMICS project, we have therefore investigated the effect of the buried Si-SiO_2 interface on the transient enhanced diffusion of boron marker layers grown on SOI substrates following a non-amorphising implant. This has allowed us to verify that the Si/BOX interface acts as an additional sink for interstitials during thermal anneal to provide a reliable estimation of the interface recombination length.

A reference bulk Cz-Si wafer and a Smart-Cut SOI wafer from SOITEC with a Si top-layer thickness of 160 nm were used for this study. An epitaxial Si layer was then grown by CVD on both wafers (about 1.5 μm-thick), containing three Boron marker layers with a peak concentration of ~1×10^{18} cm^{-3}. Implantation damage was then created in both wafers by a non-amorphising Si^+ implant at 40 keV to a dose of 6×10^{13} cm^{-2}. The wafers were then cut into 2×2 cm^2 pieces and corresponding samples from each one were simultaneously annealed at 740°C in N_2 for times ranging from 1 sec to 2 hours, using a Mattson 3000 Plus RTP system. In such conditions, an extended defects layer consisting of {311} defects is expected to be formed, with a defect density peak at a depth of ~100 nm [110] and an initial width of ~150 nm. The boron chemical profiles were measured by SIMS using a CAMECA IMS 6F

system with 1000 eV O_2 primary ions and oxygen flooding under non-roughening conditions [111]. Finally, for the diffusion data analysis, we used a fitting method based on the interstitial kick-out mechanism [112] to extract the diffusion enhancement, D_B/D_B* which provides, in turn, a direct measurement of the silicon point defect supersaturation, $S_{Int}= D_B/D_B^* = C_I/C_I^*$, where D_B is the boron diffusivity, C_I is the interstitial point defects concentration and the stars indicate the parameters' equilibrium values.

Figure 71 shows B depth profiles measured by SIMS in the bulk Si reference (Figure 71a) and in the SOI wafer (Figure 71b) after implantation with 40 keV Si^+, 6×10^{13} cm^{-2}, and annealing at 740°C for different times (1sec, 300 sec and 2700 sec, respectively). A significant diffusive broadening is observed for all the boron marker layers after each time interval. This broadening largely exceeds what would be expected from an equilibrium diffusion process, indicating that implantation-induced enhanced diffusion has occurred, in agreement with the presence of a defect layer in the implanted region [113]. In addition, it appears that the three boron marker layers in the Si wafer exhibit a similar diffusion behaviour independently of their depth position. In contrast, the broadening of the marker layers in the SOI wafer, while being sistematically less pronounced than in the Si reference, continuously decreases when going from the shallowest to the deepest one. This results are clearly consistent with an efficient interstitial trapping at the buried Si-SiO_2 interface, in agreement with previous reports [99,103]. However, a quantitative analysis of the experimental results can only be done after the TED levels associated to the measured profile broadenings have been correctly evaluated.

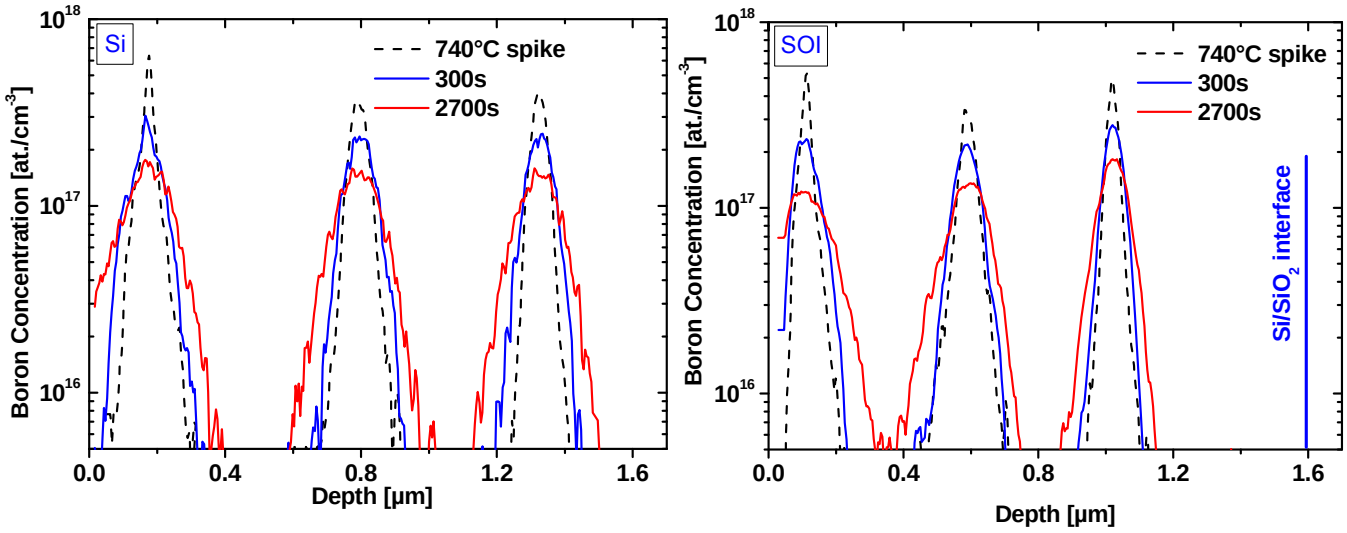

Figure 71: Boron depth distribution profiles following Si^+ implantation at 40 keV 6×10^{13} cm^{-2} and annealed at 740 °C for various time intervals.

It has to be noted that in both wafers the shallowest Boron marker layer lays within the defect region. Although the Boron concentration is quite low and it is not expected to affect defect formation as previously suggested in ref. 114, the top marker layers of the two wafers have not been considered for the extraction of the interstitial supersaturation. The results obtained for the reference Si wafer at an annealing temperature of 740°C are shown in Figure 72 (filled symbols and solid lines). The reported time evolution of the S_{Int} is in agreement with the well known evolution of the implantation-induced defects which are responsible for the diffusion enhancement [113,115]: the almost constant value of supersaturation for annealing times up to 600 sec corresponds to the Oswald ripening of the {311} defects, while the final decrease is due to their dissolution. More importantly, both boron marker layers exhibit the same diffusion enhancement, independently of their depth. Considering the high diffusivity of silicon interstitials and the absence of traps in the grown structures, the measured interstitial supersaturation therefore corresponds to the one which exists in the defect region.

In Figure 72 we also report the simulation results (dashed line) after annealing at 740°C, obtained using the commercial software Sentaurus Process from Synopsys [116]. As-implanted nterstitial and vacancy

profiles are generated using the built-in implant simulator which is based on a Monte Carlo binary collision approximation model with cumulative damage. Boron diffusion is described by a 5-stream diffusion model [116] already implemented in the process simulator. The whole defect evolution is described by the model of Zographos et al. [117]. As shown in the Figure, after calibration, the time dependence of the interstitial supersaturation is perfectly predicted by the simulations.

Finally, Figure 73 reports the experimental and simulation results of Boron TED in the SOI wafer (dotted lines: simulations; symbols: experiments). In this figure, the interstitial supersaturation is plotted as a function of the depth of the analysed marker layers and the various curves correspond to the different time intervals investigated. The points located at a depth of 100 nm represent the interstitial supersaturation value in the region containing the implantation-induced {311} defects, as extracted from the Si reference wafer.

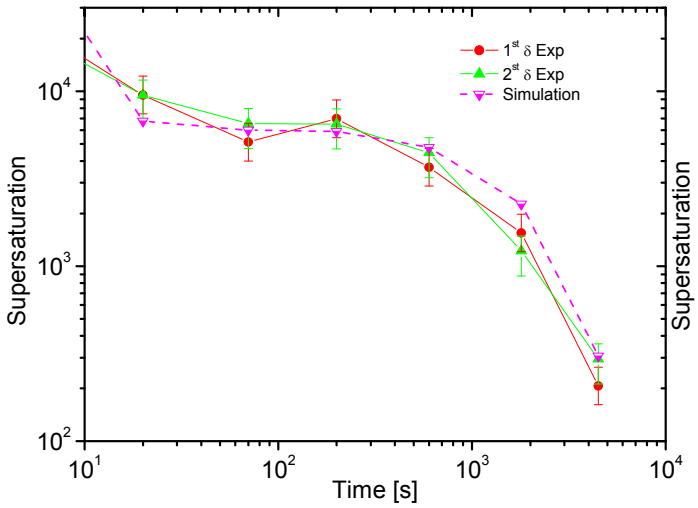

Figure 72: Interstitial supersaturation in the bulk structure, versus time. Implantation of Si at 40 keV and a dose of 6×10^{13} cm^{-2}. The dashed curves are simulated with SProcess. Surface recombination length=1nm. The two boron marker layers are located at a depth of 780 nm and 1330 nm, respectively.

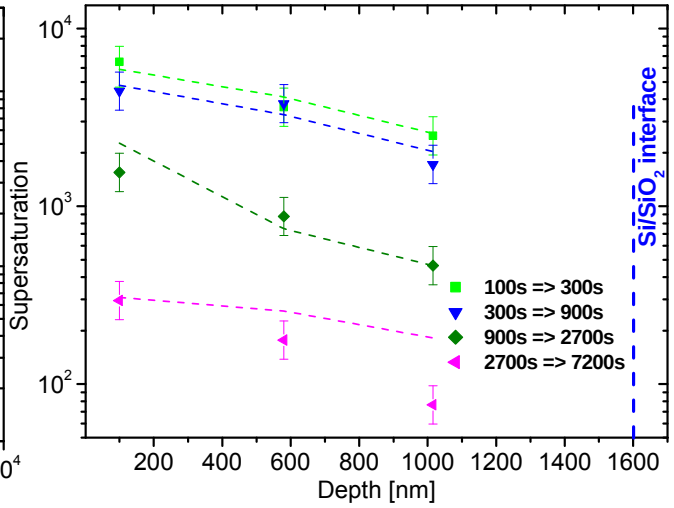

Figure 73: Depth dependence of the diffusion enhancement of boron marker layers grown on a SOI substrate, during annealing at 740 °C following Si^+ implantation at 40 keV 6×10^{13} cm^{-2}.

The experimental results shown in Figure 73 clearly indicate that, over the entire annealing time range, the interstitial supersaturation continuously decreases when approaching the buried Si/SiO_2 interface, confirming that excess interstitials diffusing out of the defect region recombine at the buried Si/SiO_2 interface, in agreement with previous studies. For the simulation of the SOI supersaturation data, the buried oxide layer is therefore placed below the Si CVD-grown layer, to take into account the presence of an additional trapping interface, while keeping all the other simulation parameters fixed to the values obtained from the reference Si wafer. The excellent agreement between simulations and experiments clearly confirms that the observed phenomenon in SOI wafers can be modelled in terms of an additional capture of interstitials at the buried Si/SiO_2 interface. The best results were achieved using an interstitial recombination length at the Si/BOX interface, L_{int}, of 1 nm.

In summary, Boron TED measurements were investigated in Si bulk and SOI wfers. The obtained data clearly confirm that the Si/BOX interface is an efficient trap for the Si interstitial atoms diffusing out of the defect region. Based on these experiments, existing models for the simulation of B TED in Silicon have been modified to include an additional buried recombination site for silicon interstitials. The best results were achieved using an interstitial recombination length at the Si/SiO_2 interface, L_{int}, of 1 nm.

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14 Modeling of boron trapping at end-of-range defects in pre-amorphized ultra-shallow junctions

One of the main challenges of the continuous downscaling in metal-oxide-semiconductor (MOS) transistor manufacturing is the attainment of low-resistance and ultra-shallowjunctions. One way to achieve shallow junction formation is through pre-amorphizing implants (PAI) to reduce ion channeling during implantation and to improve dopant activation [118]. PAI co-implant creates a large amount of damage in the Silicon lattice just beyond the amorphous/crystalline (a–c) interface [119], which upon annealing precipitates into the so-called end-of-range (EOR) defects. The EOR defects as well as their later dissolution generate a local point defect supersaturation that may affect heavily the diffusion and the activation of dopants through various phenomena, such as transient-enhanced diffusion (TED) [120,121] and boron-interstitial cluster (BIC) formation [122,123]. In addition, it is known that in ultra-shallow p–n junctions fabricated using PAI, the tail of the dopant concentration profiles shows an anomalous peak [124,125] in correspondence with the EOR defects. With the progressive reduction of the junction depth, predicted by the ITRS, this phenomenon will become more and more critical, as, in ultra-shallow junctions, both the EORs and the B peaks are located at few nanometers from the surface.

It is generally accepted that the boron atoms trapped by the EOR defects in the so-called “trapping peak” are immobile and electrically inactive. However, the EOR defects are known to exist under various kinds: SMall Interstitial Clusters (SMICs) of a few atoms, {311} defects, {111} rod-like defects, and Dislocation Loops (DLs) [126,127,128], and it is therefore important to understand which of these defects are more effective in trapping boron atoms in order to reliably simulate this phenomenon.

Colombeau et al. [125] developed a boron-trapping model in which it is assumed that the capture of boron atoms depends only on the density of SMICs. Due to the intrinsic nature of the Ostwald ripening mechanism of the defect evolution, this model systematically predicts a decreasing trend for the boron-trapping peak when increasing the thermal budget (either annealing time or temperature).

However, some experimental data [129] show that the boron trapping peak can have a different behaviour and for instance it increases in the early stage of annealing. Therefore, more data and an improved model are needed to correctly predict the boron diffusion profile in the vicinity of the EOR defects region.

In the ATOMICS project, we first used a dedicated structure to experimentally study the boron trapping at EOR defects, by a combination of secondary ion mass spectrometry (SIMS) and plain-view Transmission Electron Microscope (TEM) measurements. Based on the experimental results,we have then developed and implemented in the Synopsys Sentaurus Process process simulator a boron-trapping model that takes into account the direct influence of both {311} defects and DLs, and this for the first time. Our results clearly show that the {311} defects are more effective than DLs in trapping boron atoms.

The physical basis for our approach is shown schematically in Figure 74. A Silicon wafer with a nominal uniform boron concentration ~2×10^{18} cm^{-3} was used to study the impact of implant-induced defects on the redistribution of boron atoms. The wafer was preamorphized by a 30 keV Ge^{+} implant to a dose of 1×10^{15} cm^{-2}. The Ge PAI provides an as-implanted amorphous layer thickness of ~50 nm, as previously measured by cross-section TEM analysis [127].

The wafer was then annealed in an N_2 ambient at 700, 800, and 900°C for various times ranging from 3 to 1000 s. The final distribution of {311}’s and DLs was analysed by TEM using Weak Beam Dark Field (WBDF) imaging conditions. It has to be noted that the boron doping concentration was chosen to avoid any modification of the defect evolution by the presence of boron, as previously suggested in Refs. 130,131,132. This allowed us to simultaneously observe the evolution of {311} and DL densities in all of the annealed specimens. The boron concentration profiles were measured by SIMS.

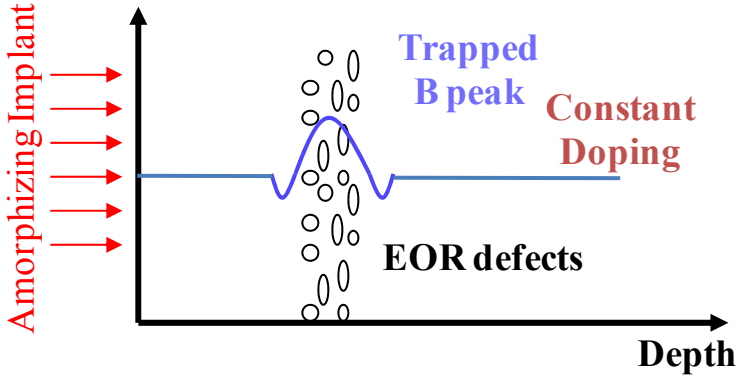

Figure 74: Schematic illustration of the structure used in this experiment and physics underlying initial conditions for investigating boron trapping at EOR defects.

Figure 75 (dashed lines) shows the measured boron profiles after annealing at 700°C, for various annealing times. All the profiles exhibit a peak at a depth of 50nm (the measured position of the EOR defects band) which indicates boron trapping at EORs. At this temperature, the maximum boron concentration in the trapping peak is found to increase with increasing annealing time. TEM analysis performed on the same samples (not shown) indicates that at this temperature only {311} defects are formed, when undergo the usual Ostwald ripening (i.e. increase in size, decrease in density). This clearly suggests that {311} defects actively contribute to the formation of the trapping peak.

At 800°C, it is observed that the boron-trapping peak firstly increases, and then decreases with increasing annealing time, while at 900°C, the boron-trapping peak systematically decreases with increasing annealing time. TEM analysis (not shown here) indicates that, at 900°C, only DLs are present, that, similarly to the {311} defects in the samples annealedat 700°C, increase in size and decrease in density during annealing.On the other hand, a more complex evolution is observed during annealing at 800°C, with the {311} defects, representing the vast majority of the defects population, progressively transforming into DLs as a function of annealing time. It has to be noted that, independently of the annealing temperature, once DLs are formed, they are energetically stable and are therefore expected to be still present even after very long anneals.

Figure 76 (squares) summarizes the time evolution of the maximum boron concentration in the trapping peak, as extracted from SIMS data. It can be noted that the highest peak concentration achievable at 900°C (after a 3 s anneal), is lower than that observed at the other temperatures. Furthermore, the boron trapping peak quickly disappears after some seconds of annealing, although DLs are still present for annealing times up to some hundreds of seconds. This result suggests that the DLs contribution to trapping is less pronounced than that of {311}s. In fact, the boron trapping peak, that is visible for small annealing times, could be associated to the initial presence of {311}s, which are known to be entirely replaced by loops after a few seconds anneal at 900°C. This hypothesis is compatible with the 800°C trend in which the peak value starts to decrease at a later time during annealing. This can be understood considering that the transformation of {311}s into loops takes place at longer annealing times for 800°C anneals with respect to 900°C.We can conclude from the experimental data that the evolution of boron-trapping peak is driven by the evolution of {311} defects and that the DLs contribution to the trapping mechanism is less pronounced.

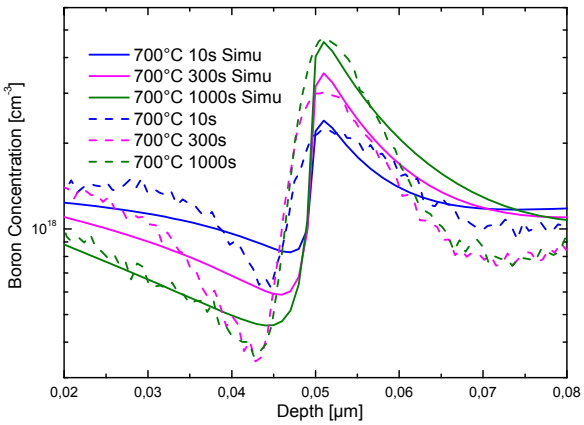

Figure 75: Comparison between experimental (dashed lines) and simulation (solid lines) data of Boron concentration profiles after annealing at 700 °C.

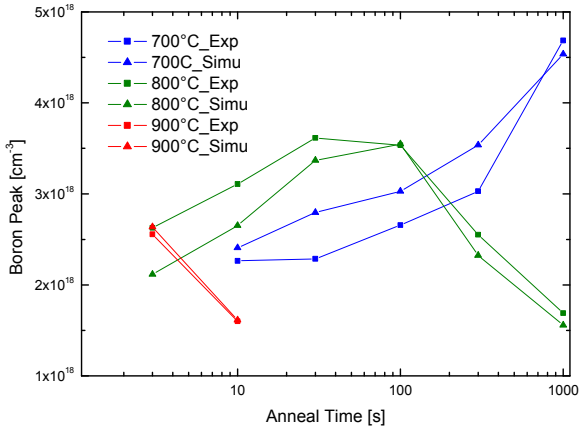

Figure 76: Boron-trapping peak evolution for various annealing temperatures: comparison between experimental data (squares) and simulation results (triangles).

For the simulation of the experimental data, we have used the commercial software Sentaurus Process [133]. In order to simulate {311} and loops nucleation, interstitial and vacancy profiles are generated for each implant dose and energy using the built-in implant simulator, which is based on a Monte Carlo binary collision approximation model with cumulative damage. The BI diffusion is described by a 5-stream diffusion model [125] already implemented in the process simulator. The whole defect evolution is described by the model of Zographos et al. [134]

In order to model the boron trapping at EOR defects accurately and efficiently, some simplifying assumptions were required. Only neutral BI pairs (B^-I^+) can be captured and emitted from extended defects in our model. Moreover, it is assumed that SMICs (I2, I3, I4) do not contribute to the total amount of boron trapping at EOR defects and that the mobile BI pairs can only be trapped by {311} defects or DLs. It was also assumed that the trapped B^-I^+ pairs are located along the defects' perimeter.

We first define the "BI capture efficiency" of a defect as the ratio, $\alpha_{Bdefect}^{\max}$, between the number of available traps along the edges of the defect and the total number of interstitial atoms in the defect, $\alpha_{B311}^{\max}$, which is given by the following formula:

$$\alpha_{B311}^{\max} = \frac{2 \cdot \sqrt{\rho_{311}} \cdot (L_{311} + w_{311})}{w_{311} \cdot L_{311} \cdot \rho_{311}}$$

where *w311* is the {311} width on a [3 1 1] plane (which is supposed to be a constant equal to 4 nm, consistently with previously reported models [135], ρ_{311} =5×10^{14} cm^{-2} is the interstitial density in a {311} defect, and consequently $\sqrt{\rho_{311}}$ is the linear density of interstitials in a {311} defect and *L311* is the average {311} defects length and can be calculated as follows:

$$L_{311} = \frac{C_{311}}{\rho_{311} \cdot D_{311}}$$

where $\frac{C_{311}}{D_{311}}$ represents the average number of interstitials trapped in a {311} defect.

For dislocation loops, the definition of $\alpha_{Loop}^{\max}$ is as follows:

$$\alpha_{BDL}^{\max} = \frac{2\pi \cdot R_{Loop} \cdot \sqrt{d_{111}}}{\pi R_{Loop}^{\ 2} \cdot d_{111}} = \frac{2}{R_{Loop} \cdot \sqrt{d_{111}}}$$

where R_{Loop} is the average radius of dislocation loops, given by

$$R_{Loop} = \sqrt{\frac{C_{Loop}}{2 \cdot \pi \cdot d_{111} \cdot D_{Loop}}}$$

With C_{Loop}/D_{Loop} being the average number of interstitials trapped in DLs and $d_{111} = 1.57\times10^{15}$ cm^{-2} is the density of atoms in a {111} silicon plane.

We further assume that all capture rates are diffusion-limited and proportional to the concentration of free trap sites for BI at {311} defects and DLs edges, respectively.

The capture rate for BI at {311} defects can be expressed as

$$K_{311}^{cap} = 4\pi \cdot r_{B311}^{cap} \cdot D^{BI} \cdot C_{BI} \cdot C_{B311}^{*}$$

where r_{B311}^{cap} is the capture radius, D^{BI} the diffusivity of $B^{-}I^{+}$ pairs, C_{BI} the concentration of $B^{-}I^{+}$, and $C_{B311}^{*} = \alpha_{B311}^{\max} \cdot C_{311} - C_{B311}$ is the concentration of free trap sites for BI on {311} defects. The capture radius is a model parameter and can be expected to be close to the interatomic distance in the Si lattice (~1 Å).

The capture rate of BI at the perimeter of the loops can be similarly expressed as

$$K_{Loop}^{cap} = 4\pi \cdot r_{BDL}^{cap} \cdot D^{BI} \cdot C_{BI} \cdot C_{BLoop}^{*}$$

Again, r_{BDL}^{cap} is a calibration parameter, which is expected to be close to the interatomic distance in the Si lattice while the total free concentration of trapping sites on loops, C_{Loop}^{*}, can be obtained by

$$C_{BLoop}^{*} = \alpha_{BLoop}^{\max} \cdot C_{Loop} - C_{BLoop}$$

The emission rates of trapped BI from {311} defects and loops are assumed to be simply proportional to the number of trapped BI:

$$E_{311}^{BI} = e_{311}^{BI} \cdot C_{B311}, \qquad E_{BDL}^{BI} = e_{BDL}^{BI} \cdot C_{BDL}$$

e_{311}^{BI} and e_{BDL}^{BI} are the most important parameters for the calibration of the model. Since the emission process involves a reaction barrier it should be possible, at least in principle, to express these coefficients as an Arrhenius function of the temperature.

In conclusion, the model has four calibration parameters: r_{B311}^{cap}, r_{BDL}^{cap}, e_{311}^{BI} and e_{BDL}^{BI}, whose values must be determined by comparison with the experimental data.

Before adding the boron-trapping model to the simulations, the extended defects' evolution has been simulated and compared with the experimental results such as those presented by Boninelli et al. [127]. The results confirmed that the defect evolution was well simulated by Sentaurus Process. Once this verification was completed, we have proceeded to the calibration of boron-trapping parameters. It has to be noted that when using the extended defect model in the anneal simulation of the defect evolution, interstitials can be captured or released from a {311} defect or a loop. Therefore when adding the boron-trapping model developed in this work, free $B^{+}I^{-}$ couples and free interstitials interact independently with {311}s and loops.

As an example, Figure 75 presents the results of simulations (solid lines), as compared with experimental data (dashed lines) after annealing at 700°C. The increasing trend of the peak

concentration is well reproduced by the simulations, and this for all of the three investigated temperatures (800 and 900°C are not shown).The simulation results are summarized in Figure 76 (triangles), which presents the evolution over time of the boron-trapping peak at 700, 800 and 900°C. Indeed, the various trends of the peak concentration at different temperatures are perfectly reproduced, including the peak concentration decrease observed at 900°C as well as after 100s at 800°C, when most of the {311} defects have been transformed into DLs. The results confirm that the observed phenomenon can be modeled in term of capture and release of boron atoms at the {311} defects formed in the EOR region.

In summary, Boron trapping at EOR defects was investigated by SIMS and TEM. The experimental results suggest that the evolution of the boron trapping peak is driven by the evolution of {311} defects and that the DLs contribution to the trapping mechanism is less pronounced. An analytical model for the conccomitant boron trapping at {311} defects and dislocation loops was developed by taking into account the geometry of the EOR defects. The trapped species is represented by neutral BI pairs which can be captured either by {311} defects or by dislocation loops. The model accurately reproduces the complex evolution of the trapping peak as a function of both the annealing time and temperature. These results confirm that the evolution of the boron-trapping peak is closely related to the evolution of the {311} defects, therefore suggesting that boron trapping is associated to the capture and release of boron at the {311} defects formed in the EOR region.

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15 Diffusion and activation models for dopants

15.1 ChargedCluster Model

The *ChargedCluster* model implemented in Sentaurus Process is based on the model for BIC formation and dissolution developed in the FRENDTECH EU-project. Within the project ATOMICS, its implementation has been improved and generalized to enable its usage for any type of cluster family, such as BICs, As-V-clusters, or F-point defect clusters. A brief summary is given in the following. For simplicity and readability, the model summary is given in terms of BICs, although the implementation is not limited to this particular use case.

- We consider a family of dopant – defect clusters, e.g. BICs.
- Each cluster is identified as B_mI_n, where m is the number of substitutional B atoms and n is the number of silicon self-interstitials needed to form the cluster. n can be positive, zero, or negative. In the last case, we would have a B-V cluster rather than a BIC. Each cluster has the following properties:
    - Formation energy E_{form}. This is defined as the energy needed to form the cluster from substitutional B atoms. The formation energy includes the energy needed to create (at the silicon surface) the point defects incorporated in the cluster.
    - Cluster degeneracy N
    - Cluster charge. In the current implementation, only a single charge state is allowed for one type of cluster. Only free point defects and dopant-defect pairs, which are the only mobile species in the model, and which may both be considered as the smallest possible "clusters", are allowed to occur in various different charge states, with a relative abundance depending on the local Fermi level.
- The formation and diffusion of point defects and dopant-defect pairs (the smallest clusters) is implemented outside the *ChargedCluster* model. The *ChargedCluster* model can be used in

combination with the *ChargedPair* (3-stream) or the *ChargedReact* (5-stream) diffusion model for dopants.

- Cluster "growth" is described by any of the four reactions:
  - $B_mI_n + I \rightarrow B_mI_{n+1}$
  - $B_mI_n + V \rightarrow B_mI_{n-1}$
  - $B_mI_n + BI \rightarrow B_{m+1}I_{n+1}$
  - $B_mI_n + BV \rightarrow B_{m+1}I_{n-1}$

  Each cluster has a capture radius for each of the above reactions. Typically, the capture radius is close to the lattice constant of silicon. By using an Arrhenius function for the capture radius, the growth reaction rate may include an energy barrier. All "growth" forward reactions are expressed by:

  $$\text{Forward rate} = 4\,\pi\, r_{capture} \times e^{-Ebarrier/kT} \times [A] \times [B] \times (D_A + D_B)$$

  Here [A] and [B] are the concentrations of the reaction partners, and D_A and D_B are the corresponding diffusivities. If one or both reaction partners may appear in several charge states (this is allowed for point defects or dopant-defect pairs), a summation is done over all possible combination of charge states.

- Cluster dissolution by emission of mobile particles is described by the corresponding backward reactions. The reaction rates are derived from the principle of detailed balance (in thermal equilibrium, for each individual reaction, the forward and backward rates must be equal) and from the equilibrium concentration of clusters, which can be derived from statistical thermodynamics as:

$$(B_mI_n)^c_{equilibrium} = N \times B_{SUB}^{\wedge m} / 5e22^{\wedge(m-1)} \times (I/I_*)^{\wedge n} \times (n/n_i)^{\wedge(-m-c)} \times \exp(E_{form}/k_BT)$$

  where c is the cluster charge, m is the charge of substitutional B, and I/I* is the local interstitial supersaturation.

In *Sentaurus Process*, the *ChargedCluster* model can be selected for individual impurities. Calibrated default parameters exist for the following cluster families:

- BICs (B_2, B_2I, B_2I_2, B_3I, B_3I_2, B_3I_3)
- As-V clusters (As_2, As_2V, As_3, As_3V)
- In-I clusters (In_2I, In_2, In_2V)
- F-I clusters (F_2, F_2I, F_3I_2)

The calibration of the *ChargedCluster* model is relatively difficult in comparison to other, simple cluster models, because the *ChargedCluster* model offers several model parameters for each cluster size, and therefore a large total number of model parameters.

15.2 BIC model

The *ChargedCluster* model has been calibrated for BICs.. The final calibration of BIC formation energies has been performed by an automatic parameter optimization with *Sentaurus Workbench*, based on a selection of more than 20 B SIMS profiles including a range of industry-relevant process conditions with a focus advanced pMOS ultra shallow junctions. The calibration result has been successfully tested against a set of more than 100 B SIMS profiles and sheet resistance data, including data for USJ formation by flash lamp annealing [136].

The calibration has been integrated into the so-called *AdvancedModel*s section of the *Advanced Calibration* set of models and parameters. Compared to the standard model for B activation, the

calibrated BIC model gives significantly better results for B activation for low temperature processes, and for spike anneals or millisecond anneals with very small thermal budget.

From application perspective, the disadvantage of the BIC model is, that many equations need to be solved, which increases the CPU time for process simulation task. Six equations need to be solved for the six BICs included. In addition, the highest accuracy with the BIC model is only obtained, if it is combined with the ATOMICS model for interstitial clustering kinetics, which is accurate but needs seven equations to be solved for interstitial clusters.

Within ATOMICS, attempts were made to reduce the number of BICs used in the *ChargedCluster* model from six to four. A calibration with only 4 BICs has been published [137] by IISB in collaboration with Mattson and Synopsys. In this work, a good agreement between simulations and experimental data has been obtained for literature data on thermal annealing of high dose B implants at 800 °C and 900 °C, and for spike anneal and flash lamp anneal data for B USJ formation. In this calibration a very strong dependence of BIC formation energies on the temperature was assumed. According to Schermer[5], the formation energy for the B_3I_2 cluster should vary from -0.44 eV at 800 °C to +0.78 eV at 1050 °C, which corresponds to a change in cluster equilibrium concentration by a factor of $e^{1.22eV/kT}$, which is about 10^5. While it may be plausible that the formation energy of clusters is a function of temperature, such a pronounced change appears unlikely to be correct. Therefore, the calibration with six BICs and temperature independent cluster formation energies is favored by Synopsys.

An attempt by Synopsys to achieve a good calibration of the BIC model with only 4 BICs and temperature-independent cluster formation energy did not arrive at the accuracy obtained with the calibration based on 6 BICs.

15.3 F diffusion and cluster model

An accurate but general enough model for F diffusion and clustering was developed within ATOMICS. Compared to other F models such as the *Advanced Calibration* model used until 2008 or Diebel's model [138], the new model is more complex but also more accurate for a wider range of experiments. The earlier F model of *Advanced Calibration* doesn't model the F diffusion or clustering, but assumes a direct influence of F on B diffusion by modification of the B diffusivity. Diebel's simplified model includes the solutions for interstitial F and one cluster type F_3V, which reacts with I to decay into 3 F.

According to *ab initio* calculations [139], F tends to stay in the interstitial position due to a strong interstitial F binding. In the context of the five-stream diffusion model *ChargedReact*, this means that the neutral component of *ChargePair* is set to a relatively high value, leading to higher interstitial F (*FluorineInt*) concentration than the substitutional F (*Fluorine*) concentration in general. Moreover, the literature indicates that interstitial F prefers to decorate vacancies to form so-called F vacancy clusters. In the framework of the *ChargedCluster* model in which substitutional impurities cluster with silicon point defects, these clusters of interstitial F atoms and vacancies (that is, e.g., Fi_3V) result in F interstitial clusters (that is, F_3I_2) through the following relation:

$$Fi_3V <=> F_3I_3V <=> F_3I_2$$

In the ATOMICS F model, the allowed cluster types are F_2, F_2I, and F_3I_2 with formation energies taken from *ab initio* calculations[6].

The initial conditions of F after ion implantation are mainly interstitial F for crystalline silicon and partially clustered in F_2I, and F_3I_2 in recrystallized silicon. The three-phase segregation model is selected as the Si/SiO_2 interface model for F with parameter values allowing for strong dose loss.

The procedure *AdvancedFluorineModel* of *Advanced Calibration* C-2009.06 defines the physics-based model for F diffusion and clustering in silicon. It can be used in combination with both models for interstitial clusters, that is, the default *1Moment* model and the *Full* model of the *AdvancedModels* set.

Figure 77 shows the simulation results of the ATOMICS F model and Diebel's model for an example of an amorphizing F implantation and spike anneal, where both models have comparable accuracy.

The B activation enhancement and diffusion retardation in presence of F is more accurately simulated with the new model, see Figure 78. The interaction of F with B is indirect; trough the consumption of interstitials by pairing and clustering with F, fewer interstitials are available for B deactivation and diffusion.

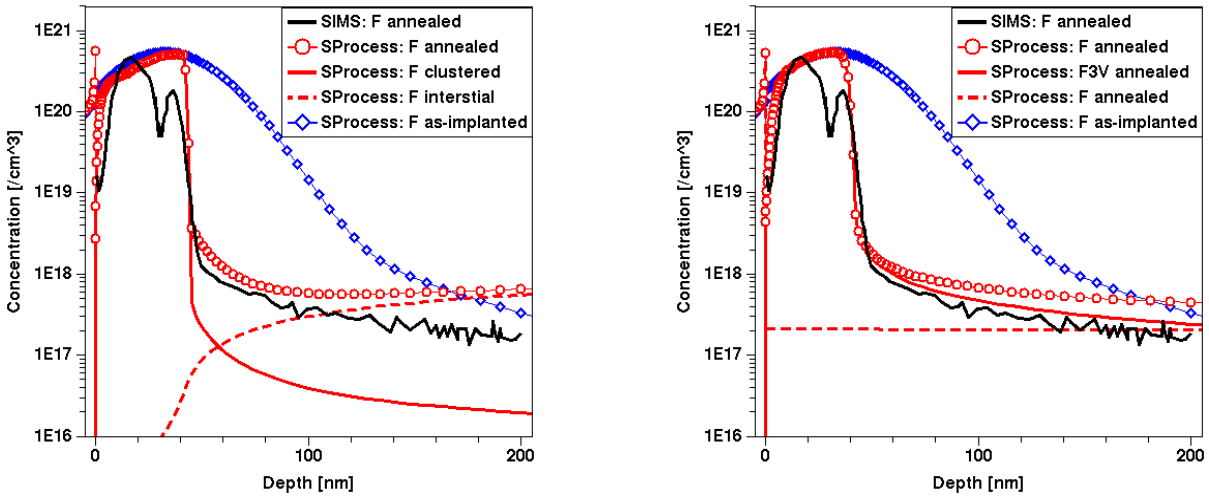

Figure 77: SIMS [140] profiles of F (F 20 keV 3e15 cm^{-2} implant in Si, 1050 °C spike annealed) compared with simulated profiles of the new F model (left) and Diebel's model (right).

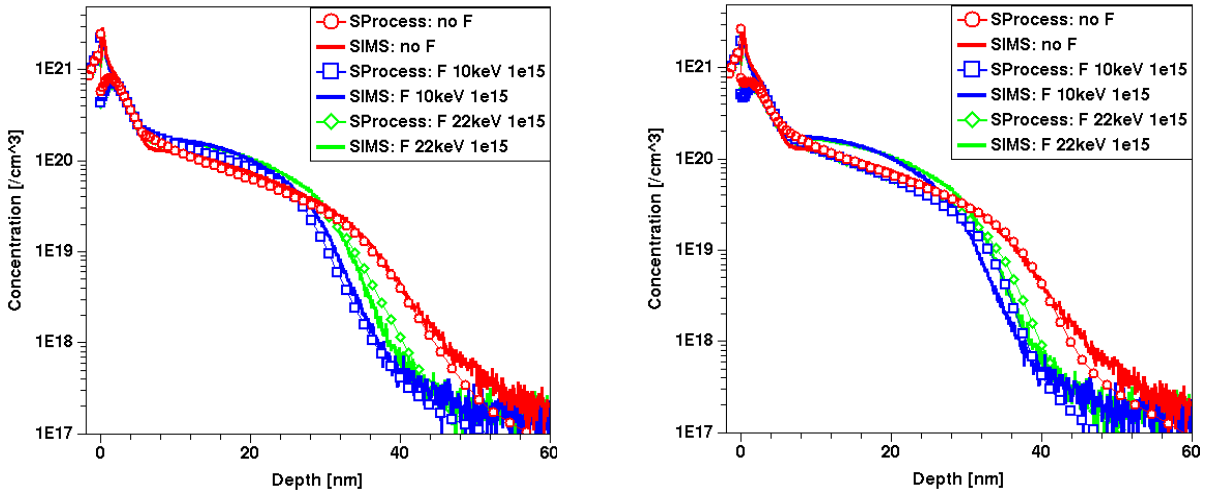

Figure 78: SIMS [141] profiles of B (B 0.5 keV 1e15 cm^{-2} implant in Ge pre-amorphized Si, with and without F co-implantation, 1050 °C spike annealed) compared with simulated profiles of the new F model (left) and Diebel's model (right).

15.4 B dose loss in presence of F

In addition to the indirect influence of F on B by its interstitial consumption, we model a direct F interaction with B for dose loss. On one hand, enhanced B diffusion in Ox in presence of F is modeled. On the other hand, two F atoms located in the Si/SiO_2 interface are allowed to cluster with a B atom, resulting in an F-dependent B dose loss. In the presence of F, some B atoms in the interface cluster with F, thereby freeing interface traps for single B atoms. This leads to an increased total number of B traps in the interface and, therefore, a stronger B dose loss. The interface trap density, emission, and trapping rates, and the cluster formation and dissolution rates have been calibrated by Synopsys based on SIMS

data. The *Sentaurus Process Alagator* scripting implementation of the B-F cluster formation at Si/SiO_2 interfaces is part of the procedure *AdvancedFluorineModel* of *Advanced Calibration*.

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16 Advanced SIMS analysis

During the project, CSMA has successfully fulfilled the SIMS requirements for the project, delivering in excess of 500 SIMS profiles for the various workpackages.

The project requirements dictate SIMS resolutions of the order ~ few nm for reliable measurement of diffusion of B, As, Sb in silicon, silicon germanium and in pure germanium for the various tasks.

The SIMS analysis thus requires the use of ultra low energy beams (500- 1000 eV) of either O_2^+ and Cs^+ ions (depending on the species being analysed), to minimise the pre-equilibrium region, in order to allow accurate quantification the SIMS data in the near surface region. Furthermore the use of low energy beams (under non-roughening conditions) will minimise the ion beam mixing effects resulting in SIMS decays of ~ few nm for high resolution measurement of diffusion and segregation effects .

A major challenge, from an analytical view point, is to minimise the ion induced roughening effects in SIMS under low energy sputtering conditions. These effects are generally a consequence of the sputtering process, influenced by the chemistry of the surface and the angle of incidence and the primary beam species ;these effects also occur more severely under low energy oxygen bombardment rather than when using caesium. In general, ion induced evolution of topography is negligible under normal (or near normal) incidence sputtering conditions. However, normal (or near normal) incidence conditions are not always possible or convenient especially when using magnetic sector SIMS instruments and hence in such cases protocols have been developed, using oxygen flooding conditions which also minimise the ion induced roughening effects under O_2^+ irradiation conditions .

The measurement of As and Sb require different analytical conditions to that of B. For these measurements Cs bombardment conditions are more appropriate (i.e. rather than O_2 for B analysis). The utilisation of protocols making use Cs primary beams and detection of the Cs_2M^+ secondary cluster ions for quantification has provided the key benefits for reliable quantification for these dopants and matrix elements (e.g. . Ge in SiGe); furthermore the low energy ion impact energies (500 -1000 eV) under these conditions have also resulted in excellent SIMS decays for high depth resolution measurements required for these cases. When appropriate we have taken account of the differing erosion rate SiGe (cf. silicon), when analysing SiGe to provide an accurate depth scale for the measurements.

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17 Electrical characterization of the lateral doping distributions in MOSFETs

A tight control of the doping distributions in the modern state-of-the-art CMOS transistors is a must. This is because of a high sensitivity of the basic performance parameters of the deeply scaled MOS transistors to the distribution of the doping in both source/drain and in the channel region. It is well known that the junction depth of the source/drain extensions impacts the short channel effects. The lateral position of the pn-junctions between the source/drain extensions and the channel determines the effective electrical gate length of the MOS transistor as well as the overlap capacitances between the gate electrode and the source and drain electrodes. The lateral position of the doping profiles in the modern state-of-the-art MOSFETs have to be controlled with an accuracy of few nanometers. There are

a number of methods to measure the depth profiles of the doping in silicon with such accuracy. In contrast, a measurement of the lateral distributions of the doping in MOS transistors is complicated and requires special measurement methods on specially prepared samples. In this project, we investigate the possibilities of the electrical measurements to control the lateral doping distributions in scaled MOS transistors.

17.1 The principle of the electrical characterization method

The method suggested in this work is based on a set of samples fabricated under identical conditions in which the gate length of a MOS-transistor-like test structure is varied. As schematically shown in Figure 79, the variation of the gate length leads to a progressive overlap of the source and drain profiles, and associated source and drain depletion regions. This overlap changes significantly the electrical properties of the test structures which can, in turn, be used to characterize the lateral dopant profile.

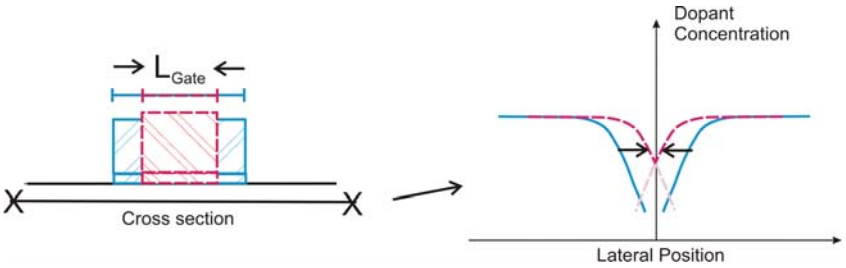

Figure 79: Schematic representation of the variation of the gate length of a MOS-transistor-like test structure on the lateral dopant concentration.

As alternatives, the influence of the overlapping profiles on the gate capacitance and on the drain current was investigated by device simulations using Sentaurus TCAD [142]. It turned out that the influence on the drain current is much more pronounced. Since measuring currents is usually less problematic than measuring capacitances for our structures, the best suited experimental set-up is shown schematically in Figure 80.

Apart from the varied gate length, the test structures on which the electrical measurements are performed have the same geometrical shape as the MOSFET for which the lateral source/drain doping profile should be characterized. To separate the effects of inhomogeneous source/drain and channel doping, a uniformly doped channel is used. The doping distributions in the source and drain regions are formed by ion implantation and annealing to activate the doping. To characterize the lateral doping distribution, we suggest measuring the electrical current I_{Leak} between the source and the drain electrode at a small source-drain voltage V_{DS} while keeping the gate voltage V_{GS} constant at a level that is close to the flat-band-voltage for this test structure.

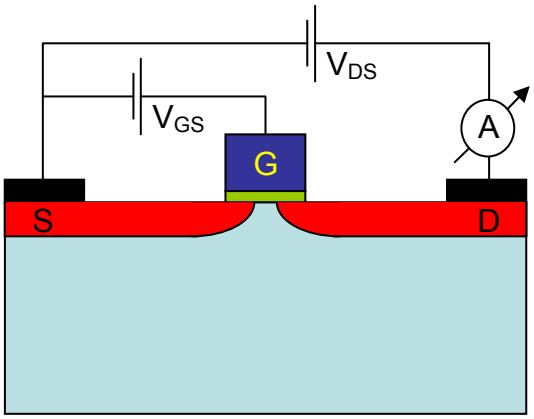

Figure 80: Scheme of the electrical measurement to characterize the lateral doping distribution in MOSFETs.

As mentioned above, the measurements of the drain current have to be performed for several gate lengths of the test structure shown in Figure 81. Since for different physical gate lengths different electrical gate lengths of the test structure will be realized and the drain current increases for smaller electrical gate lengths it is expected that the drain current will be a good indicator of the lateral vicinity of the source and drain doping. Besides, an additional increase of the drain current is expected when the source and drain doping profiles overlap so that the electrical carrier concentration increases at smaller physical gate lengths.

A first analysis has been performed on a simple architecture of a MOSFET using accurately calibrated models for the simulation of the rapid thermal annealing (*RTA*) [143,144] which were applied for the simulation of the doping distributions in the transistors considered. Figure 81 shows the results of the simulations for the source-to-drain current in a p-channel MOSFETs-like test structure with boron doping in the source and drain and a uniform arsenic doping of 10^{17} cm^{-3} in the channel.

As expected, the drain current depends strongly on the transistor gate length. It changes by about 9 orders of magnitude when the gate length is varied from 25 to 110 nm. This indicates a high sensitivity of the suggested measurement to the lateral position of the source/drain doping. A similar sensitivity can be expected when the separation of the source and drain is originated from the thermal diffusion of the lateral doping profiles. In the simulations shown in Figure 82, the lateral profile shape has been varied by changing the peak temperature during post-implantation annealing. Even the effects of an increase by 10 K are well represented in the electrical characteristics and shifts in the p-n junction depth by 2 nm are well resolved.

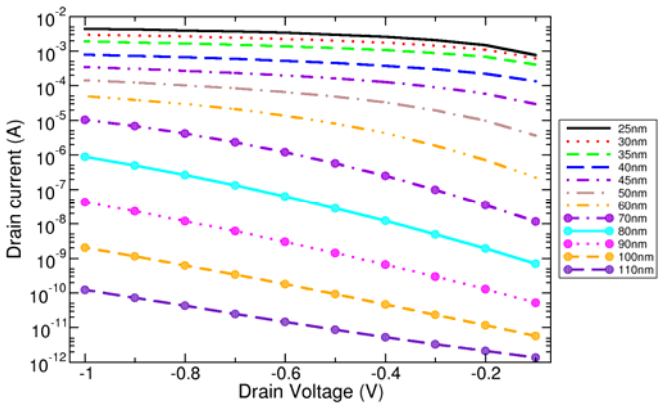

Figure 81: Drain current as a function of drain voltage in PMOSFETs with different gate lengths (device width is 1 µm) at a gate voltage of +0.6 V

The method presented here is based on I_{Leak} measurement for different device lengths and permits to estimate lateral doping profile shape.

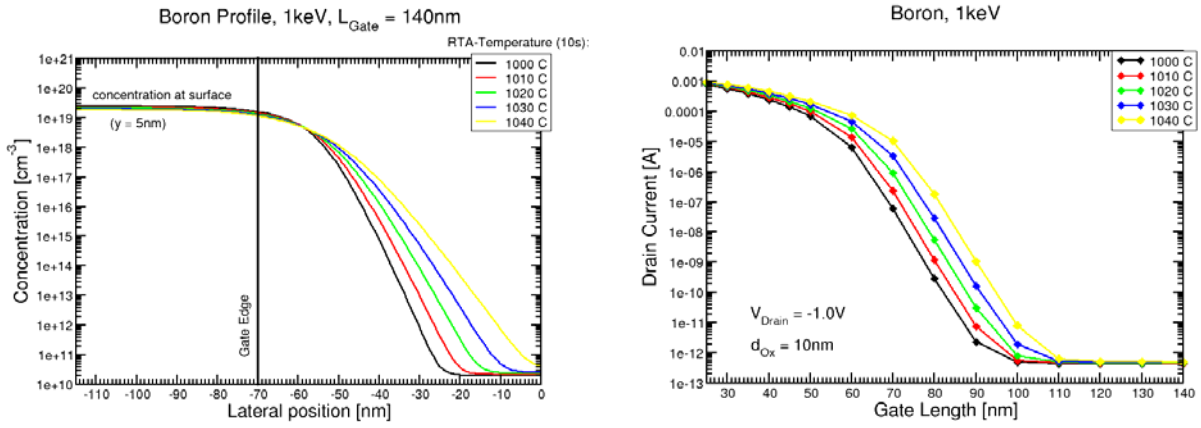

Figure 82: Doping profiles obtained by varying the RTA peak temperature (left) and effects of the varied lateral penetration depth on the electrical characteristics of the test structures (right)

17.2 Application of the method for an industrial 65 nm NMOS bulk silicon process

A generic process flow of 65 nm drawn gate length bulk silicon MOSFET devices is taken to illustrate the feasibility of the characterization method on fabricated devices. This process flow is adapted to simulate NMOSFET devices with gate lengths ranging between 90 nm and 35 nm. TCAD process simulations are performed with SPROCESS SYNOPSYS process simulator [40] including state-of-the-art diffusion models calibrated for ultra shallow junction (*USJ*) [145] as described in detail in [146].

This generic process flow includes main advanced CMOS process steps such as: 15 nm thick oxy-nitride gate dielectric; Standard retrograde well implantations including $V_{T\text{-}adjust}$ and Anti-punch-trough implants, followed by standard rapid thermal processing *RTP*; L_{dd} and Source-Drain implants; and a spike anneal at 1050 °C is performed for dopant activation at the end of the process flow.

2D net-doping distribution obtained by TCAD is depicted in Figure 21. In this NMOSFET device, L_{dd} junction steepness is about 2-3 nm/dec along channel direction and Source/Drain junction steepness is about 10 nm/decade vertically.

As presented in previous sub-section, the characterization method is based on the measurement MOSFET current leakage resulting from punch-through mechanism. The electrical characteristics are simulated ramping drain voltage with V_{gate} near flat-band voltage in order to avoid any carrier redistribution due to gate biasing. MOSFET devices with various gate lengths ranging from 90 nm to 35 nm are simulated and resulting electrical characteristics are shown in Figure 22, for NMOSFET device width of 1 µm.

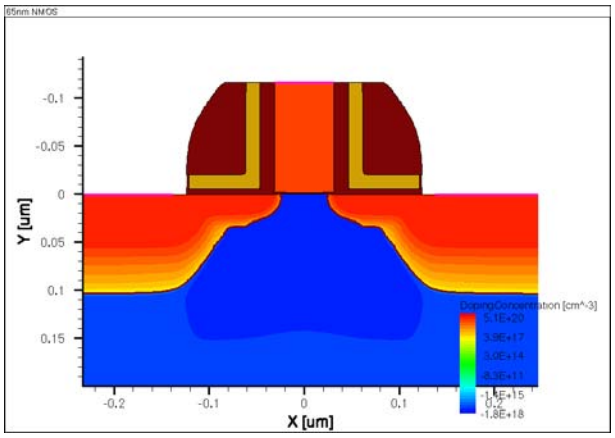

Figure 83: 2D net doping concentration of TCAD simulated NMOS.

The device simulations of the NMOSFET are based on Drift-Diffusion model that includes state-of-the-art models for advanced CMOS devices but excludes band-to-band tunneling (*B2B*). Quantum mechanical effects are neglected as well as possible velocity overshoot because these effects can be disregarded in the regime of interest. Figure 84 demonstrates the strong influence of gate length over drain current in this full NMOSFET TCAD process simulation case including all main process steps and validate the principle of the method. This validation is important because this process flow of NMOSFET includes retrograde p-well (with Anti-punch-through) and pocket implants leading to high boron concentration in the channel, thus limiting the leakage between Source/Drain junctions.

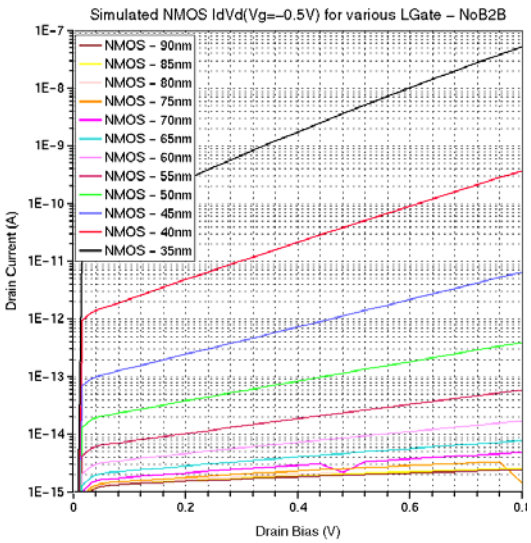

Figure 84: TCAD simulated Id-Vd characteristics (Vg= -0.5 V) for various NMOSFET (Channel width=1 µm)

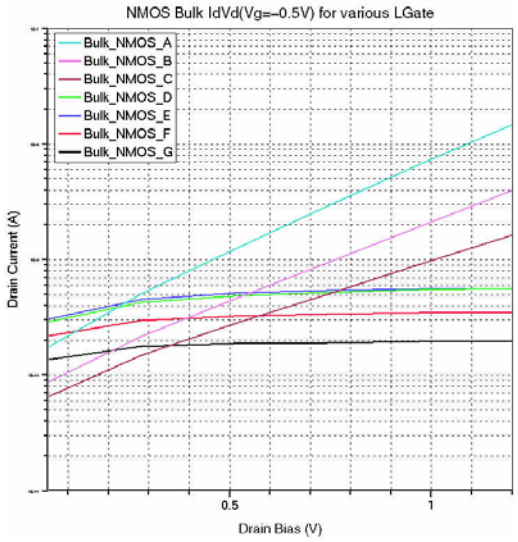

Figure 85: Measured 65 nm NMOSFET Id-Vd characteristics (Vg=-0.4 V)

In order to avoid any influence of the band-to-band tunnelling mechanism that might take place in the device, the leakage current monitored is not at $V_d=V_{dd}$ even if the characterization sensitivity would be maximized in those bias conditions. Thus, the output of interest is the leakage current I_{Leak} (I_{drain} @ $V_g=V_{fb}$, V_d= 0.4 V).

In Figure 23, the I_d-V_d (V_g=-0.4 V) characteristics are shown for various gate-lengths ranging from 55 nm to 10 µm corresponding to A, B, C… and G lines in an increasing sequence of gate lengths. The electrical characteristic allows demonstrating the leakage current exponential increase for short gate-lengths as described in previous section. Furthermore, we observe in Figure 23 an unexpected effect for low drain biases resulting in lower drain currents for short L_{gate} devices than for large ones. This is induced by the redistribution of boron pocket/well implants in case of short channel devices, so-called reverse short channel effect (*RSCE*) in N-type MOSFET. The observed non-monotonous increase of the leakage currents, which can be qualitatively explained by the overlap of the pockets for smaller gate lengths, have to be investigated in some more detail. Since in the real bulk silicon process we found a strong RSCE coming from the pockets in the channel, MOSFET samples without pockets should be used, if characterization of the source/drain extensions is envisaged. However, the method showed its ability to distinguish differences in the doping distributions which appear, if the annealing temperature was changed by only a few degrees. Furthermore, qualitative information on the lateral doping profiles can be extracted from the comparison of the electrical characteristics.

The example presented above shows that a method for electrical characterization of the lateral distribution of the active doping in CMOS devices is established. The method has been verified using numerical TCAD simulations and its sensitivity to process fluctuation has been evaluated. Electrical measurements on a real NMOS of the 65 nm demonstrated its high sensitivity and indicated potential difficulties of interpretation on devices with the non-uniform doping distributions in the channel.

17.3 Application of the method for the evaluation of SOI interface recombination effect

The influence of the Si/BOX interface on interstitials point defects evolution and dopants diffusion is investigated by comparing the standard 65nm CMOS process applied to a Bulk and a PDSOI substrate by means of TCAD simulations. Using a State-of-Art simulation set-up including the advanced diffusion and activation models developed in the frame of EC project ATOMICS, and more specifically, the recently developed model of interstitial point defects recombination at the Si/BOX interface is considered, a different lateral diffusion of dopants is seen in the active region of the CMOS devices.

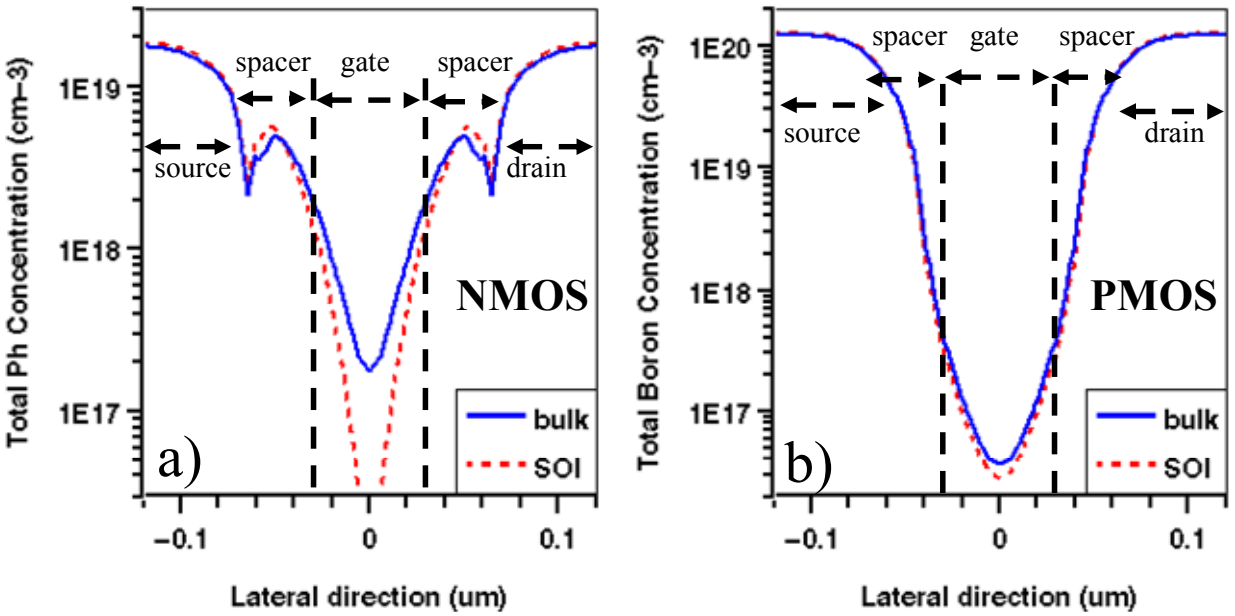

Figure 86: Horizontal cut at a depth of 30nm below the Gate Oxide of PD-SOI (red line) vs. bulk Si (blue line): a) Lateral active phosphorus concentration, b) Lateral active boron concentration.

The effect of the different lateral diffusion of dopants in Silicon in presence of a second Si/SiO2 interface induce a difference in the Drain Current characteristics studied in our methodology that is more sensible in NMOS devices as seen in next Figures.

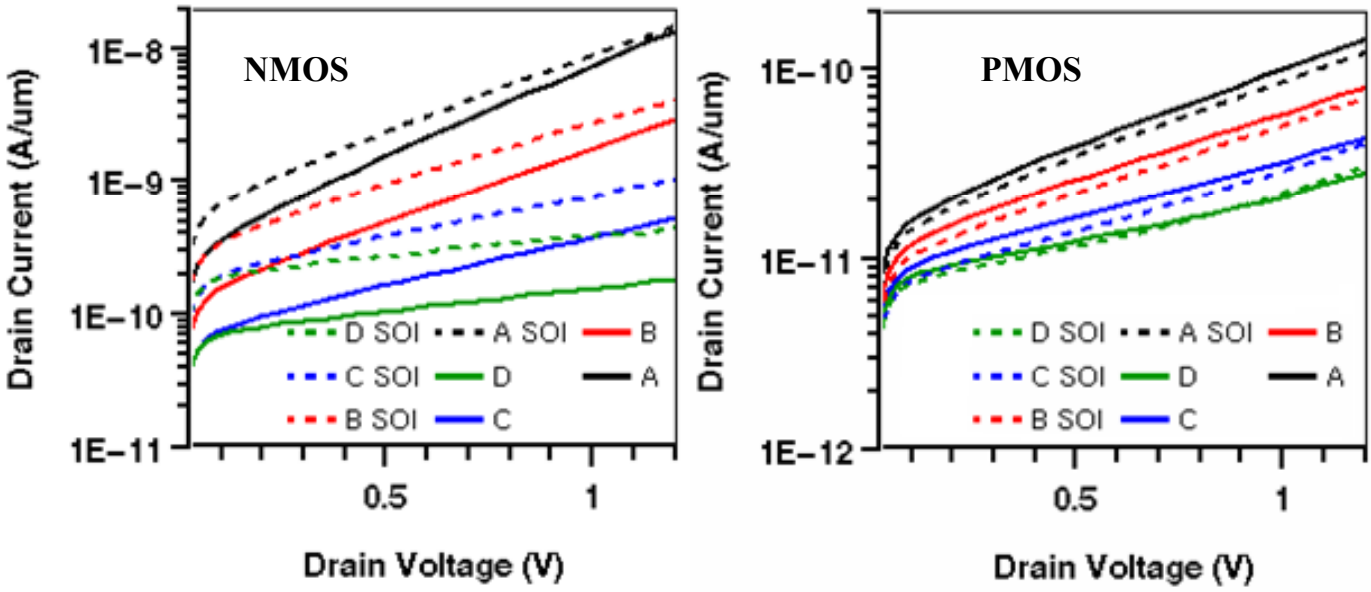

Figure 87: Bulk Si (solid lines) vs PD-SOI (dashed lines) I_d-V_d (Width=2.5 um) simulated characteristics.

Thus, the application of the developed methodology to standard PD-SOI MOSFET devices and the comparison with equivalent bulk Si device demonstrates the impact of the Si/BOX interface on Extended defects distribution, on dopants profiles and on the static electrical characteristics.

17.4 Complementary studies using the method

The developped methodology is a powerfull tool to help TCAD calibration and the analysis of process variations.

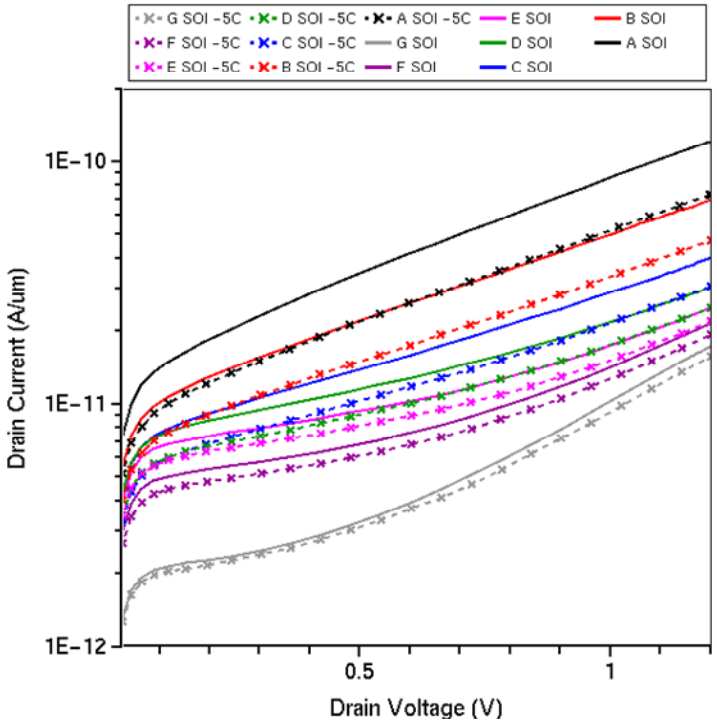

Figure 88: Impact of a 5°C difference of the Spike annealing temperature on the punch- trough currents of PMOS PD-SOI devices.

Moreover, the usefulness of the characterisation methodology is illustrated in Figure 88 where the sensibility of the method to lateral diffusion profiles variations was tested to study the impact of a slightly different thermal process on PMOS devices.

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18 Early use of models in European projects

Due to the continuous scaling of CMOS devices, the usage of rapid thermal annealing (RTA) schemes and millisecond annealing (MSA) schemes is essential. Conventional bulk MOSFETs require very shallow junctions at high active doping concentrations, to suppress short channel effects and reduce source/drain access resistances. The usage of fully depleted silicon on insulator (FD SOI) MOSFET, on the other hand, eliminates the challenge of very shallow junctions, as the diffusion of dopants is limited by the silicon body thickness. However, due to un-doped channels used in FD SOI MOSFETs, the source/drain extension overlap below the gate-stack is hard to control by using conventional annealing schemes. Further, as in conventional bulk MOSFETs, a high active doping concentration of the source/drain extensions is required in FD SOI MOSFETs to reduce access resistances. Therefore, the usage of RTA and MSA schemes is essential in FD SOI MOSFETs, too. Additionally, the problem of continuously increasing source/drain Schottky contact resistances at decreasing device dimensions has to be taken into account, as well in conventional bulk MOSFETs as in FD SOI MOSFETs. As the source/drain Schottky contact resistances depend on the active surface doping concentration at the metal/silicon interface, RTA and MSA schemes can help to efficiently reduce contact resistances.

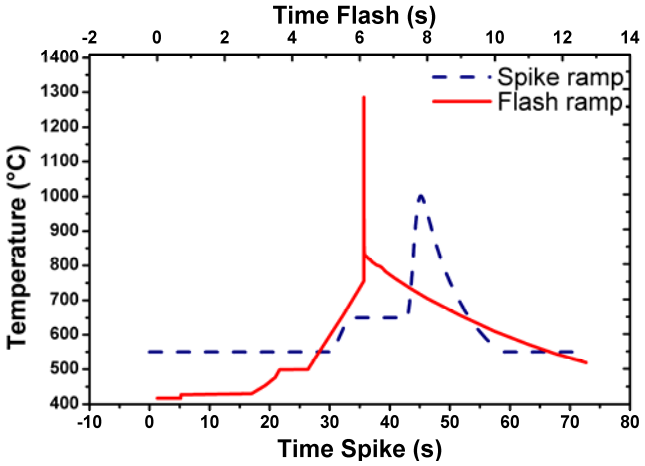

Figure 89: Temperature ramp of spike and flash annealing used in process simulations

To investigate the advantages of using RTA and MSA annealing schemes (Figure 89) in CMOS device processing, process and device simulations of various promising device architectures were performed in the IST Integrated Project PULLing the limits of NANOCmos electronics PULLNANO (IST-026828). For that, a calibrated version of a model developed within ATOMICS for simulating activation and diffusion of arsenic [147,148] was transferred early to the subproject SP3 of PULLNANO. There, based on the likewise transferred RTA and MSA annealing recipes from Mattson Thermal Products, it was used for simulating the effects of the respective annealing schemes on activation and distribution of dopants. Device simulations were done in PULLNANO SP3 to exhibit the impact of the different annealing schemes on the final MOSFET performance. Finally, SPICE models of the different annealed MOSFETs were extracted in PULLNANO SP6 to investigate the impact of RTA and MSA schemes on the circuit behavior. Some results of PULLNANO SP3 and SP6 are presented below, to demonstrate the necessity of using extended activation and diffusion models for simulating the influence of RTA and MSA schemes on the electrical MOSFET performance.

18.1 Process Simulation Results

To demonstrate how RTA and MSA schemes influence on the electrical performance of FD SOI MOSFETs, process simulations were performed using temperature ramps presented in Figure 89 and extended models for activation and diffusion of arsenic. For that, a FD SOI MOSFET with 21 nm gate length, 1 nm gate oxide thickness, 5 nm silicon body thickness and 10 nm buried oxide thickness was used (Figure 90). At final stage of processing, four annealing schemes were applied to the device: spike annealing, spike followed by flash annealing, flash annealing and flash followed by spike annealing. After the process simulation, the lateral active arsenic doping concentration was observed. Figure 91 shows the lateral doping profiles, extracted 1.5 nm below the gate oxide. As seen, the flash annealing (triangles) and the flash annealing followed by spike annealing (solid line) results in a desired abruptness of the source/drain extensions. The lateral shape of the active arsenic doping concentration resulted from the spike annealing (squares) and spike annealing followed by flash annealing (circles) is smoother, compared to flash and flash+spike and does not undercut an active arsenic doping concentration of 7×10^{17} cm^{-3}. Aiming at low leakage currents and short channel effects, the flash and flash+spike might be, from a technological point of view, more beneficial, compared to spike annealing and spike+flash annealing.

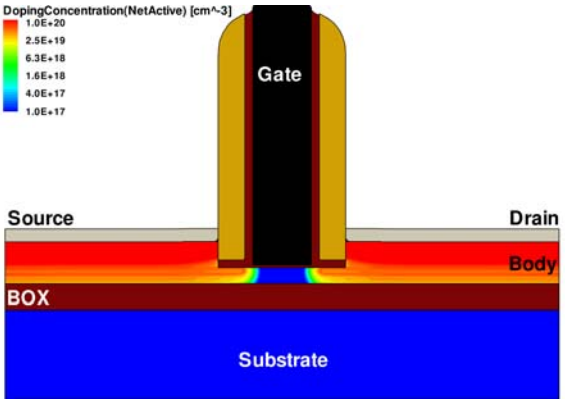

Figure 90: Fully depleted silicon on insulator (FD SOI) MOSFET

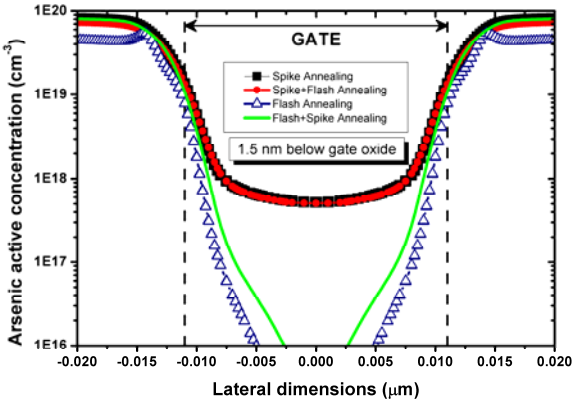

Figure 91: Lateral arsenic active concentration resulted from four different RTA and MSA schemes

18.2 Device Simulation Results

Numerical Drift-Diffusion simulations were performed to investigate the electrical behavior of FD SOI MOSFETs by using different RTA and MSA schemes in the process simulations. Figure 92 shows the output characteristics of the FD SOI NMOS (Figure 90) for different annealing schemes. It has to be mentioned that Schottky contact resistances were taken into account in the device simulation setup. As seen, the spike annealing followed by a flash annealing scheme (solid line) results in the highest drive current, followed by the flash annealed MOSFET (circles). Using spike annealing or flash annealing followed by a spike annealing schemes result in drive currents, which are approximately only a half of the drive current resulted from the spike+flash annealing. This can be explained by higher surface doping concentration, resulted from the flash annealing. As seen in Figure 93, as well the I_{on}-I_{off} behavior of the flash annealed and spike+flash annealed devices over performs the I_{on}-I_{off} behavior of the spike annealed and spike+flash annealed devices applicable.

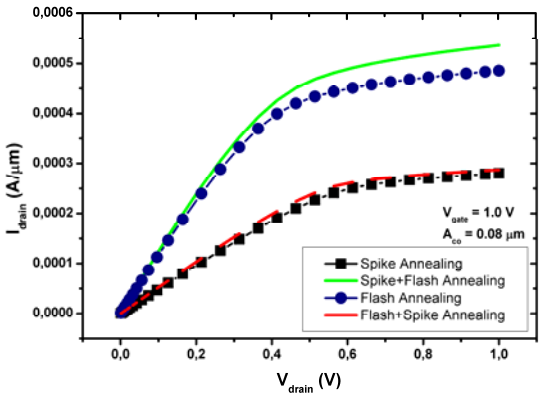

Figure 92: I_d-V_d characteristic of the FD SOI NMOS using four different RTA and MSA schemes

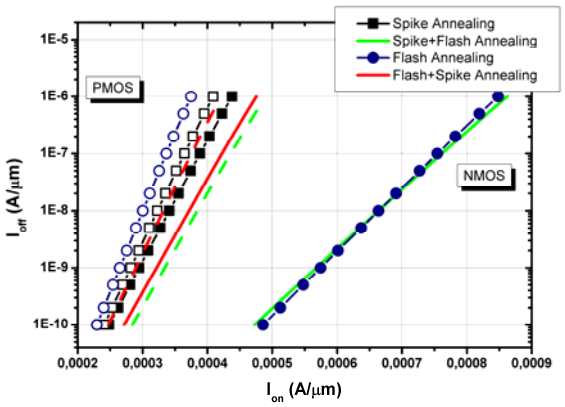

Figure 93: Ion-Ioff behavior of FD SOI MOSFETs using four different RTA and MSA schemes

18.3 Circuit Simulation Results

SPICE parameters of the flash annealed and spike+flash annealed devices were extracted to investigate the circuit performance of RTA and MSA annealed devices. For that, a pulsed voltage source was applied to the input of a simple inverter stage. After that, the rise and fall times of the output signal was calculated by the difference of the output to input signal at 0.5 V. The flash annealed inverter (Figure 94

(dashed line)) results in t_{fall} = 9.2 ps and t_{rise} = 7.6, while the spike+flash combination speeds up the circuit (t_{fall} = 8.4 ps, t_{rise} = 5.5 ps) (Figure 95, dashed line).

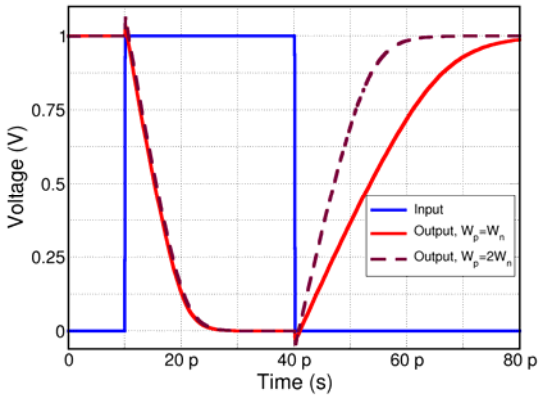

Figure 94: Dynamic inverter performance using flash annealed CMOS devices

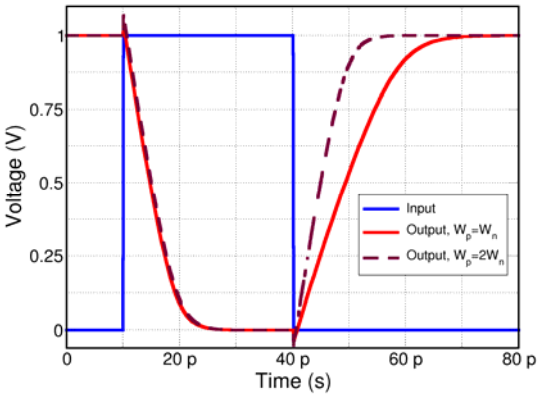

Figure 95: Dynamic inverter performance using spike+flash annealed CMOS devices

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