Fraunhofer Institute for Integrated Systems and Device Technology IISB
Schottkystrasse 10
91058 Erlangen, Germany
www.iisb.fraunhofer.de

Dr. Martin Schellenberger
Phone: +49 9131 761 222
Fax: +49 9131 761 72222
E-mail: martin.schellenberger@iisb.fraunhofer.de

Contact

Fraunhofer Institute for Integrated Systems and Device Technology IISB
Schottkystrasse 10
91058 Erlangen, Germany
www.iisb.fraunhofer.de

Dr. Martin Schellenberger
Phone: +49 9131 761 222
Fax: +49 9131 761 72222
E-mail: martin.schellenberger@iisb.fraunhofer.de

Joint Development with

JENOPTIK Automatisierungstechnik GmbH

© Fraunhofer IISB | www.iisb.fraunhofer.de
PRINCIPLE OF TLS-DICING

Crack guiding by thermally induced mechanical stress.

Two-step process:

1. **Crack initiation** with diamond tip or ablation laser; a predetermined cleaving point defines the TLS start.

2. **Cleaving step** with laser heating and subsequent water cooling; high tensile stress inside the overlap zone between heating and cooling results in a complete cleaving of the substrate.

TLS PROPERTIES & BENEFITS

Zero kerf width
- More chips per wafer

High edge quality
- No chipping
- High bending strength

No recast, no residues
- No subsequent cleaning

High feed rates
- High throughput

Materials under investigation:
Si, SiC, mc-Si, Ge, GaAs, GaSb

EXCEPTIONAL QUALITY

1-pass dicing of Si-wafers
- Successfully tested up to 925 µm thickness

Fast resizing of Si-wafers
- Bare and processed Si-wafers, e.g., 450 mm to 300 mm
- Process time below 1 min

High-speed and high-quality dicing of 4H-SiC
- Feed rates up to 200 mm / s
- No chipping