

# FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB



1 Printed TFT gate electrodes on flexible foil substrate

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# THIN-FILM MATERIALS FUNCTIONALITY FROM INKS

## Introduction

Fraunhofer IISB offers services along the entire process and value chain of printed electronics fabrication, covering

- ink formulation and analysis,
- thin-film deposition and characterization, and
- device and application development.

At Fraunhofer IISB, several dedicated laboratories for printed electronics as well as a cleanroom facility fully equipped for 200 mm CMOS processing are available. For the handling of air sensitive materials, Fraunhofer IISB runs a glove-box line providing the complete process flow of ink formulation, film deposition, annealing, metal deposition, and electrical characterization without breaking the inert atmosphere. In addition, strategies for the handling in ambient air are available for air-sensitive materials. Experienced operators, engineers, and scientists perform service and development tasks.

### Ink formulation

Functional nanoscale materials for printed electronics can be synthesized by gas-phase synthesis or wet-chemical precipitation. For ink formulation, particles are milled, stabilized, and dispersed in organic solvents or water. Characterization of ink covers various aspects like viscosity, density and surface energy measurements. Handling and analysis can be performed in inert atmospheres or ambient air. In a second approach, molecular precursors, e.g. metal salts are formulated to give efficient inks for on-substrate conversion into metal salts. Special focus is paid to a high molecular concentration and the chemical conversion reaction.

# Thin-film deposition

Fraunhofer IISB offers several techniques for thin-film deposition from inks like spin coating, spray pyrolysis, ink-jet, and screen printing.



As interaction between substrates and inks is crucial for optimum printing results, our expertise in surface analytics and surface modification, e.g. via plasma treatment, can be contributed for process optimization.

Device and application development

Fraunhofer IISB offers services towards printed device and application development as well as the combination of printed thin-films and conventional thin-film processing. In the latter case, a range of low-temperature, glass- and plastic compatible techniques like plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), as well as sputtering techniques are available. Mixing of printing techniques and conventional technologies enables a broader range of processing capabilities (e.g. materials or tools), reference devices allowing material benchmarking, or test structures allowing rapid testing of new materials, and getting fast and reliable results.

For e.g. printed semiconductor characterization, preprocessed TFT, inverter, or ring oscillator devices fabricated in our clean room facility with customized layout are used.

For device characterization, standard and advanced electrical measurement techniques are offered. Additional services can be provided towards the integration of printed devices into systems. Printed devices are combined with standard devices like microcontrollers or FPGAs for demonstrator development addressing the benefit of flexible and inexpensive printed devices.

- 2 Formulated semiconductor ink
- 3 SEM image of cross section of a printed ZnO layer, prepared by FIB

4 Printed temperature sensor

#### Key techniques along the process chain for printed electronics

| Process Group                      | Techniques   | Characterization                       |
|------------------------------------|--|--|
|                                    | gas-phase or wet-chemical synthesis, ball<br>milling, high-speed centrifugation, precursor<br>formulation                                    |  |
|                                    | ink-jet, spin coating, spray coating, screen<br>printing, plasma treatment   | AFM, SEM, EDX, TEM, FIB, TEM, XRD, XPS |
| Device and application development | full 200 mm CMOS line, glovebox line, com-<br>bination of printed devices and conventional<br>electronics, pre-processing of test structures |  |