Zero Overvoltage Switching “ZOS”
Breaking the rules of parasitic inductance


1 Abstract

Turning off an electrical path is causing trouble by parasitic inductance since beginning of power electronics. Ages are spent to avoid oscillations and voltage overshoot while compromising on switching speed. Not only since new Wide Band Gap devices are available, a demand for new power modules and packages emerged and innovative low-inductance or resonant concepts have been introduced successfully. In contrast, the ZOS method offers a solution to unleash unlimited switching speed in real-world applications without overvoltage on the semiconductors. Moreover, in best case, it is even avoiding any subsequent parasitic oscillation. The idea is to use the intrinsic parasitic inductances and parasitic capacities to build up a resonant circuit. The turn off event excites the resonant circuit and the free-wheeling diode stops it automatically after half a period, e.g. after a view nanoseconds. These resonant parasitic elements are thereby utilized to switch off a fixed current in a lossless, overvoltage-, and EMI compliant way. By designing the circuit and parasitics properly, there is no extra component necessary and even relaxed industrial style semiconductor housings and low-budget capacitors can build up the circuit, as parasitic inductance is now functional part of the topology.

2 Explaining the ZOS Converter Circuit and Control Strategy

The technology focuses on the switching-off transient, which is causing problems in typical hard-switched topologies. To simplify the problem, only a classic boost converter, as seen in Fehler! Verweisquelle konnte nicht gefunden werden., is described to explain the ZOS approach.

2.1 Classic Turn-Off

$T_{\text{bot}}$ is turned on for a specific time to increase the phase current $I_{\text{ph}}$. During turn-off event, $T_{\text{bot}}$ faces a so called voltage overshoot, which is necessary to force $I_{\text{ph}}$ through the parasitic inductance $L_{\text{par}}$. In state-of-the art technology, $L_{\text{par}}$ should be as low as possible and switching speed of $T_{\text{bot}}$ needs to be limited to keep the max. voltage overshoot below all SOA limits. That is also true on a more relaxed situation where $T_{\text{bot}}$ is considered to have a parasitic or additional discrete capacitance $C_{\text{par}}$ in parallel.

2.2 The ZOS Cell

To convert the circuit to a ZOS Cell, the following design rules must be met. In best case, real components are already quite near to the optimum design by only little or no hardware changes. Figure 1 shows the parasitics which are now part of the topology. The lowside transistor $T_{\text{bot}}$ is sketched as an ideal switch $S$ next to additional (body-) diode and $C_{\text{par,bot}}$ and may represent a fast MOSFET for example.

- The parasitic capacitance $C_{\text{par,top}}$ of the active free-wheeling component should be near or equal to the low side parasitic $C_{\text{par,bot}}$. That is even true for typically non-linear capacities. This rule is very easy to achieve for half-bridge configurations by default.
- On a given hardware and parasitics, the phase current $I_{\text{ph}}$ at the turn-off point must be set according to following equation:

$$I_{\text{ph}} = \frac{U_{\text{ZK}} \sqrt{\frac{8}{\pi} C_{\text{par}}} \left(\frac{L_{\text{par}}}{L_{\text{par}}} \right)}{L_{\text{par}}}$$

- If phase current is given by the application, the designer may adapt the parasitics or add extra capacitors and inductors.

![Figure 1: ZOS Cell design](image1.png)

![Figure 2: Idealized ZOS transient wave-forms](image2.png)
The chips and/or the gate driver must be designed to turn off as fast and snappy as possible. That can be achieved e.g., by switching a 25 mΩ SiC MOSFET with a gate resistor RG of less than 1 Ω. Less speed will eliminate the ZOS effect.

Following these ZOS Cell rules, the ZOS effect occurs as follows:

Step 1: The channel S inside the transistor is shut off as fast as possible during \( t_1 \), which may also take several ns in physical devices.

Step 2: Output capacitance is charged by the phase current \( I_{ph} \) and thereby MP is rising. The parasitic top side capacity \( C_{par, top} \) shifts the level of its cathode K over the DC link voltage \( U_ZK \) without any overvoltage on \( T_{bot} \). Thereby \( i(L_{par}) \) rises and oscillation begins.

Step 3: The oscillation ends immediately after half a period at \( t_3 \) - exactly where the current \( i(L_{par}) \) is at its maximum. In an ideal setup, the maximum equals \( I_{ph} \) while \( u_D \) is zero at this point. Furthermore, the oscillator is stopped by the freewheeling diode, which simply shortens \( C_{par, top} \).

### 2.3 Simulation Experiment

One interesting ZOS showcase is a simulation experiment on varying the gate resistance \( R_{gate} \). Following classic theory, overvoltage can be reduced by increasing the gate resistor. Following the rules of ZOS Cell design, it is shown how overvoltage can be decreased against all expectations by lowering the gate resistance (and raising switching speed). By that approach, the losses can be cut down to about 2% of the nominal datasheet losses (in this simulation example) by applying an external \( R_{gate} \) of about 1 Ω (additional to the internal chip resistance) instead of 20 Ω recommended. The simulation turns off the optimum ZOS current of 84 A using the Cree SPICE Models, which are a good choice for transient simulations.
2.4 Measurement Experiment

Claiming overvoltage may disappear by increasing switching speed, adding parasitic inductance and ramp up the current is a very tough job resulting in disbelief and shaking heads. That’s why a proof of concept test setup was build.

The setup available has a drawback as 4.3 Ω gate resistors per chip (optimum would be below 1 Ω) are used inside the power module. To compensate this issue as far as possible, -10 V negative gate voltage (instead of -5 V) was applied to switch off faster.

A  Half bridge SiC module with 4x C2M0025120D per switch and 4x 10 A SiC diodes
B  Increased DC-Link inductance by adding about ~50 nH (2x100nH in parallel)
C  Test voltage 400 V DC U2x
D  Test phase inductor connected between MP and high side DC link
E  u_r measured by both Kelvin contacts SB and ST similar to Figure 4.

Figure 5: ZOS test setup SiC power module with DC-Link PCB and film capacitors

To proof that the ZOS effect exists, the current I_on was alternated by changing to on-time and thereby ramp up different current values. Figure 6 shows a turn off current of about 50 A. Figure 7 turns off at an even larger current of about 68 A but hitting ZOS operation point. The experiment can be done at different voltages, currents and parasitic inductances, all showing optimal ZOS point as long as the module is switched as fast as possible.
2.5 Further Key Aspects

The key point of these rules is the unlimited switching speed that allows cutting losses down to zero. Combined with classic Zero Voltage Switching (ZVS) during turn-on, it is possible to build up a real-world converter without significant switching losses at all.

Most applications need a power regulation. Several techniques allow set up average current while keeping optimum \( I_{\text{ph}} \) at turn-off point:

- Varying \( I_{\text{ph}} \) around optimal ZOS point is still sufficient, e.g. by ±5%
- Switch off phases on multi-phase designs would allow \( N_{\text{ph}} \)-step regulation
- Under recommended BCM operation, frequency can be reduced by Valley Skipping, enabling current reduction approximately by factor 2
- Finally, controlling power down to zero is always possible by classic burst-mode operation.

2.6 Applications

The ZOV technology can be used in every converter technology being able to control the current during the turn-off operation point. That is possible for nearly any classic isolated and non-isolated Buck-, Boost-, Forward-, Phase-shift, Flyback- and other DC-DC converters from zero watts Point-of-Load converters to megawatt switching cells. Even load regulation is possible, implementation is more easy for constant-power applications like LED illumination or on-board chargers.

A very interesting application is also a Flyback converter. In this case, the converter can use the stray inductance of the transformer and the secondary side diode to model the ZOS effect. As there is no overvoltage and oscillation, no RC, RCD, or active snubber is necessary.

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