An Isolating IGBT Halfbridge Driver with Embedded Magnetics

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Abstract
This paper describes the functions of a compact isolated IGBT halfbridge driver module which is built on PCB embedded magnetics. The whole driver is built in a package with the standard DIL-32 footprint. A unique feature for this small package is the gate drive power of more than 1W for each output channel. In addition, the driver is designed for an insulation voltage of 1200V. With this features no bootstrap circuit or an extra DC/DC converter is necessary. The new integration concept is based on a planar printed circuit board (PCB) transformer. Expensive wire wound cores could be replaced with an innovative method for magnetic flux guidance. For the transmission of the gate control signal and the gate drive power a modulated carrier signal in the range of MHz is used. The extension of this method by a feedback channel will be described. The galvanic insulated transmission of the gate control signal, gate drive power and diagnosis feedback signal is now possible by using a single inductive coupling element. The pros and cons of a PCB transformer in gate driver circuits are discussed. Theoretical investigations as well as comparative measurements of a version with a standard toroidal ferrite core are presented. The high reliability and robustness of the driver are shown with application oriented measurements.

Introduction

The gate driver concept presented in [1] is based on an inductive coupling between the primary and the secondary side of the driver. A single transformer is used to transmit the gate control signal and the gate drive power. One of the main advantages of our approach is the possible reduction in size.

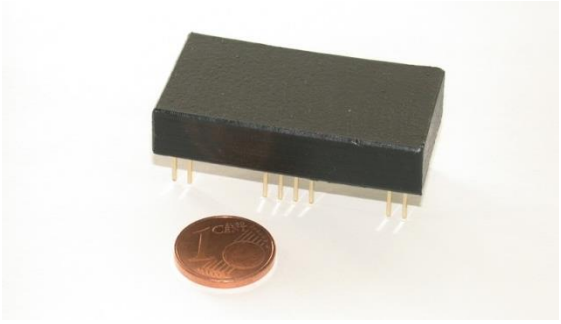

Figure 1: Intelligent insulating halfbridge IGBT driver in DIL-32 package with embedded magnetics

Figure 1 shows an intelligent insulated halfbridge driver, which is based on the proposed concept. Within the base area of a DIL-32 package the driver provides a unique functionality, like a galvanic isolation for DC link voltages up to 1200V or 1W gate drive power for each output channel.

In order to reach this high degree of miniaturization two main problems had to be solved. In a first step, nearly all the secondary side functionality has been integrated in an ASIC. This includes the decoder of the IGBT switching information. In the next step, the insulating transformer, which normally consists of a wire-wound toroidal core, was replaced by an integrated planar version. In the following these solutions will be illustrated and the results will be discussed.

Integration of the decoder and the feedback channel into an ASIC

Figure 2 shows the decoder block diagram for decoding the IGBT switching information at the secondary side of the driver as presented in [1]. The decoder is integrated in the secondary side ASIC.

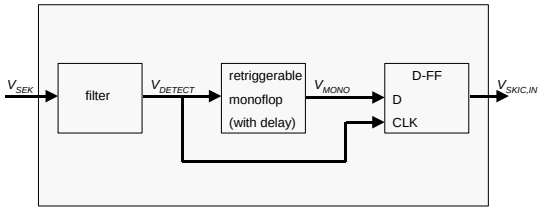

Figure 2: Decoder block diagram

An additional feedback channel has been implemented. The feedback is realized by means

of an heavy increase of the secondary side load. When a fault is detected, e.g. an IGBT overcurrent, the supply voltage at the secondary side is loaded by an additional ohmic resistor. The supply current of the primary side driver stage rises correspondingly, this can be easily monitored, e.g. by a shunt resistor. The oscillogram in Figure 3 shows the resulting waveforms.

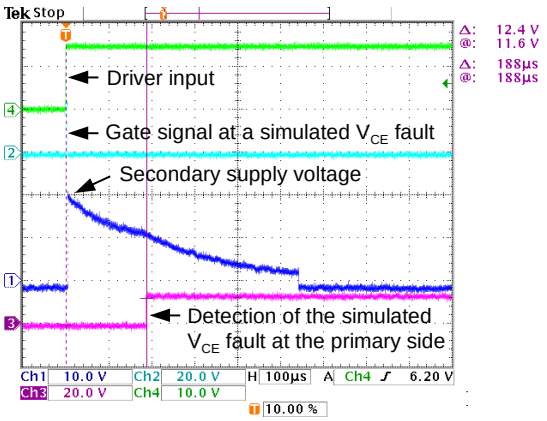

Figure 3: Fault detection and feedback

A delay of about 190µs between the simulated fault at the secondary side (Ch2) and the diagnostic feedback signal (Ch3) at the primary side is measured. By monitoring the peak value of the primary side supply current, the feedback delay time slightly depends on the total load on the secondary side. Table 1 shows the feedback delay in dependence of the gate switching frequency at a gate charge of 4.5µC:

Table 1: Fault detection delay time

f_{switch}	0 kHz	6 kHz
t_{detect}	<190 µs	<170 µs

With our new ASIC the following functions are provided:

- Decoding the IGBT switching information
- 2.5A peak gate drive current
- Negative off-state voltage
- Short circuit detection
- Independent turn-on and turn-off gate resistors
- Undervoltage detection
- Power-On reset
- Error memory
- Diagnostic feedback

Figure 4 shows the layout of the ASIC chip. The two large areas left below are the MOSFETs of the output stage, which provide up to 2.5A peak current for charging and discharging the gate.

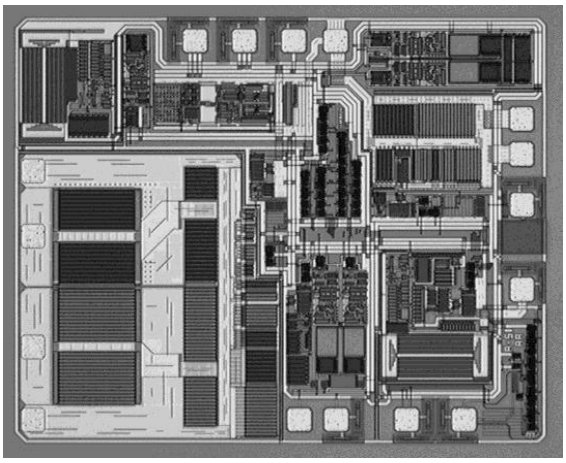

Figure 4: Secondary side ASIC SKIC1004BA (SEMIKRON)

The new driver concept has been applied in an intelligent power module (IPM), which is shown in Figure 5. This module is mechatronically integrated in an inverter drive for hybrid traction [2]. Placed between the combustion engine and the gear-box, the module must be able to work under very harsh environmental conditions especially with respect to temperature and EMI. During extensive tests, the new gate driver concept proved it´s unique noise immunity.

Figure 5: Intelligent power module, designed for a mechatronic integration in an inverter drive (600V/400A IGBT halfbridge)

The further investigations aimed on a cost reduction, a high volume manufacturability and a further reduction in size.

Planar transformers

Since many years the printed circuit board (PCB) based transformers have a good status in technology. In DC/DC converters they are commonly used in conjunction with E- or RM type cores. Compared to conventional wire-

wound cores, planar cores are easy to use but still to expensive and bulky for our applications. On the other hand, coreless transformers look quite attractive, but they are normally restricted on low-power transmission with very high frequencies.

In a planar coreless transformer, the windings are realized by one or several stacked spiral tracks on a PCB. The primary and secondary windings are separated by insulating prepreg layers. Such kinds of coreless PCB-transformers in gate drive applications are presented in [3] and [4].

Sandwich architecture

In order to meet our miniaturization targets, we have chosen a sandwich architecture. This means the planar transformer is placed between the primary and the secondary side electronics, like in a sandwich. However, this construction leads to large metal areas very close to the transformer windings, which results in a strong reduction of the inductance. Coreless transformers are therefore inapplicable in such kind of sandwich architectures.

The problem can be solved by using a ferrite polymer composed (FPC) foil, which provides a concentration of the magnetic field and shields the conducting layer (see Figure 6).

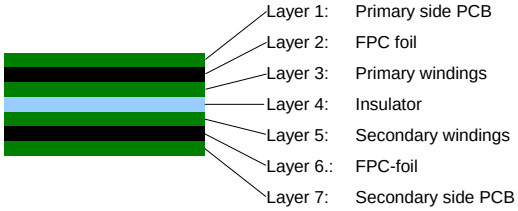

Figure 6: Layer structure with embedded magnetics

Figure 7 shows the effect of the FPC foil. The dependency of the primary inductance (measured with open secondary winding) in presence of the conducting layers and the FPC foil can be seen. Without the shielding effect of the FPC foil the value of L_{1l} is reduced down to one sixth compared to an unaffected air coil. Even though the permeability of the FPC is only about $u_r = 9$, the foil greatly reduces the influence of the copper areas.

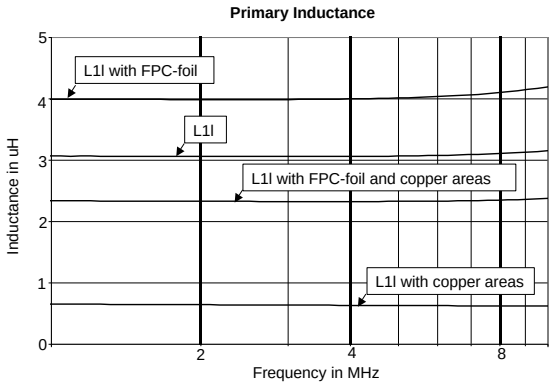

Figure 7: Primary inductance (open sec.) with FPC-foils for copper area shielding

Difference between toroidal core- and planar transformer

In the following the pros and cons of a driver with a toroidal core transformer (Figure 5) and a planar one (Figure 8) will be discussed.

Figure 8: Primary and secondary windings of the planar transformer

For experimental investigations we realized prototypes of both transformer types. The most important parameters of these are given in Table 2.

Table 2: Parameters of a toroidal core transformer and a planar transformer with embedded magnetics

Transformer		toroidal core	planar FPC-foil
Primary Inductance	L1l/µH	3.6	3.0
Secondary Inductance	L2l/µH	1.1	1.3
Permeability	u_r	125	9
Outside diameter	d_{max} /mm	11	16
Winding width	A_{cu} /mm²	0.09	0.009
Magnetic coupling	k_{avg}	0.95	0.79
Coupling capacity	C_{12} /pF	3	14
Max. power transfer (with driver)	$P_{sec,max}$ /W	1.5*)	1.0*)

*) *Measured with an input voltage leading to same rectified output voltage at no-load operation (f_{SWITCH}=0kHz)*

The target applications of this gate driver are inverters in the medium power range (10... 100kW), in which each IGBT requires a gate drive power of typically around 1W.

Measurements have shown that under the same conditions the maximum power which could be transmitted by using the planar transformer was about 0.5W lower than with the toroidal core transformer. One reason for the lower power transmission is the lower magnetic coupling of the planar version, but because of the very high transmission frequency the AC winding resistance of the transformer becomes important too.

The reduction of the maximum power transmission can be explained by using the equivalent circuit diagram in Figure 9.

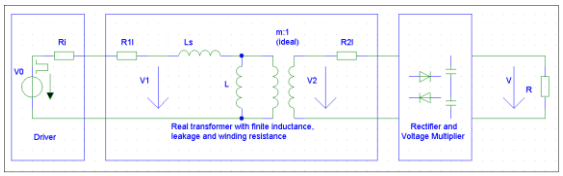

Figure 9: Equivalent circuit diagram

Core losses are neglected due to the applied low-loss ferrite material and the small magnetic flux swing. To make the influence of the leakage inductance and the winding resistance more transparent, the equivalent circuit is further simplified. The pulse voltage source in Figure 9 is substituted by a sinusoidal one, and the resistor R_d is introduced. This resistor represents the effective resistance of the voltage multiplying output rectifier. The resulting equivalent circuit is shown in Figure 10.

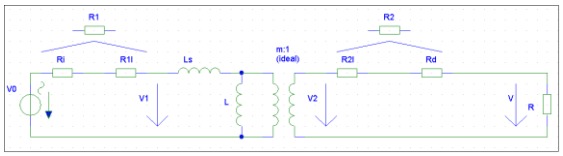

Figure 10: Simplified equivalent circuit diagram

Using this equivalent circuit, the possible power transmission can be calculated:

$$L_s = L_1\sigma \qquad L = L_1(1-\sigma) \qquad \text{(1a,b)}$$

$$m = \sqrt{\frac{L_1}{L_2}}\sqrt{1-\sigma} \qquad \text{(1c)}$$

The absolute values of the voltages are given by:

$$\frac{V}{V_2} = \frac{R}{R+R_2} \qquad \text{(1d)}$$

$$\frac{V_2}{V_1} = \sqrt{\frac{L_2}{L_1}(1-\sigma)}\,\frac{1}{\sqrt{1+\left(\frac{\omega L_2 \sigma}{R+R_2}\right)^2}} \qquad \text{(1e)}$$

$$\frac{V_1}{V_0} = \sqrt{\frac{\left(\omega^2 L_1 L_2 \sigma\right)^2 + \left(\omega L_1 (R+R_2)\right)^2}{\left((R+R_2)R_1 - \omega^2 L_1 L_2 \sigma\right)^2 + \left(\omega L_1 (R+R_2) + \omega L_2 R_1\right)^2}} \qquad \text{(1f)}$$

$$V = \frac{V}{V_2}\frac{V_2}{V_1}\frac{V_1}{V_0}V_0 \qquad \text{(1g)}$$

From Equation (1g) the dependency of the equivalent rectified output voltage *V* from the primary and secondary inductance, load, leakage inductance, the internal resistances and the transmission frequency can be derived. The power at the load *R* is given by:

$$P = \frac{V^2}{R} \qquad \text{(2)}$$

With Equation (2) the load resistor *R* in Equation (1g) can be substituted. However, an analytical solution for *P* is to complex and practically not usable. Since the output voltage *V* is only slightly affected by term (1f), this term is considered constant in a first step:

$$\frac{V_1}{V_0} = c = const. \qquad \text{(3)}$$

For a practical representation of the maximum possible output power depending on the leakage inductance, the no-load voltage must be kept constant:

$$V_{2l} = \sqrt{\frac{L_2}{L_1}(1-\sigma)} \cdot V_0 = const. \qquad \text{(4)}$$

Using Equations (2) to (4), Equation (1g) can be solved for *P*:

$$P = \frac{V\sqrt{R_2^2 V^2 + \left(c^2 V_{2l}^2 - V^2\right)\left(R_2^2 + \omega^2 L_2^2 \sigma^2\right)} - R_2 V^2}{R_2^2 + \omega^2 L_2^2 \sigma^2} \qquad \text{(5)}$$

By neglecting the influence of the leakage inductance the following approximation is valid for Equation (1f):

$$\frac{V_1}{V_0} = \frac{(R+R_2)}{(R+R_2) + \frac{L_2}{L_1}R_1} = c \qquad \text{(6)}$$

The maximum output power is determined by the undervoltage threshold of the secondary side ASIC:

$$V = V_{UV} \tag{7}$$

With an estimation of the maximum power at the undervoltage limit a corresponding load resistance can be calculated:

$$R = R_{UV} = \frac{V_{UV}^2}{P_{UV,estimate}} \tag{8}$$

Finally, referring to Equations (4) to (8) gives:

$$P_{UV} = \frac{V_{UV}\sqrt{R_2^2 V_{UV}^2 + \left(c_{UV}^2 V_{2l}^2 - V_{UV}^2\right)\left(R_2^2 + \omega^2 L_2^2 \sigma^2\right)} - R_2 V_{UV}^2}{R_2^2 + \omega^2 L_2^2 \sigma^2} \tag{9a}$$

$$c_{UV} = \frac{1}{1 + \frac{L_2}{L_1}\frac{R_1}{\frac{V_{UV}^2}{P_{UV,estimate}} + R_2}} \tag{9b}$$

$$R_1 = R_{1l} + R_i \qquad R_2 = R_{2l} + R_d \tag{9c,d}$$

Figure 11 shows the open winding series resistances of the primary and secondary side of the transformer for both the toroidal and the planar type. The measurements were done with an impedance analyzer.

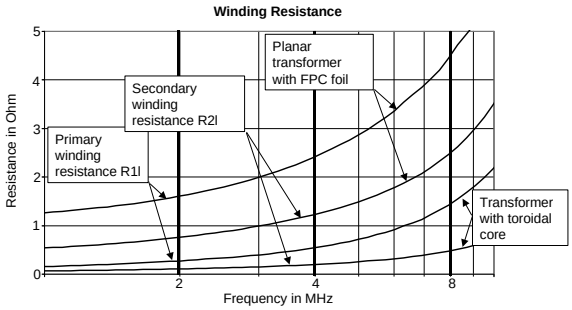

Figure 11: Measured winding resistances

Table 3 shows the corresponding winding resistance values for the transmission frequencies 2MHz, 4MHz and 8MHz.

Table 3: Measured winding resistance at 2, 4 and 8 MHz and calculated average values

f / MHz	*2*	4	8	avg(4,8)	avg(2,4)
$R_{1l,core}$ / Ω		0.5	1.4	1.0	
$R_{2l,core}$ / Ω		0.2	0.5	0.4	
$R_{1l,planar}$ / Ω	*1.6*	2.4	4.4	3.4	*2.1*
$R_{2l,planar}$ / Ω	*0.7*	1.2	2.5	1.9	*1.2*

Using the average values from Table 3 for the winding resistances and the measured values for R_i, R_d, L_1 and L_2, the maximum power transmission depending on the leakage inductance can be calculated with Equations (9a) to (9d).

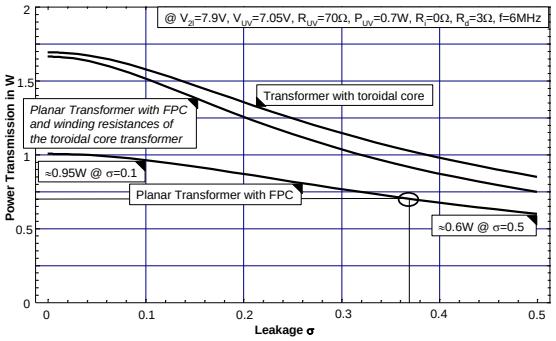

Figure 12: Power transmission in dependence of the leakage inductance (approximation)

Figure 12 shows the importance of a low AC winding resistance. The maximum power transmission is basically limited by the internal resistances when the transformer has a very low leakage inductance.

Although Equations (9a) and (9b) are only approximations the results match well the exact values as can be seen from the Figures 12 and 13.

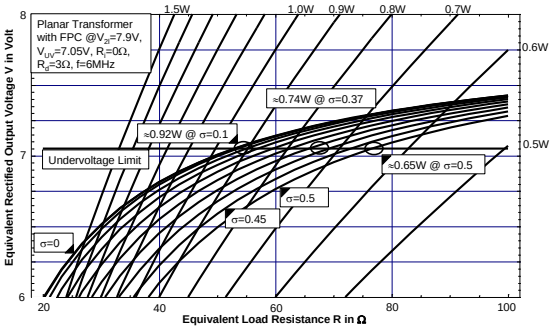

Figure 13: Power transmission in dependence of the leakage inductance and load

Figure 11 and Table 3 show a way towards an increase of the output power. Reducing the average transmission frequency from 6MHz to 3MHz results in an increase of the maximum output power by about 40% (see Figure 14). This is due to both the reduced winding resistances at 3MHz and the reduced influence of the leakage inductance (Equation 1e). In all cases the calculated and measured values agree very well.

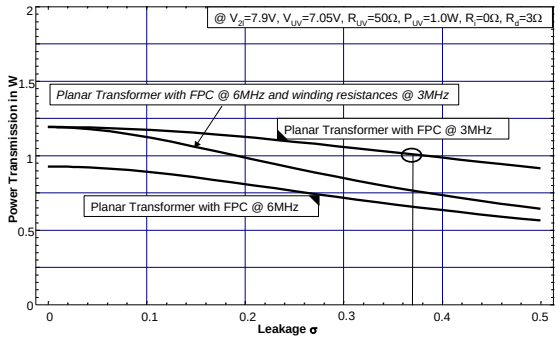

Figure 14: Power transmission in dependence of the leakage inductance (3MHz and 6MHz)

The reduction of the transmission frequency leads to an increase of the jitter and the time delays however [1]. Other optimizations are under investigations therefore. An considerable contribution to the internal losses results from R_D. Further improvements are possible by optimising the output rectifier and the voltage multiplier. Also the winding geometry has a great influence on the winding resistance [5].

Without using expensive RF litz wire the toroidal core can not benefit from the larger copper cross section because of the skin effect. The dept of penetration in the case of copper is given by:

$$\delta \approx \frac{2.2mm}{\sqrt{f\,/\,kHz}} \qquad (10)$$

With an average transmission frequency of about 6MHz the depth of penetration is about 30µm. This fits well to the 35µm thickness of the copper traces on standard PCBs.

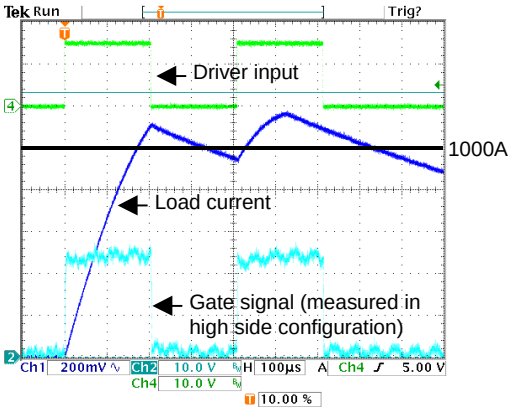

Figure 15: Double pulse measurement in high side configuration at 800V DC link voltage and 1000A collector current

A disadvantage of planar transformer is their higher coupling capacitance C_{12} between the primary and secondary side. Table 2 shows that in our case C_{12} of the planar transformer was about five times higher compared to the toroidal version. Nevertheless, no perturbation of the switching behaviour could be observed. Figure 15 shows a double-pulse measurement using the driver for controlling the high-side switch in an IGBT halfbridge at a DC link voltage of 800V and 1000A commutation current.

Summary

For an isolated halfbridge gate driver based on embedded magnetics the maximum power transmission is derived. Although being a low cost design the new gate driver provides all protection and monitoring functions of a modern high-end gate driver (e.g. desaturation monitoring, undervoltage shut-down, negative turn-off voltage, etc.). The consistent renunciation of temperature sensitive components like opto-devices and electrolytic capacitors makes the new driver especially suitable for high temperature applications. In conjunction with a very high EMI ruggedness, the driver is well suited for intelligent power modules.

Acknowlegment

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