9th SiNANO Modelling and Simulation Summer School
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Process Simulation for Advanced CMOS Devices

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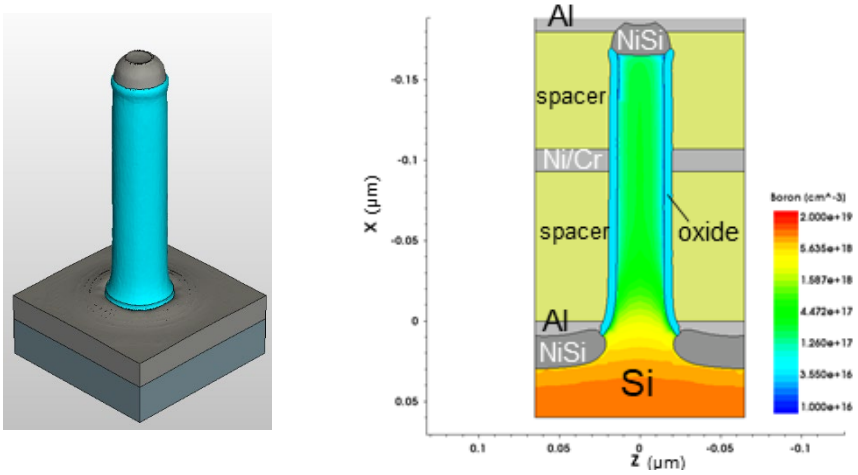
Abstract

In the presentation, an outline of the application of process simulation to the manufacturing of advanced CMOS devices will be given. This includes the process steps ion implantation, thermal annealing, lithography, deposition, etching, and oxidation. For these steps, the underlying physical models will be discussed. Aspects of the numerical implementation will be covered as well. Examples for simulation sequences will be shown, with particular emphasis on several types of advanced nano-electronic devices such as FinFETs or GAA (gate-all-around) transistors. In addition, it will be demonstrated how simulation can be used to study the impact of process variations.



3D simulation of a vertical gate-all-around nanotransistor (from the EU project MUNDFAB)