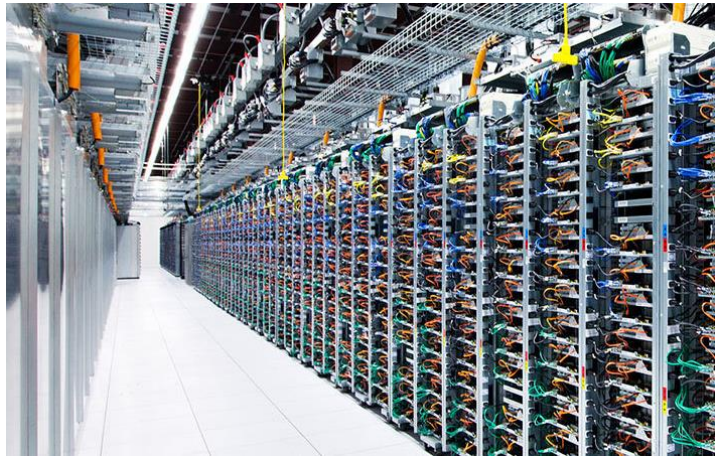
Holographic Lithography Simulations drive the ASML EUV roadmap

Timon Fliervoet & Gerardo Bottiglieri

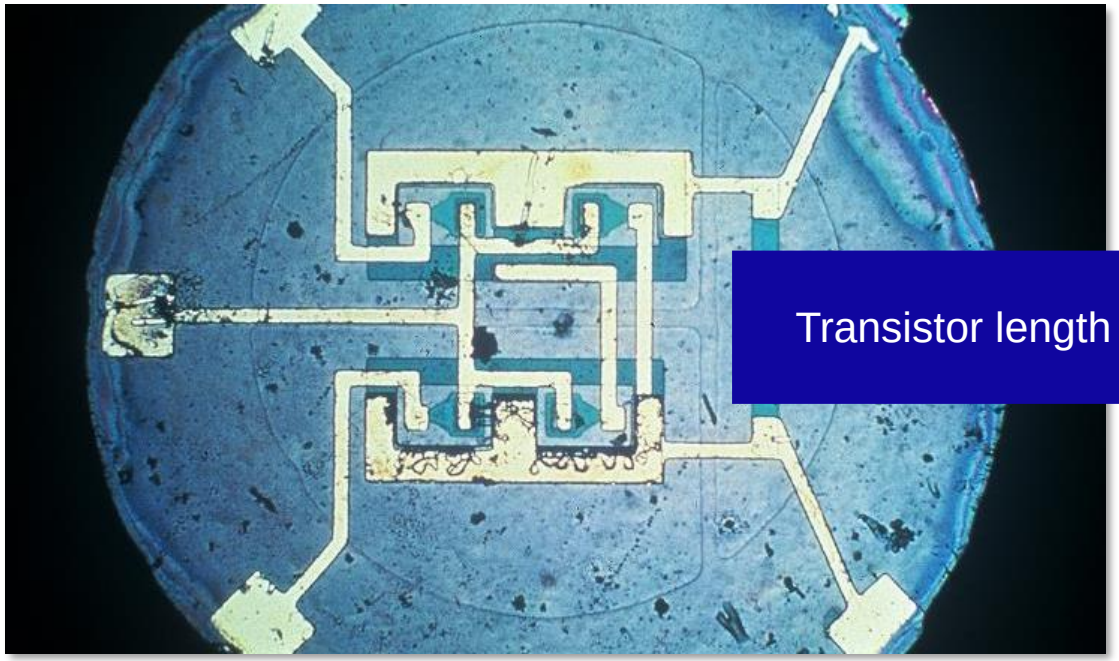
Erlangen

In our world today, chips are everywhere

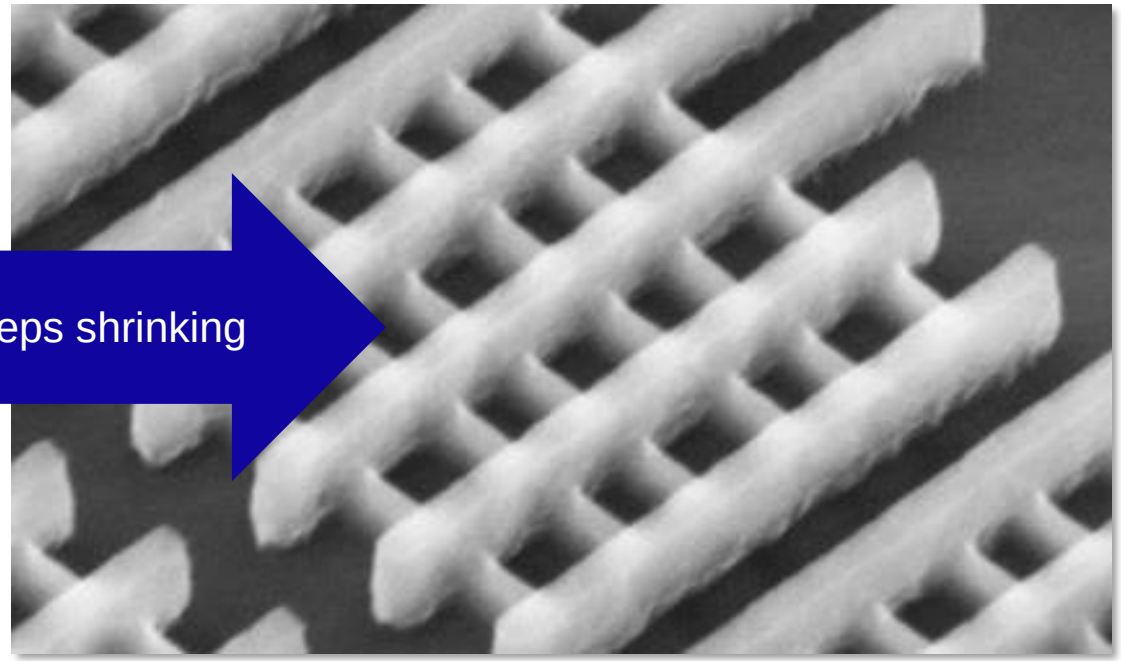


Economics dictate to make smaller transistors

Moore’s Law: number of transistors double every two years



Transistor length keeps shrinking

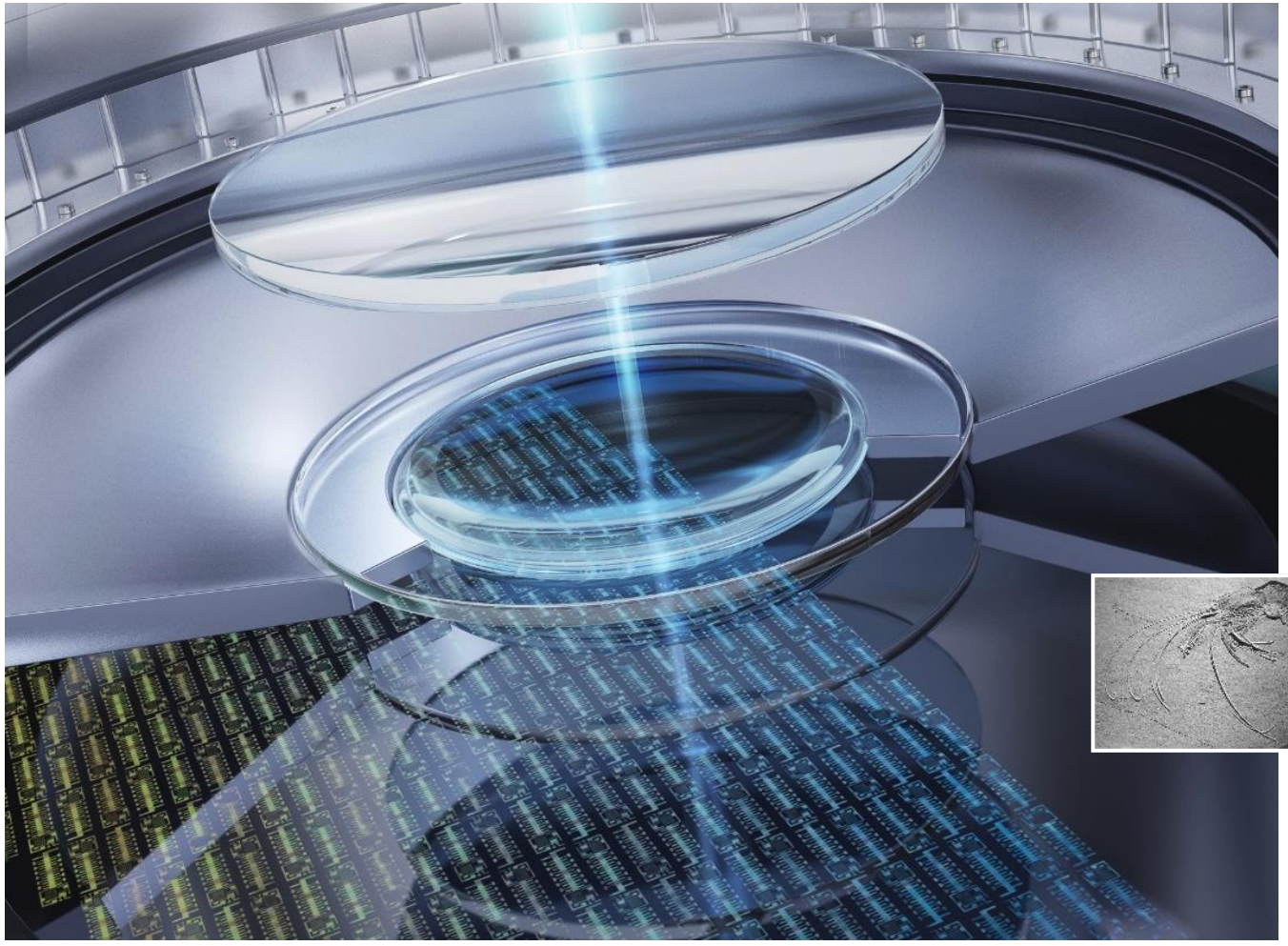


The first integrated circuit on silicon, on a wafer the size of a fingernail

(Fairchild Semiconductor, 1959)

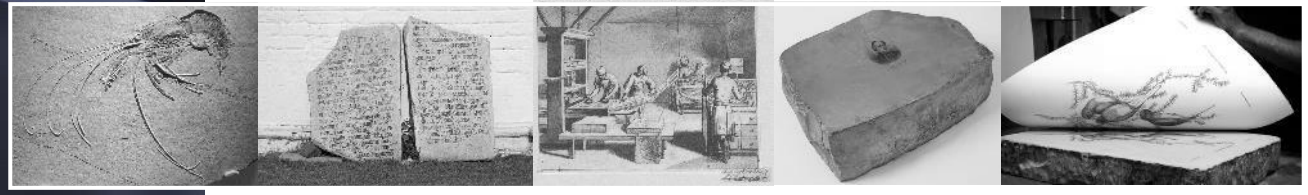
Today: Billions of transistors on the same area

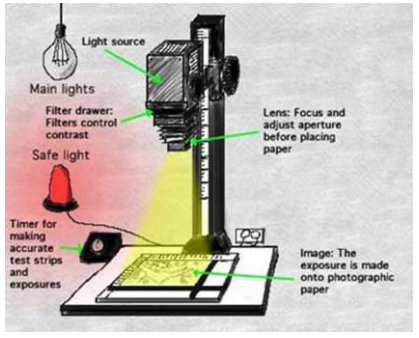
Lithography is critical for shrinking transistors



Lithography is the only semiconductor production step to process the wafer die per die, in contrast with all other production steps. This makes ASML's technology so pivotal in getting the highest yield and best performance in chip manufacturing

Lithography: Ancient Greek λίθος, lithos, meaning 'stone', and γράφειν, graphein, meaning 'to write')



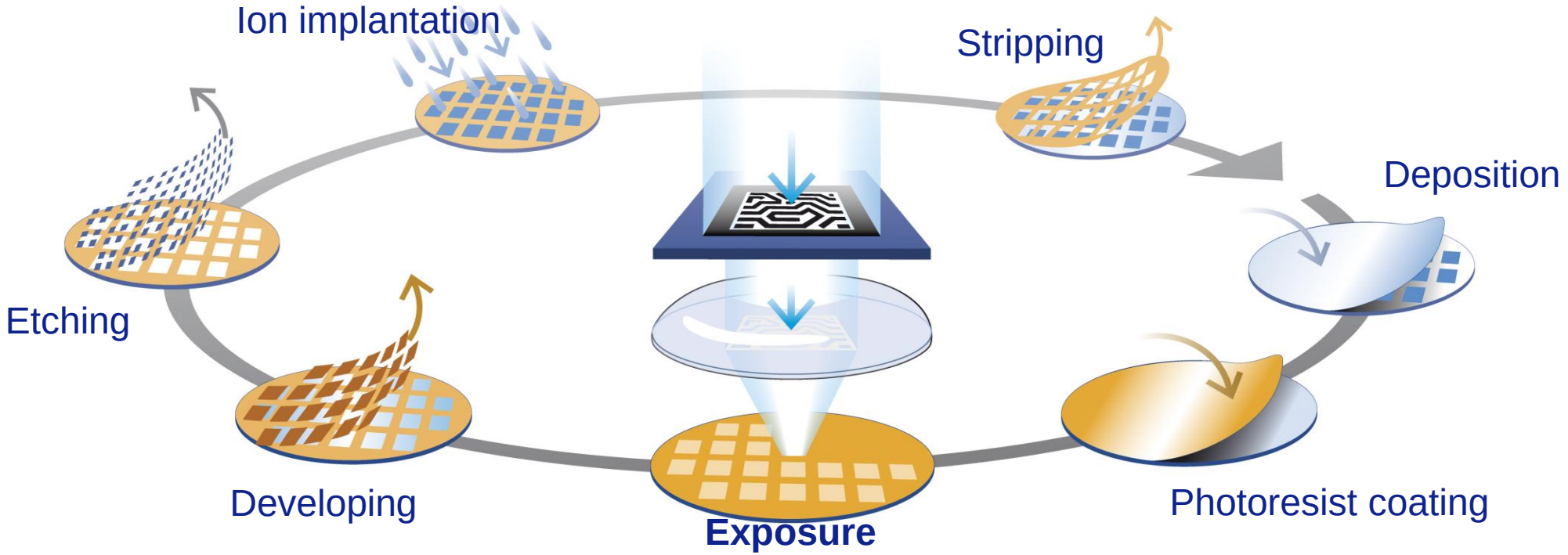


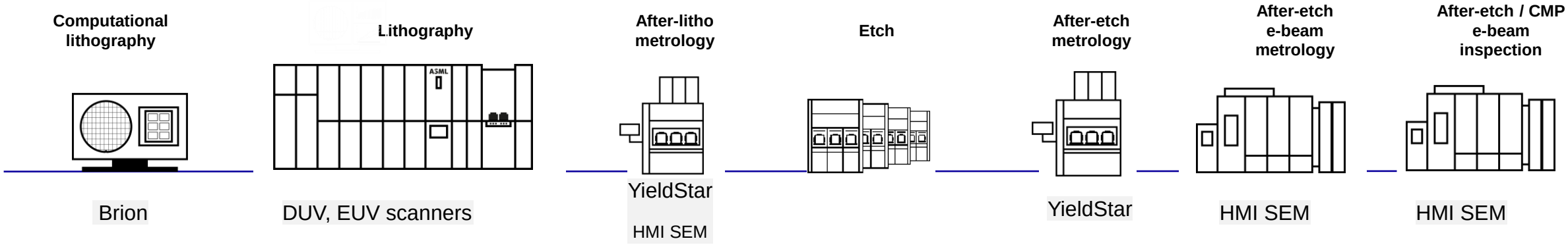
How a lithography system works

A short video

The semiconductor manufacturing loop

100’s of processing steps per wafer





A tightly integrated set of solutions for scaling and yield

Lithography scanner with advanced control capability

EUV: NXE platform

DUV: XT and NXT platform

Etch and deposition tools

Image

Make the image printable and optimize for yield

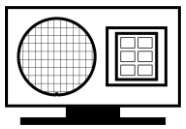
Keep production stable

Holistic lithography keeps scaling affordable

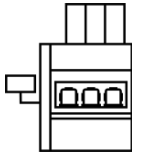
Model

Measure

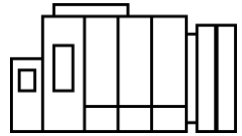
Ensure measurement captures a maximum of relevant information



Optical proximity correction



YieldStar



E-beam

Computational lithography and computational metrology

Optical metrology
E-beam metrology
E-beam inspection

Technology-wise, we had to move mountains

Sometimes it seemed impossible– until we did it

$$CD = k_1 \frac{\lambda}{NA}$$

80s

436 nm → 365 nm light
100 mm → 150 mm wafers

90s

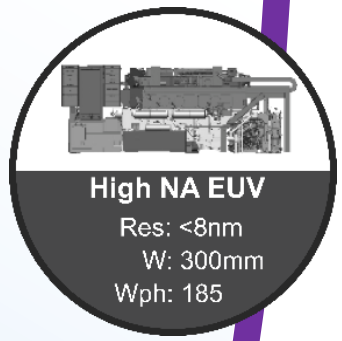
248 nm → 193 nm light
150 mm → 200 mm wafers
'step & repeat' → 'step & scan'

00s

200 mm → 300 mm wafers
Dry → immersion lithography
Single stage → dual stage

10s

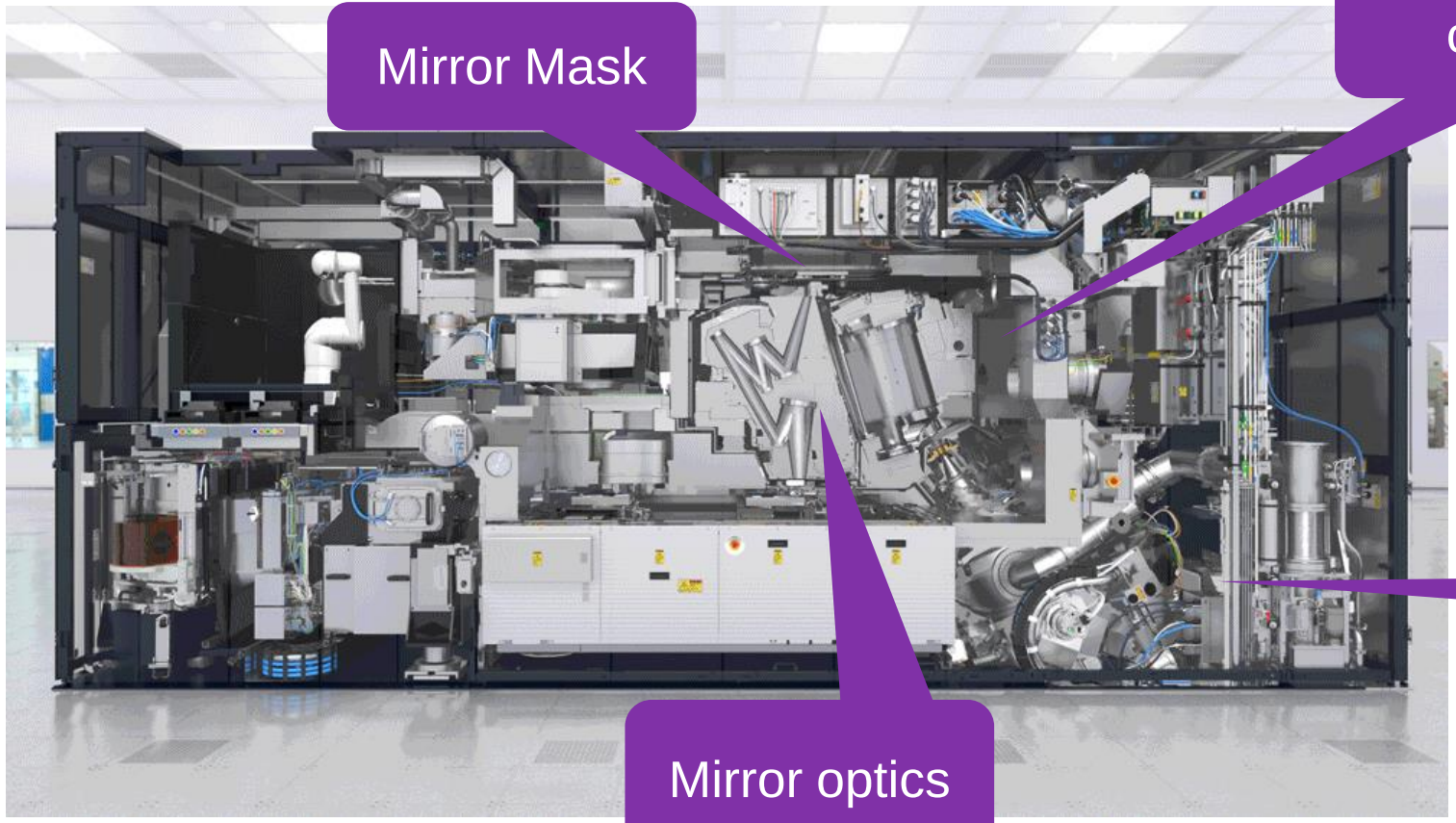
Litho → Holistic litho
Immersion → EUV
Letho 0.33 → EUV 0.55



System complexity

Key changes from DUV to EUV lithography

From transmission to reflective optics



Lithography Imaging Simulations play a Key Role in ‘Life of ASML tool’

Imaging feasibility for new tool types

No machine to experiment on

Performance verification

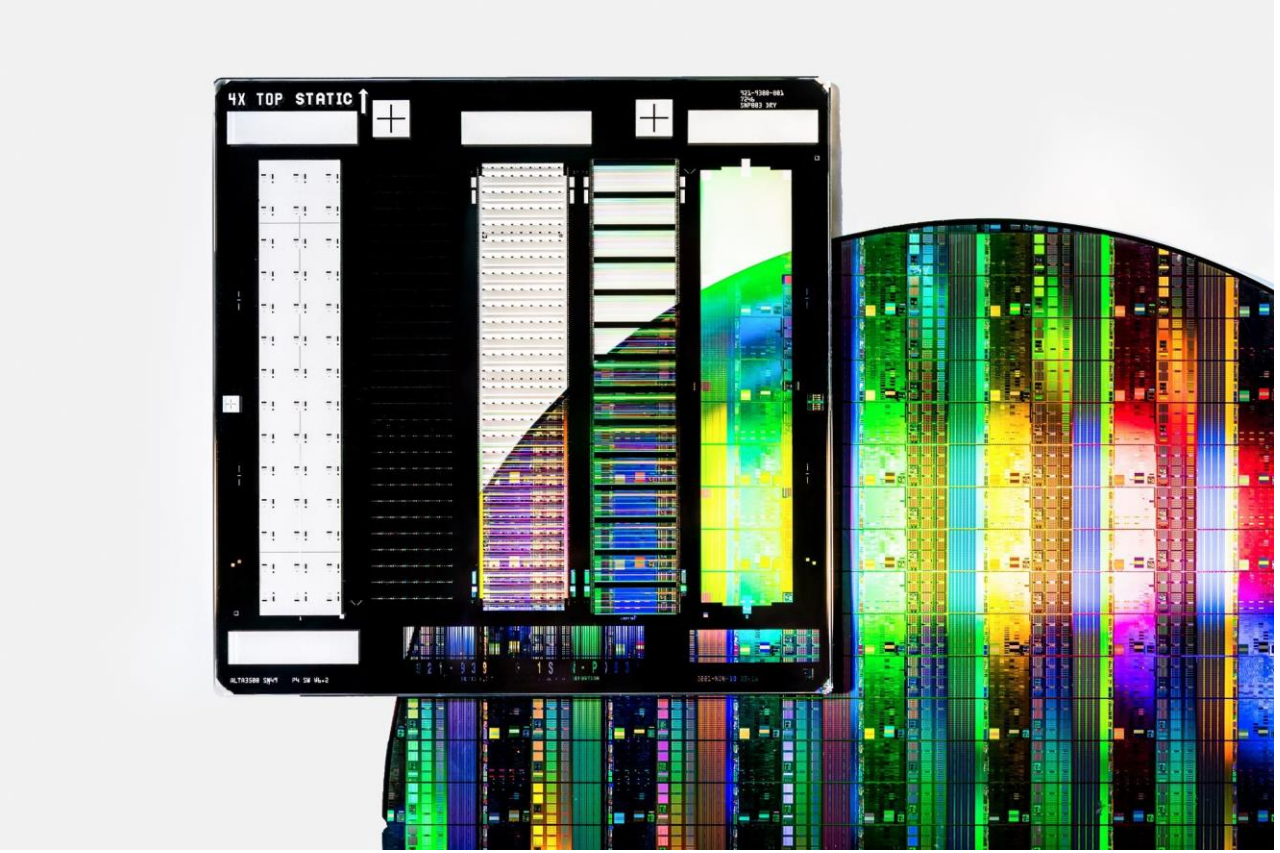
Did we build what we specified?

Root-cause finding on performance issues

Investigate sensitive parameters first

Replace experiments

Reduce number of test wafers and tool time



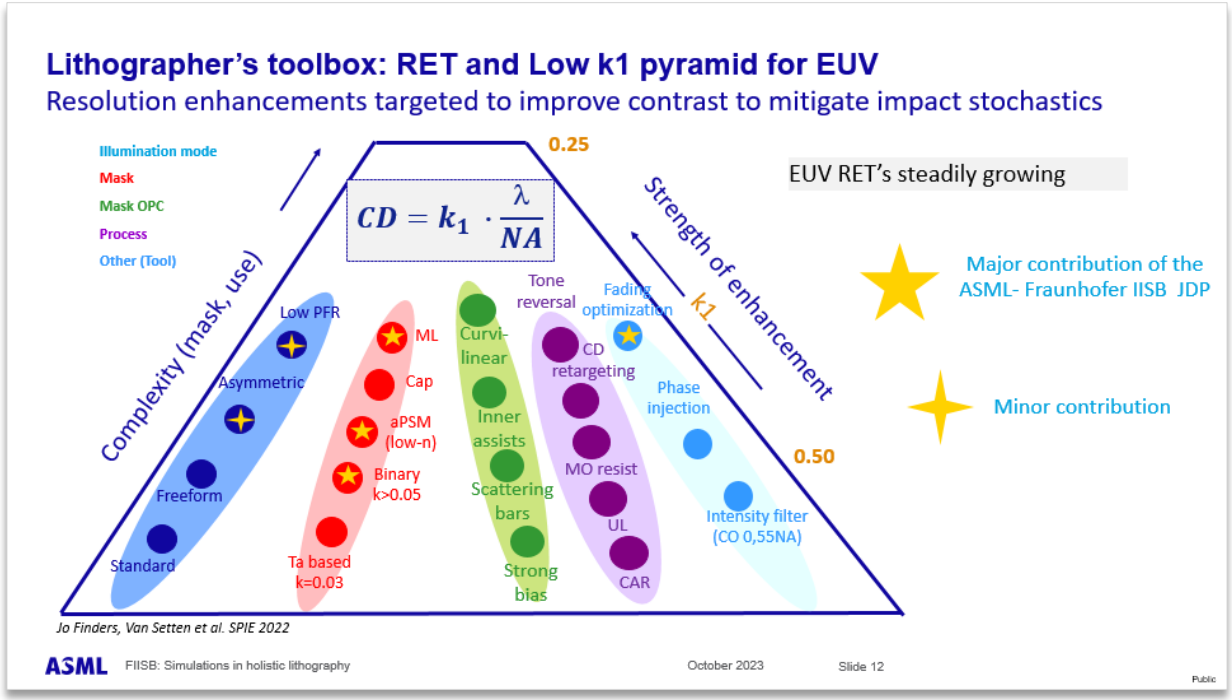
Customer support:

Accelerate process development determining litho strategy

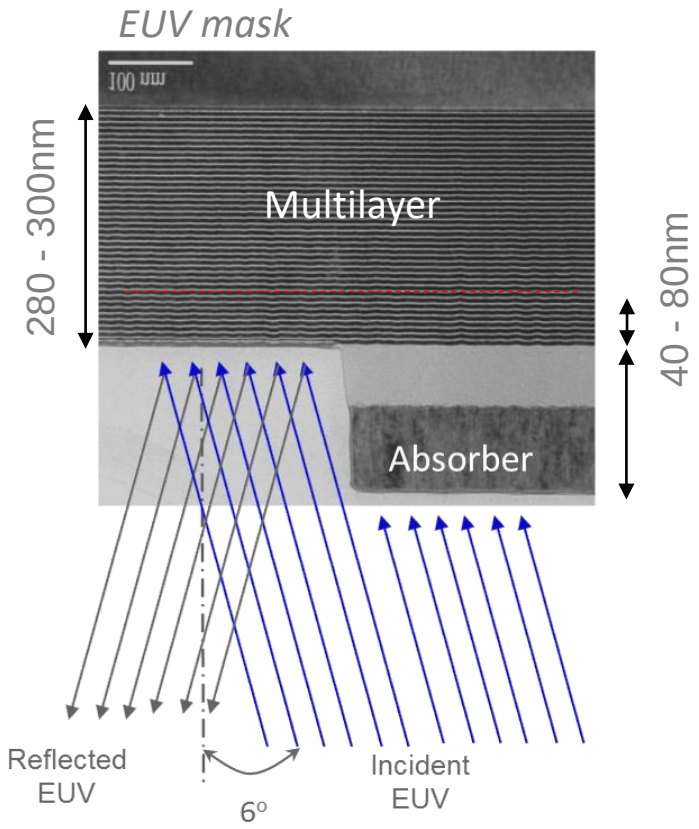
Improve yield: optimize exposure conditions to maximize process robustness

Simulations: The Quest for the Best Compromise

A machine can never be perfect in performance, cost and time



Adoption of EUV Lithography has Increased the Need for Simulations



EUV masks are complex:

a. **Multiple physical phenomena** take place at mask

b. **Multiple mask factors/components** greatly affect the final scanner lithographic performance

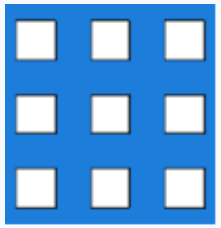
Simulations:

- Understand physical mask factors in lithography
- Recommendations for mask absorber
  - (geometry, n, k), multilayer, illumination direction, Assist Features.
- Assess mitigation strategies

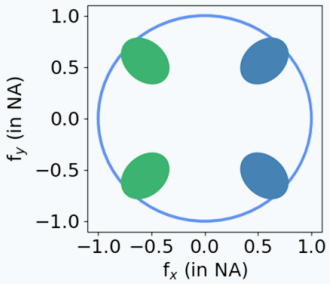
Novel exposure techniques provide improved contrast

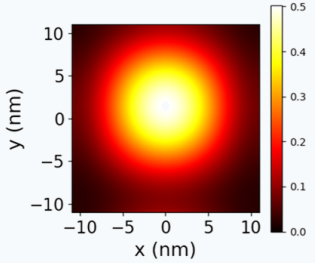
Complex simulations require fundamental understanding

Split pupil exposure



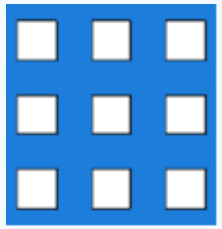
TaBN-absorber
target: 11 nm



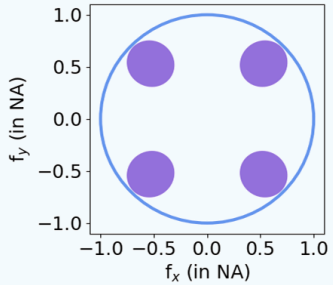


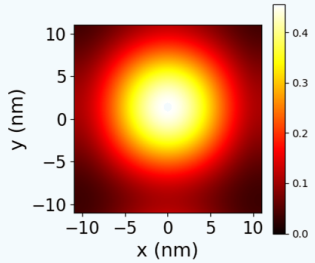
thrSize = 0.289
NILS = 2.19
nilsE = 1.18
DoF = 78 nm

Quadrupole exposure

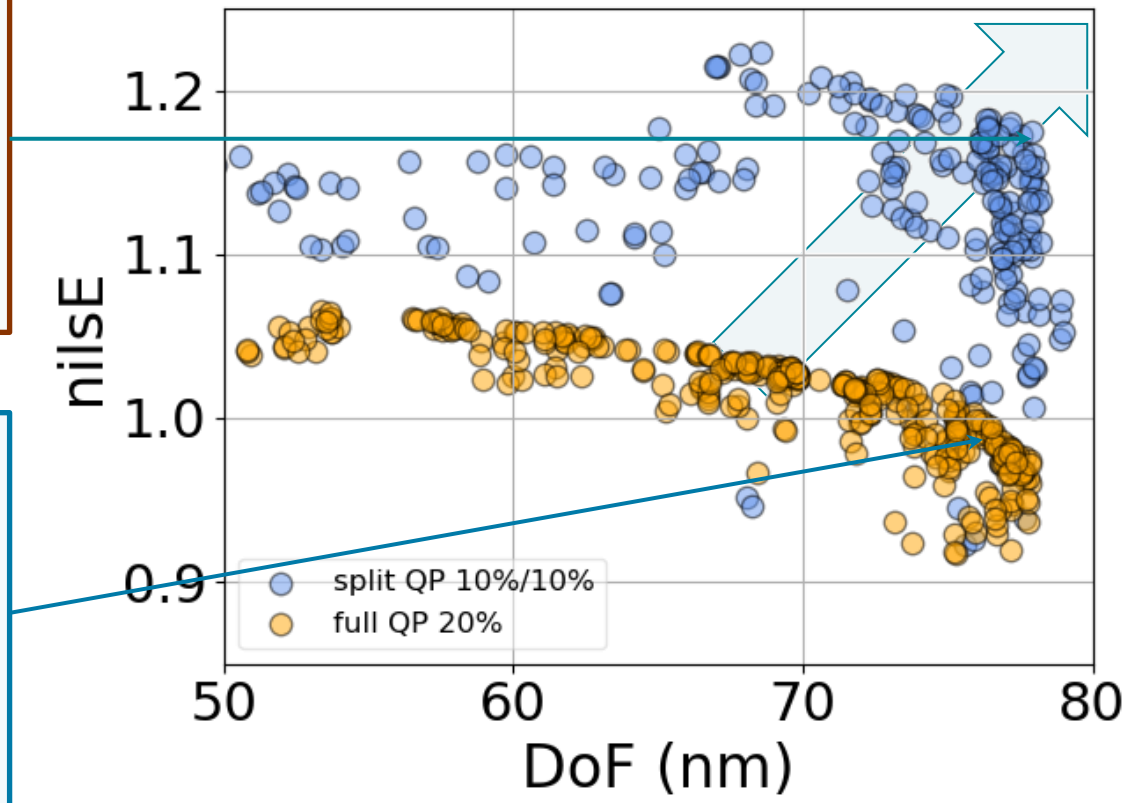


TaBN-absorber
target: 11 nm





thrSize = 0.282
NILS = 1.91
nilsE = 1.02
DoF = 75 nm



A. Erdmann et al, Exploration of imaging solutions for high NA EUV lithography by combination of dual monopole exposure strategies with low-n absorbers, EMLC 2023, Dresden

ASML-Fraunhofer IISB collaboration dates back to 2018

I. The beginning

***2018**:* Fundamentals of high-NA EUV imaging
→ Development of the Hybrid Mask Model
A. Erdmann, et al., https://doi.org/10.1117/12.2515678

II. What is the optimum mask for high NA EUV?
… or "Pathfinding the perfect EUV mask"

2019: Role of the mask multilayer (ML)
→ idealized ML model, ML properties and imaging:
H. Mesilhy, et al., https://doi.org/10.1117/12.2551870

2020: Role of the mask absorber
→ physics of low-n materials: waveguide effects, "double diffraction"
H. Mesilhy, et al., https://doi.org/10.1117/12.2587948
H. Mesilhy, et al., https://doi.org/10.1117/1.JMM.20.2.021004

2021: Imaging characteristics of low-n absorbers
→ impact of focus, illumination, biasing & tonality for single pitch Line/Spaces and Contact Holes
H. Mesilhy, et al., https://doi.org/10.1117/12.2601243

III. Multi-feature imaging, imaging improvements techniques

2022: Imaging solutions for multi-pitch L/S imaging scenarios
→ imaging tradeoffs between Contrast, Throughput Depth of Focus
H. Mesilhy, et al., https://doi.org/10.1117/12.2614174
→ demonstrate the potential of split pupil exposures on Line/Spaces

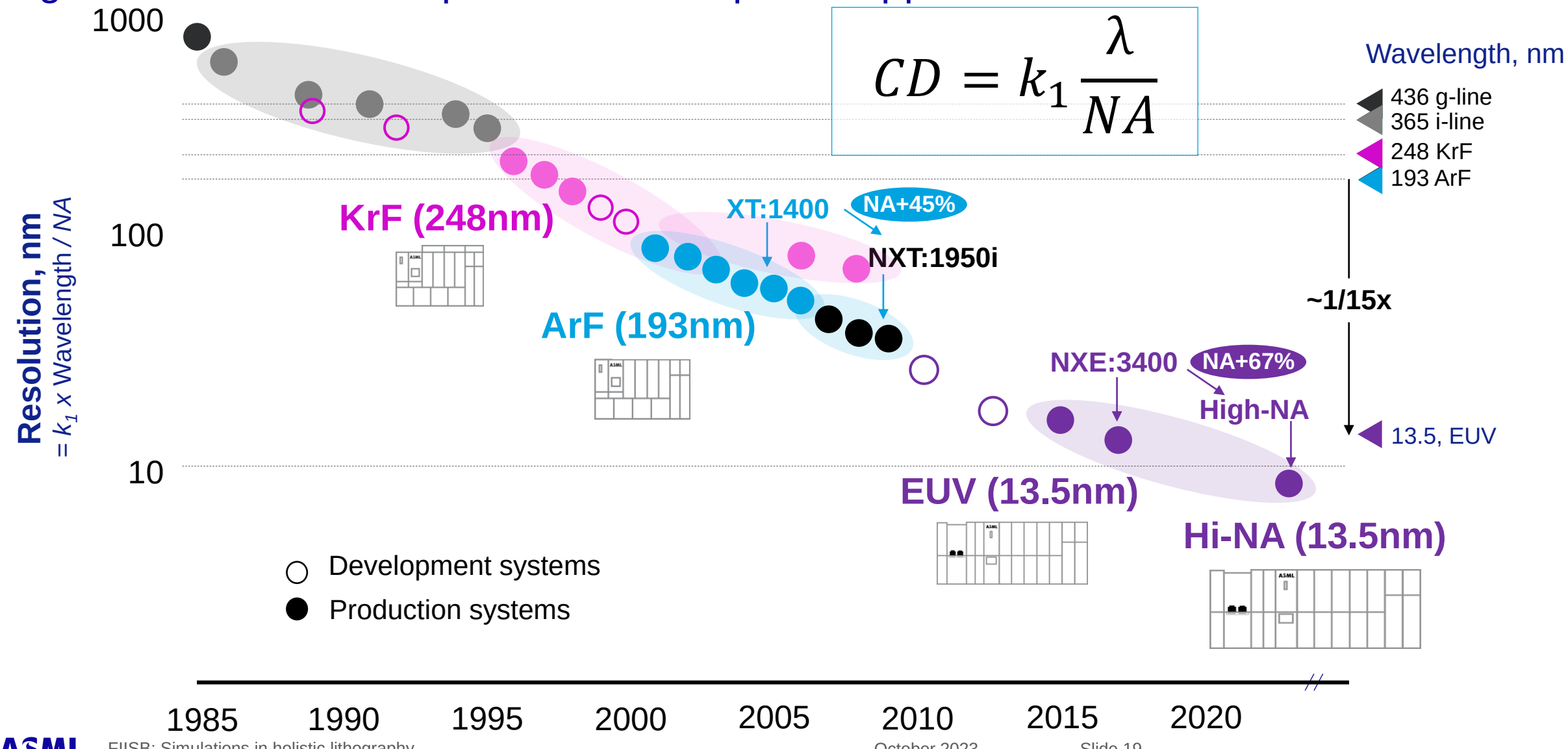
2023: Split Exposure imaging method on 2D patterns Intrinsic roughness for Metal Oxide photoresists


ASML

Making a transistor

ASML tool Roadmap

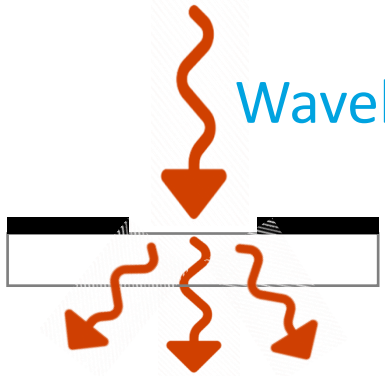
High-NA EUV on ASML product roadmap will support continuous shrink



Adoption of EUV Lithography has Increased the Need for Simulations

EUV masks are 3D

DUV



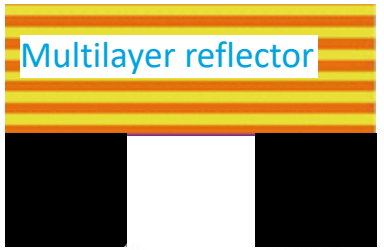
Wavelength: 193 nm

Mask absorber: 68 nm

human

German shepherd

EUV



Mask absorber: 50-70 nm

Wavelength: 13.5 nm

human

Statue of Wilhelm I in Koblenz