Friedrich-Alexander-Universität
Lehrstuhl für Elektronische Bauelemente | LEB

Process-dependent photoluminescence behavior evolution of stacking faults in 4H-SiC

N. Kölbel[1,a], B. Kallinger[2], C. Kranert[2], St. G. Müller[2], A. Fuchs[2], T. Erlbacher[3], F. Faisal[3], J. Schulze[1,2]

Motivation

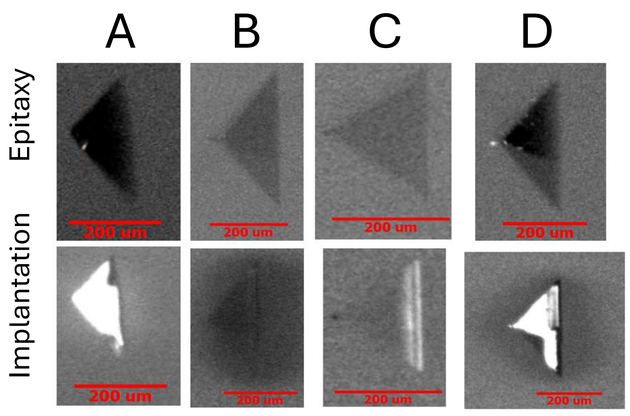
- Stacking faults (SF) are a limiting factor for device yield [1,2]
- Only 66% of PL SF cause MOSFET failure [3]
- Can the inconclusive failure rate for devices containing SFs be correlated to their properties?
- Can a subclassification based on optical measurements be established?

Experiments

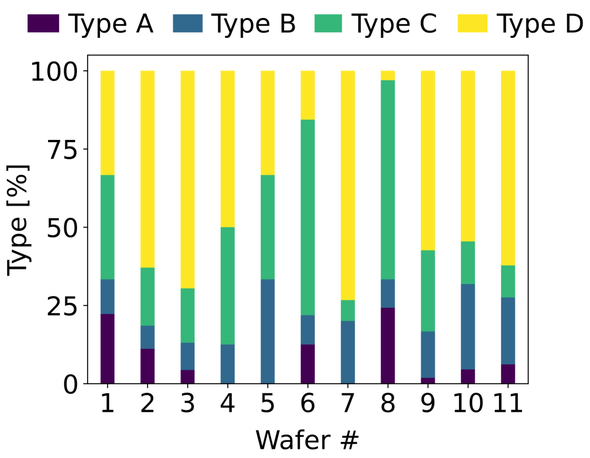
- 11 wafers (150 mm) with n-type epitaxy and patterned n+,p+,n+ implantation sequence and contacts
- Photoluminescence (PL) scans using the Lasertec SICA 88 after epitaxy and after implant and anneal
- IV-mapping for electrical assessment

Optical Mapping

- Before implantation: SFs appear qualitatively similar
- After implant and anneal: clear qualitative differences in PL signal brightness of SFs
- SFs can be categorized into four PL subtypes



A: bright triangle
B: dark triangle with dark surrounding area
C: dark triangle, partially luminescent
D: combination of A and B

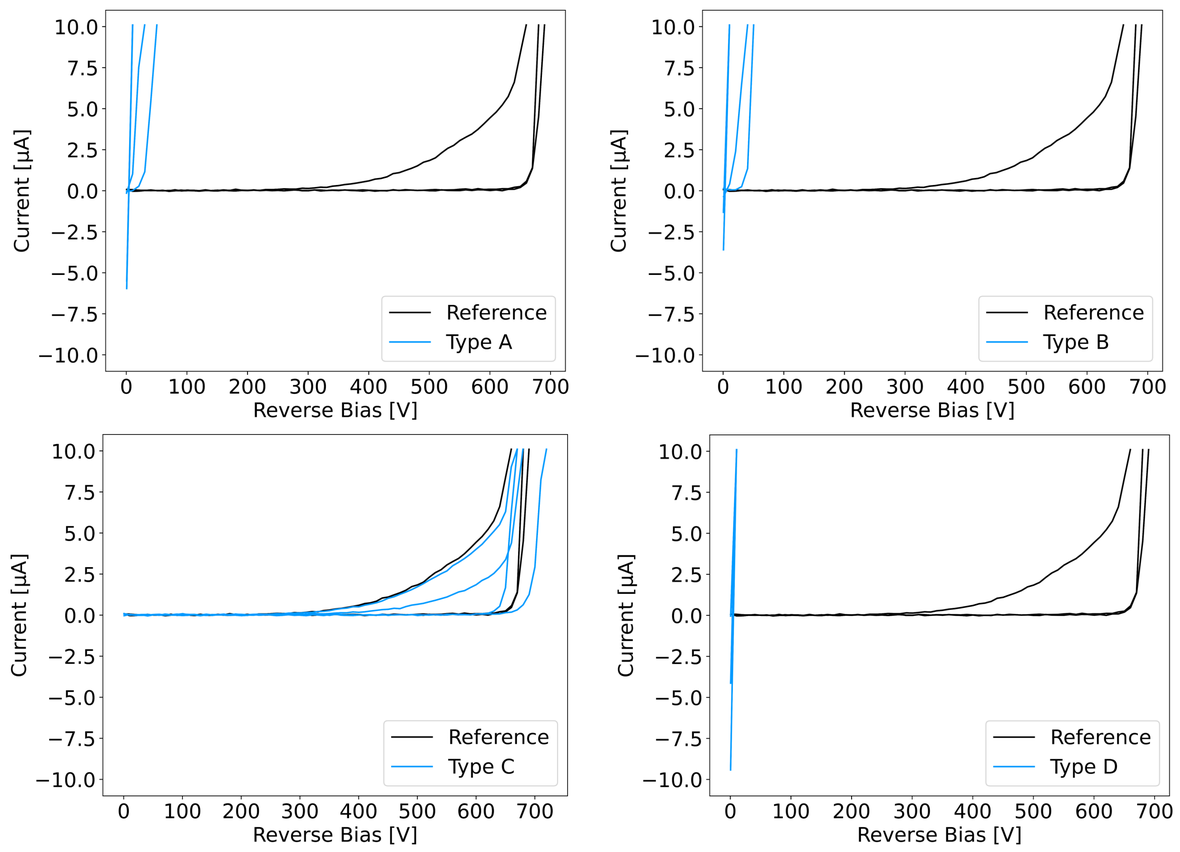


- Left plot shows relative occurrence of the different subtypes for the investigated wafers
- Type D is the most common type for most wafers
- **Exception**: wafers 6 and 8 with dominating Type C
- These two wafers got the p+ implantation at a different angle of 17°

→ **Implantation angle may have an impact on the formation of different SF subtypes!**

Electrical Mapping

- Forward and reverse bias I-V mappings of devices are correlated with the PL mappings
- 4 example devices per defect type are compared to reference devices without defect
- Each defect type has different effect on I-V characteristic under reverse bias:
  → **Type A, B, D**: strongly reduced breakdown voltage
  → **Type C**: no visible impact on breakdown voltage
  → **All types**: no visible impact in forward biasing



Conclusion

- SF that show a similar PL signature after epitaxy can be subdivided into categories using PL imaging after implant and anneal
- Indications for a correlation between different SF types and electrical failure found
- Results show the potential for further evaluation of SF during processing and subtypes to investigate impact of SF on electrical device failure

[1] Schoeck J, Schlichting H, Kallinger B, et al. (2018) Influence of Triangular Defects on the Electrical Characteristics of 4H-SiC Devices. MSF 924:164–167. https://doi.org/10.4028/www.scientific.net/MSF.924.164
[2] Das H, Justice J, Sunkari S, et al. (2024) The Role of Defects on SiC Device Performance and Ways to Mitigate them. DDF 434:51–59.
[3] Baierhofer D, Thomas B, Staiger F, et al. (2023) Correlation of Extended Defects with Electrical Yield of SiC MOSFET Devices. DDF 426:11–16.

[a]nadja.koelbel@fau.de
[1]Friedrich-Alexander-Universität, Lehrstuhl für elektronische Bauelemente, Cauerstraße 6, 91058 Erlangen Germany,
[2]Fraunhofer IISB, Schottkystrasse 10, 91058 Erlangen, Germany
[3]Nexperia Germany GmbH, Stresemannallee 101, 22529 Hamburg, Germany

ICSCRM 2025
14-19 September 2025
BEXCO, Busan, Korea