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# Towards a Fully Integrated 4H-SiC a-Plane Quantum-Chip – Transistors and Light Emitters

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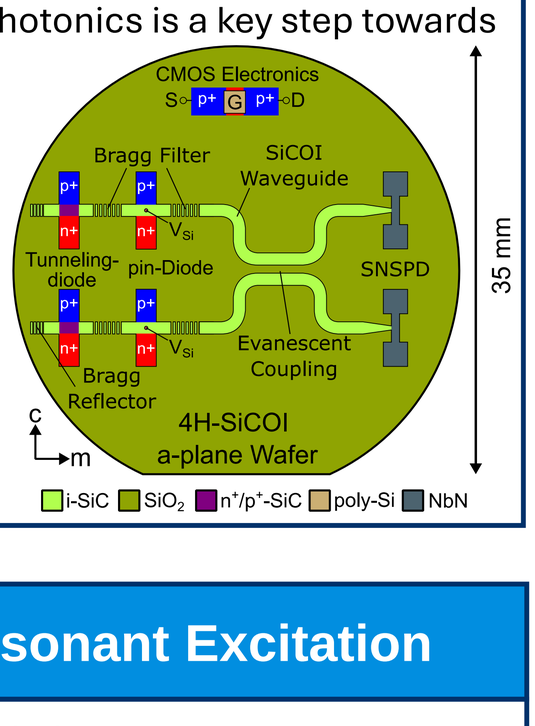
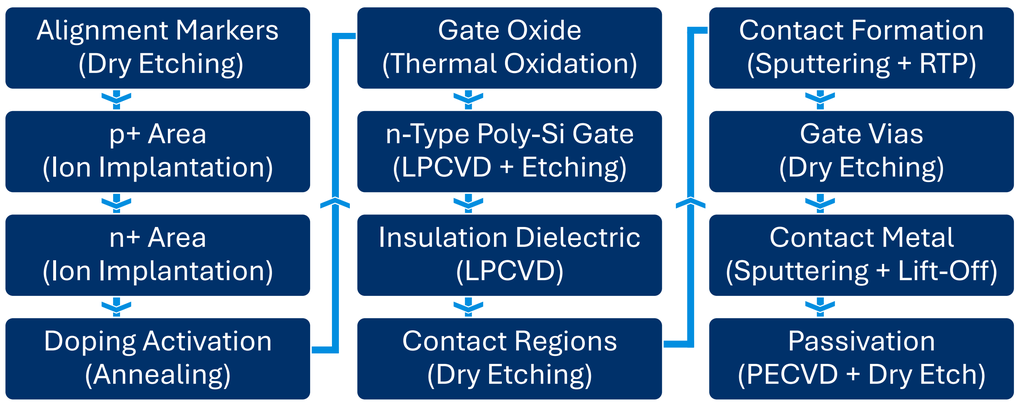
## Quantum Photonics Integrated Circuit (QPIC)

- On chip integration of electronics & photonics is a key step towards affordable integrated QPICs [1,2]
- 4H-SiC a-plane wafers allow wafer-scale resonant excitation of $V_{Si}$
- Challenges & goal:
  - CMOS process on a-plane
  - Demonstrate basic electronics
  - Integrate off-resonant light source
- Vision: Fully integrated photonics and electronics on a 4H-SiCOI a-plane wafer (see figure)

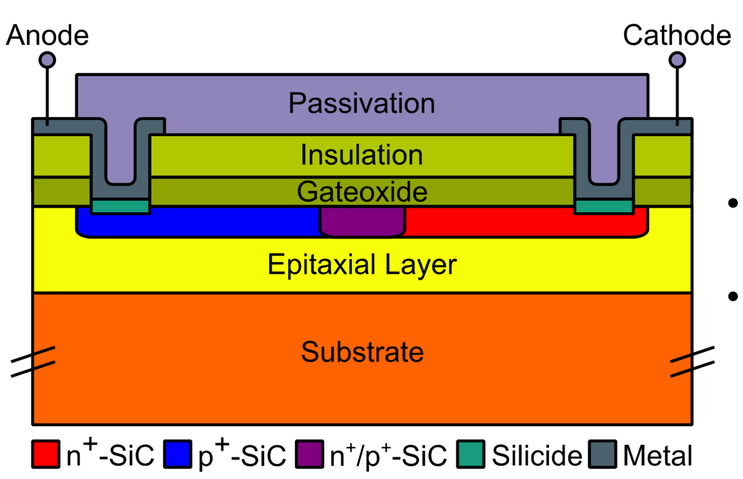



## CMOS Compatible Manufacturing of Devices

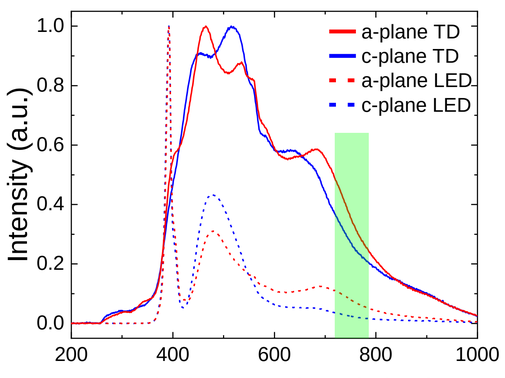
- CMOS process [3] on a-plane (35 mm) & c-plane (150 mm) 4H-SiC
- Low doped quantum ready epitaxial layer with 10 µm thickness [4]

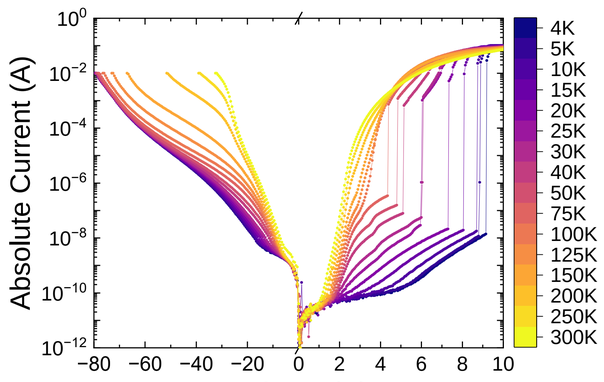



## Light Emitter for Off-Resonant Excitation



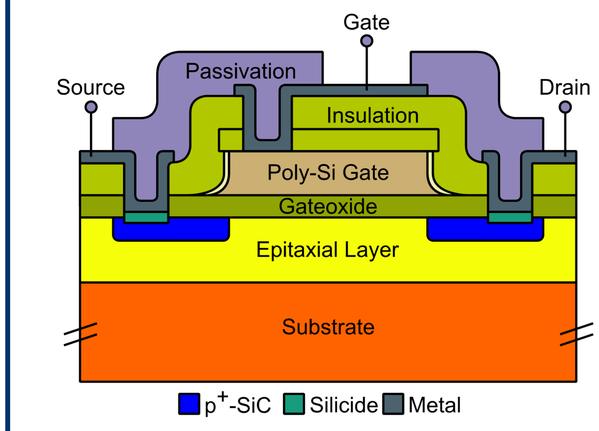

- Integration in 4H-SiCOI waveguides possible
- Overlapping $n^+/p^+$ doped emission region
- I-V forward bias: diode-like behavior
- I-V reverse bias: Zener breakdown at low bias due to $n^+/p^+$ co-doping
- Light emission in forward (LED) and reverse bias (Tunneling Diode)

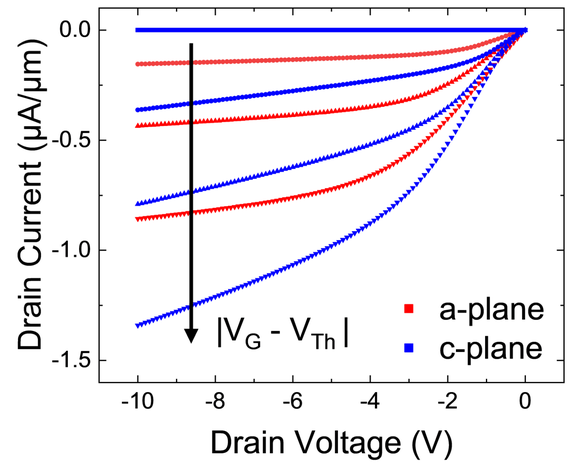



- Light emitting diode (LED):
  - Radiant recombination across bandgap or defect states [5]
- Tunneling diode (TD):
  - Tunneling-assisted optical recombination between donor and acceptor states
  - Broad spectrum, since emission energy is dependent on spatial distribution of dopants (band bending influences ΔE) [6]
  - Significant emission at 730 - 785 nm for off-resonant $V_{Si}$ excitation
- Functionality down to 4 K possible for increased voltages
- Jump in forward direction at low temperature due to freeze-out of charge carriers and re-ionization due to electric field [7]

## CMOS-Compatible Electronics



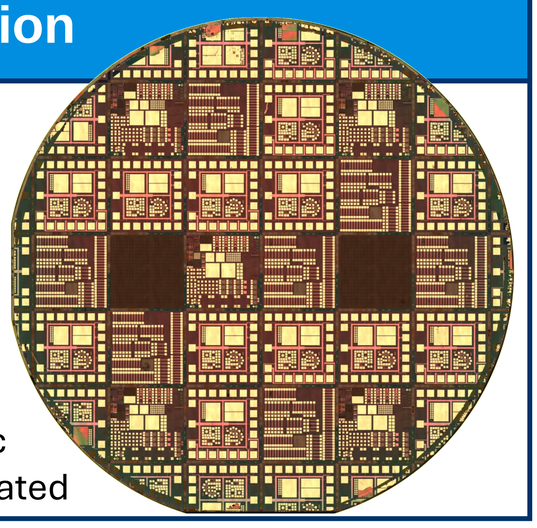




- Typical pMOS transistor shows CMOS capabilities of a-plane wafers
- Addition of mask layers for integration of nMOS and ICs possible
- Comparable electronic behavior between c-plane and a-plane
- Transistors are shown to remain functional at cryogenic Temp. [7, 8]

| Parameter | a-Plane | c-Plane |
|---|---|---|
| $I_{On} / I_{Off}$ ($10^6$) | 2.42 ± 0.04 | 2.48 ± 0.69 |
| Threshold Voltage (V) | -11.5 ± 0.05 | -6.60 ± 0.60 |
| Max. Mobility ($cm^2/Vs$) | 2.32 ± 0.14 | 2.84 ± 0.43 |
| $R_{On}$ @ $\lvert V_G - V_{Th}\rvert$ = 3.5V (kΩ) | 388 ± 7 | 321 ± 68 |

## Conclusion

- Wafer scale processing on quantum ready 4H-SiC a-plane wafers
- On-chip light source for off-resonant excitation of $V_{Si}$ demonstrated
- Light emission down to 4 K possible
- pMOS devices show comparable behavior for c- and a-plane wafers
- Key steps towards quantum photonic integrated circuits (QPICs) demonstrated



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