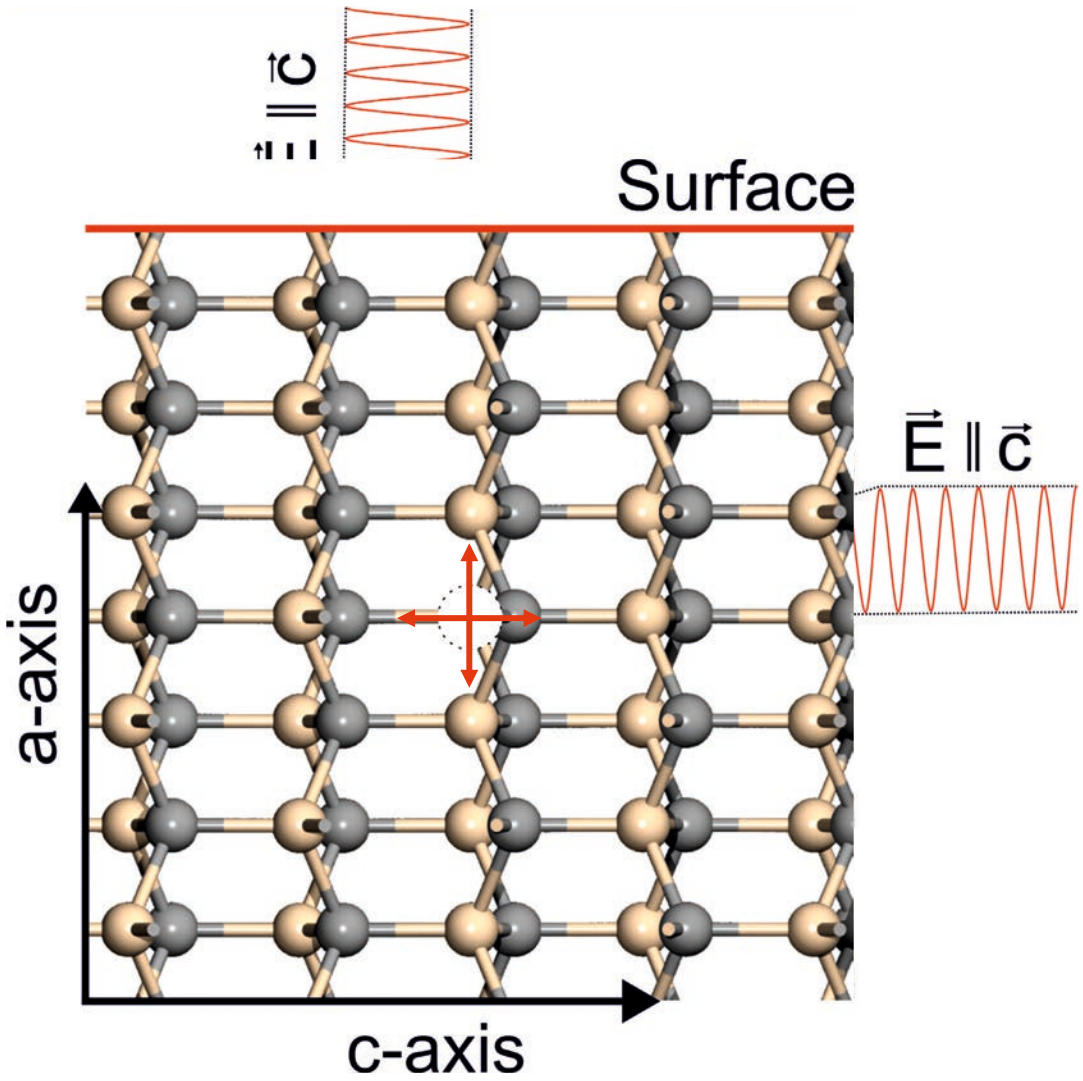
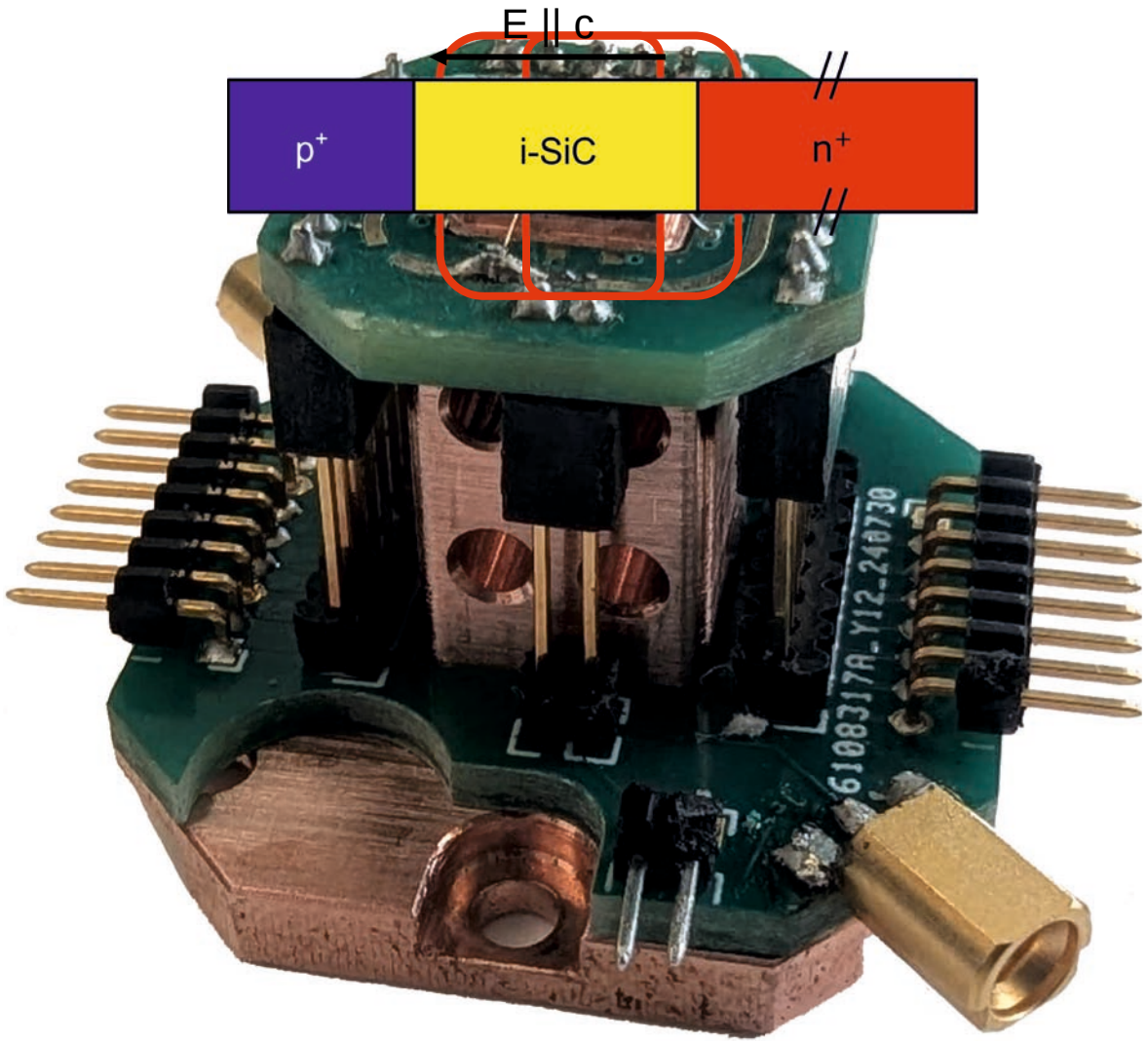
Friedrich-Alexander-Universität
Lehrstuhl für Elektronische Bauelemente

Jannik Schwarberg

Lateral pin-Diodes on 4H-SiC a-Plane Wafers

Motivation for lateral pin-diodes on 4H-SiC a-plane wafers



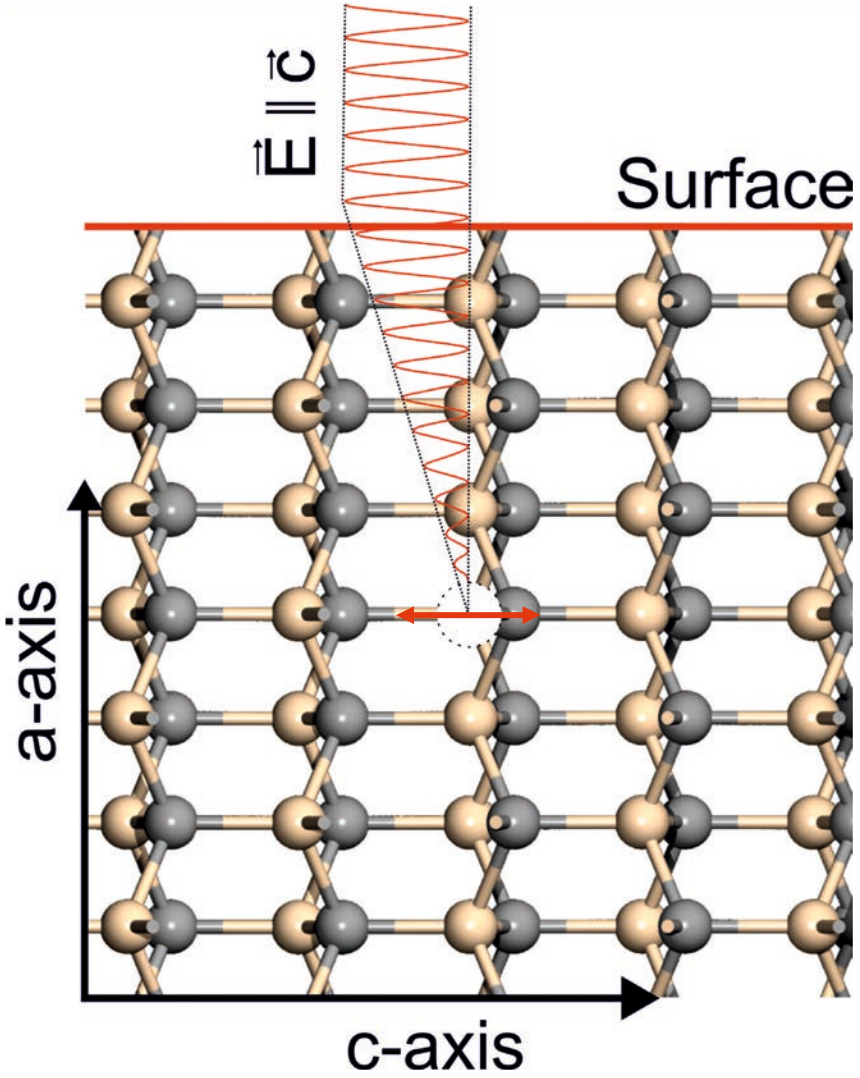


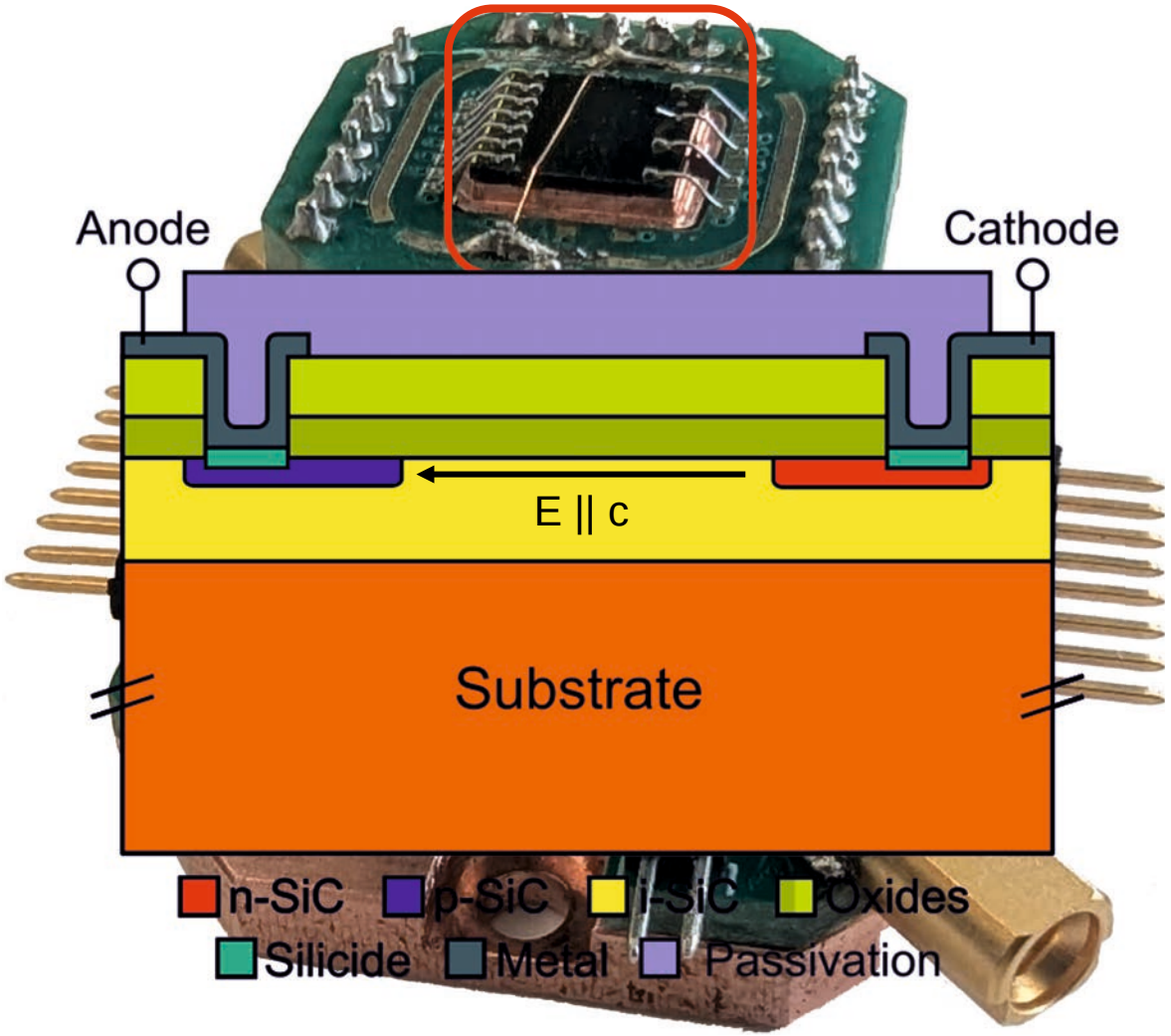
Utilization of a-plane wafers enables wafer-scale resonant excitation

Devices designs must be adapted for changed crystal lattice

N.T. Son, et al., Appl. Phys. Lett. 116 (2020) 190501.
D. Scheller, J.H. Schwarberg, et al., Phys. Rev. Applied 24 (2025). 014036.

Device concept and key processing steps

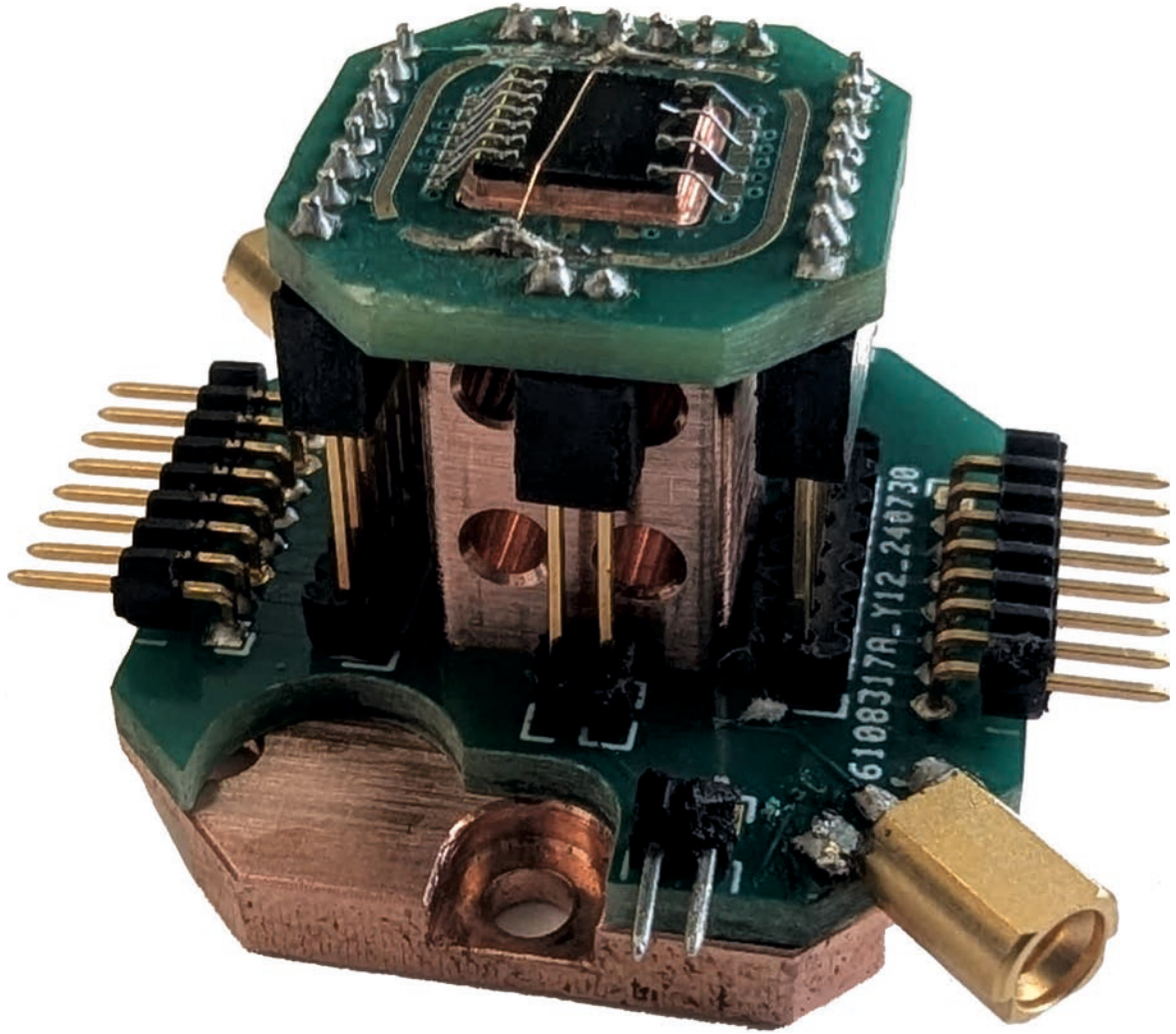


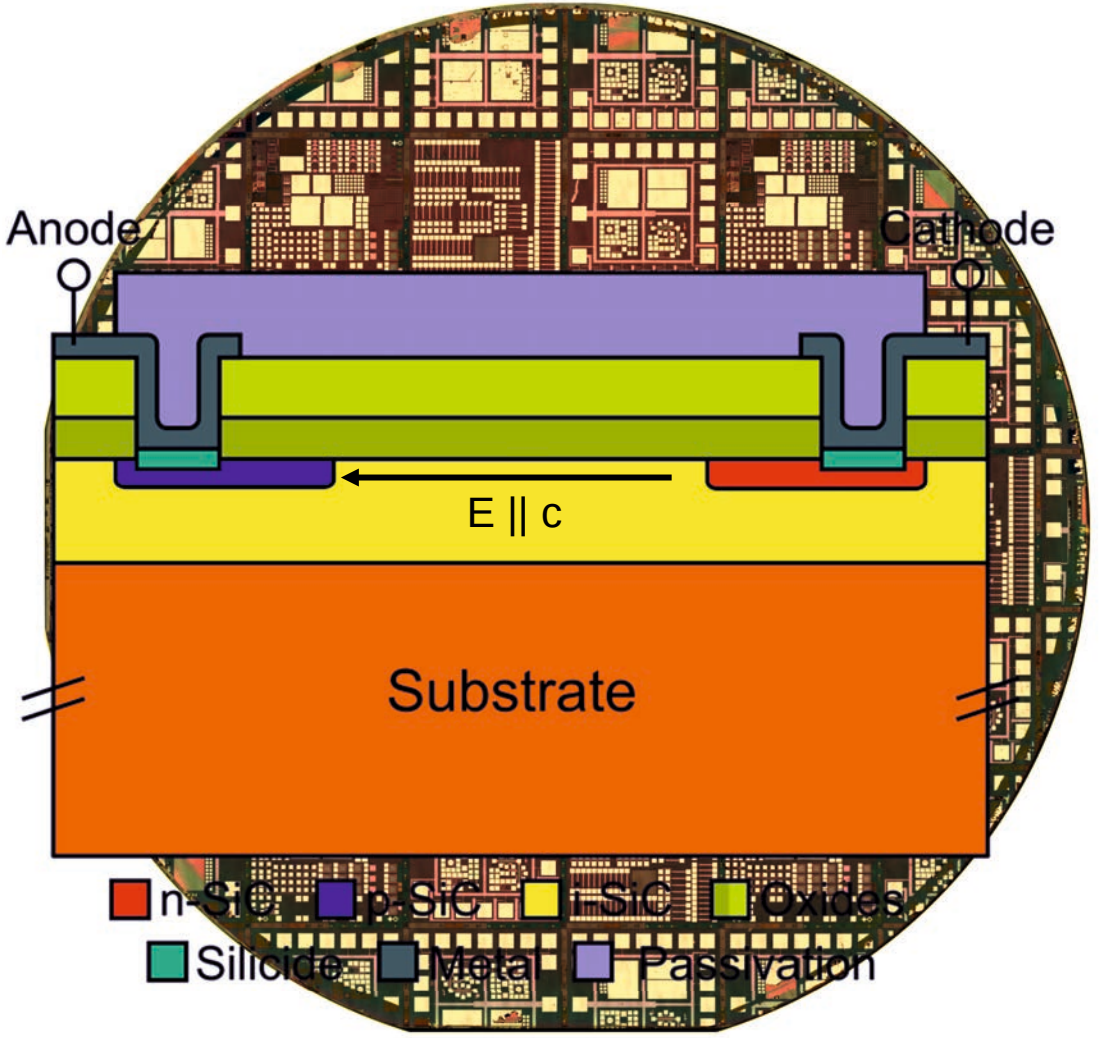


Key CMOS processes like epitaxial layer growth and thermal oxidation are transferred to a-plane wafers

J.H. Schwarberg, in: 2024 47th MIPRO, IEEE, 2024, pp. 1566–1572.

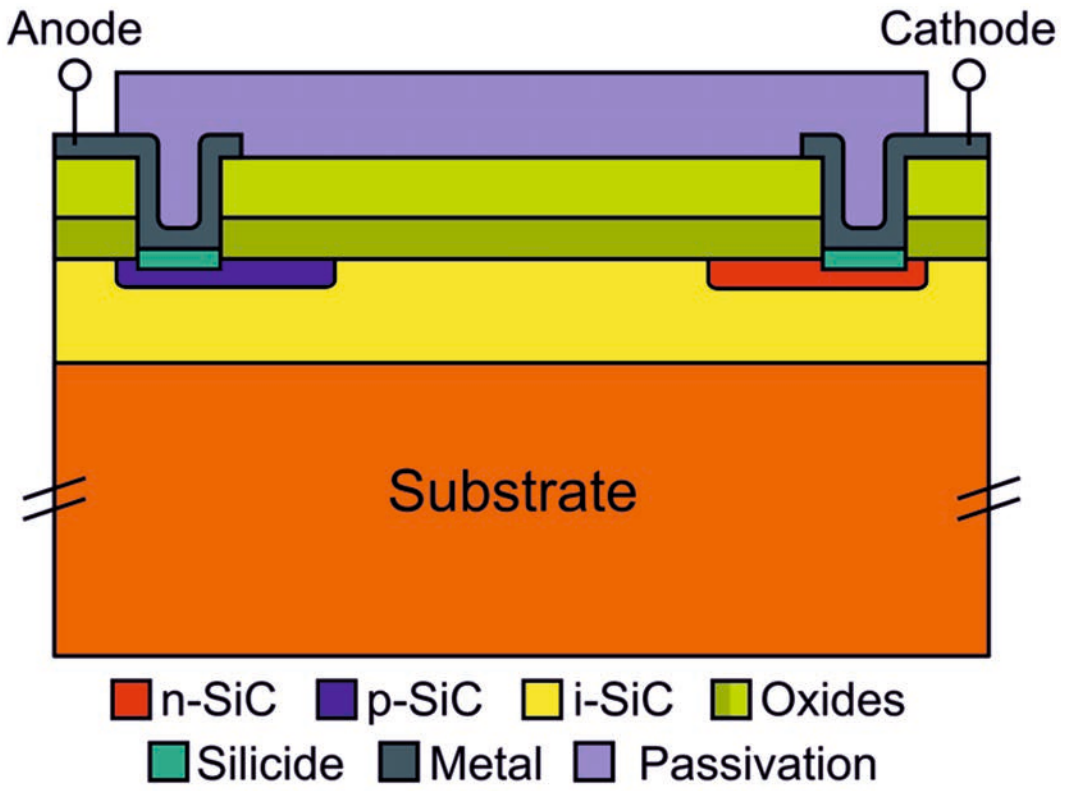
Wafer scale high temperature CMOS-compatible process

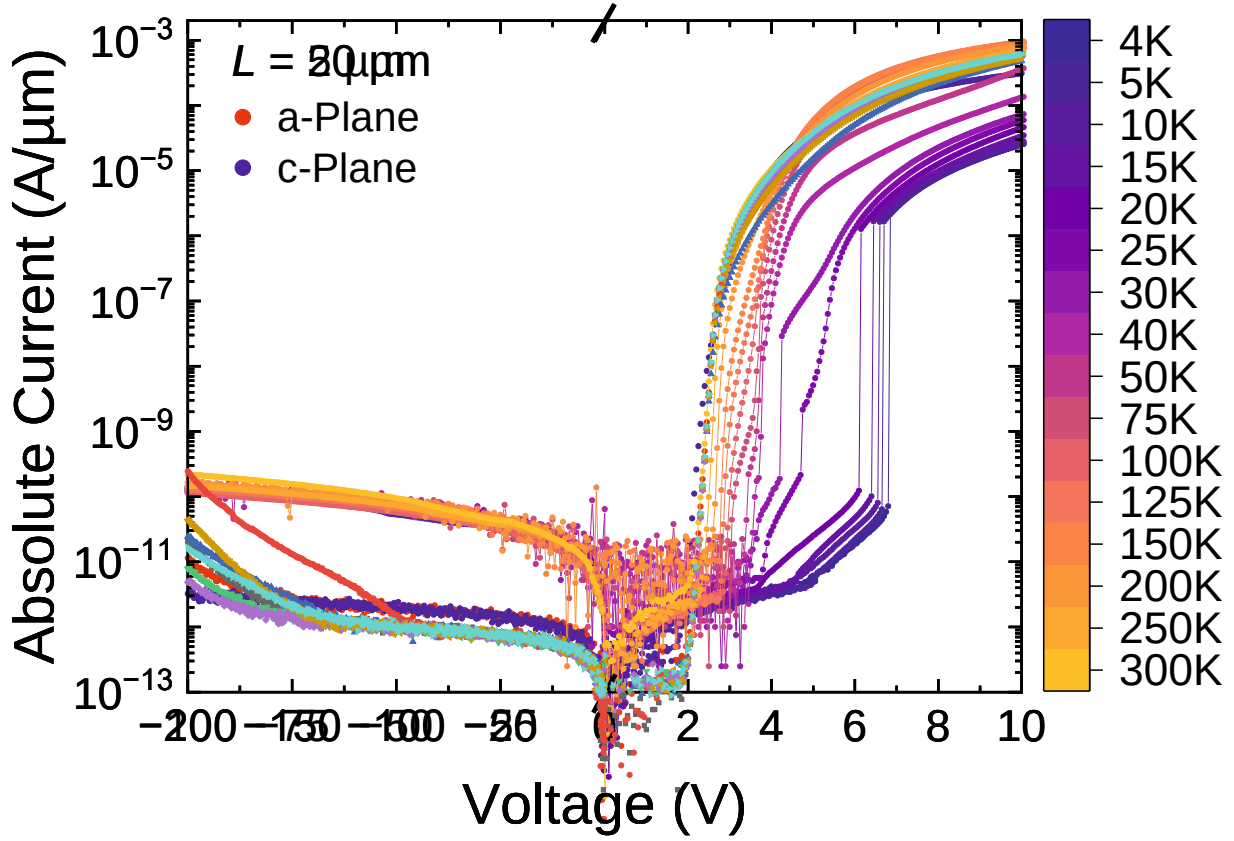




A wafer scale CMOS process on 35 mm a-plane substrates was established

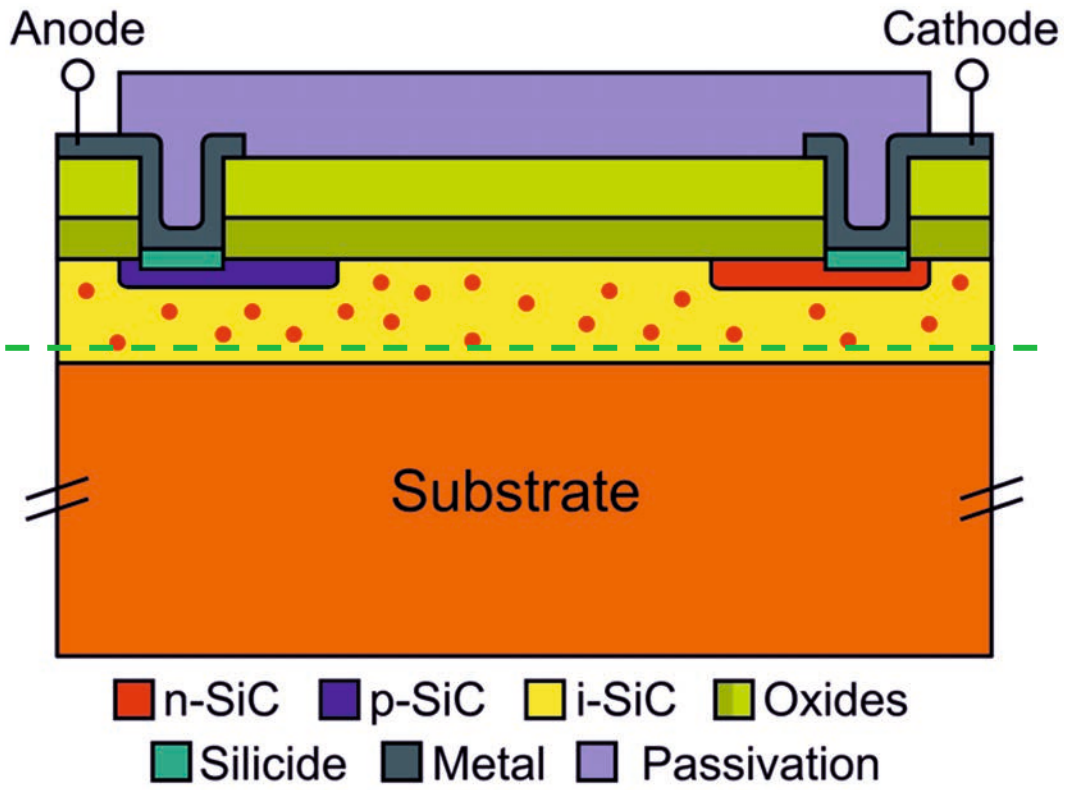
I-V characteristics at 300K and down to 4K

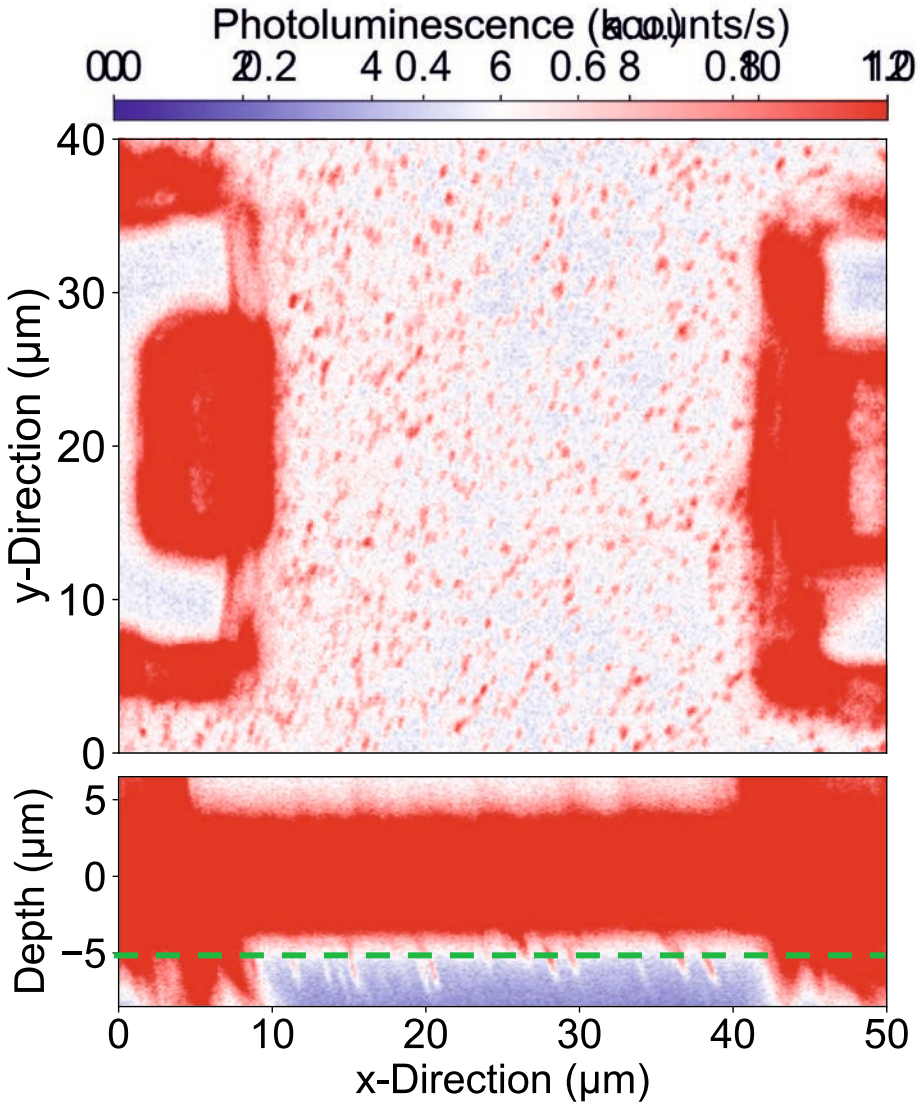




All manufactured devices show good electrical properties with low deviations
At cryogenic temperatures frozen-out dopants must be re-ionized by the electric field

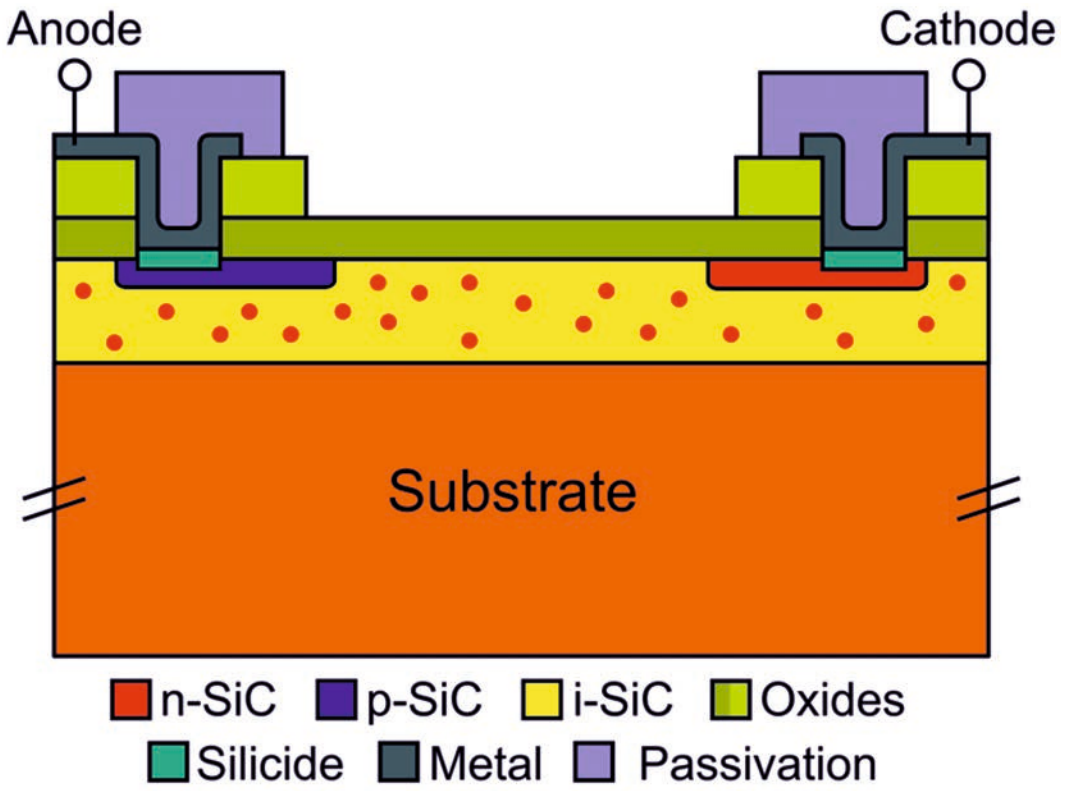
Color centers in lateral pin-diodes on a-plane wafers

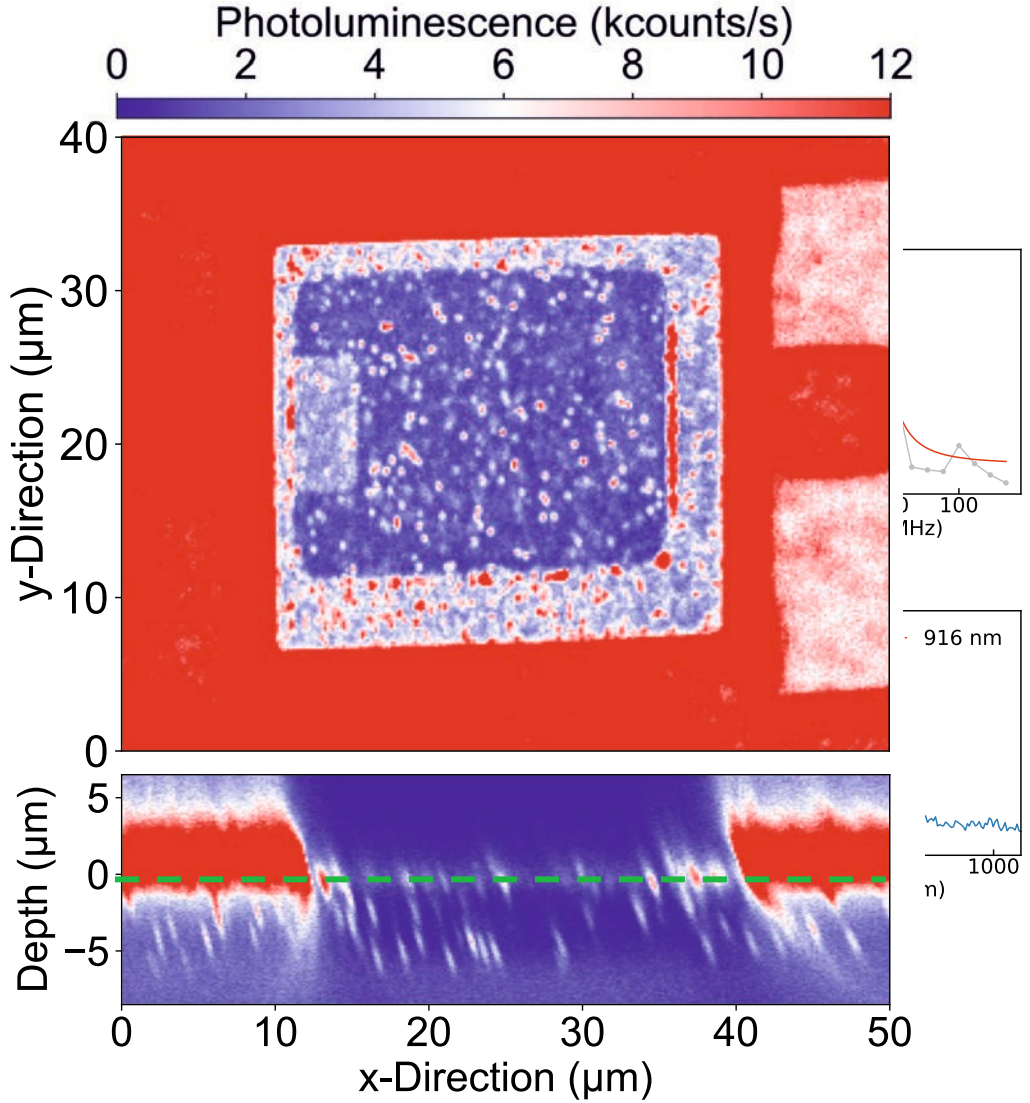




Interfaces and defects in insulation layers overshadow emission of surface-near color centers

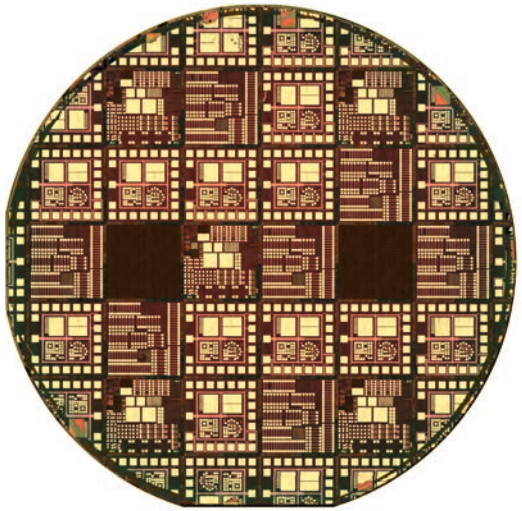
Improved device design for better SNR

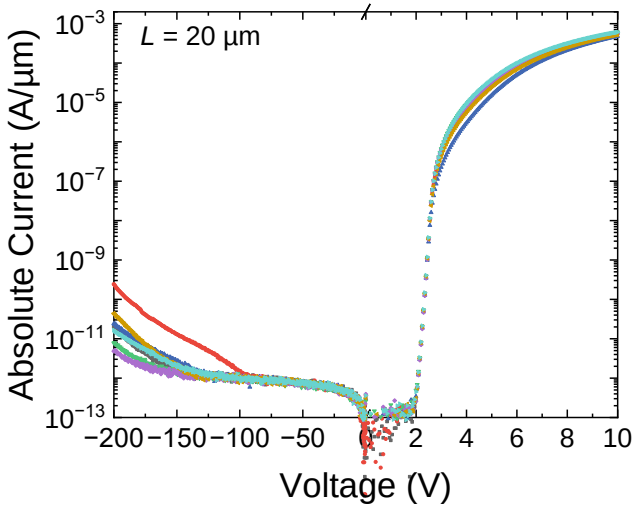


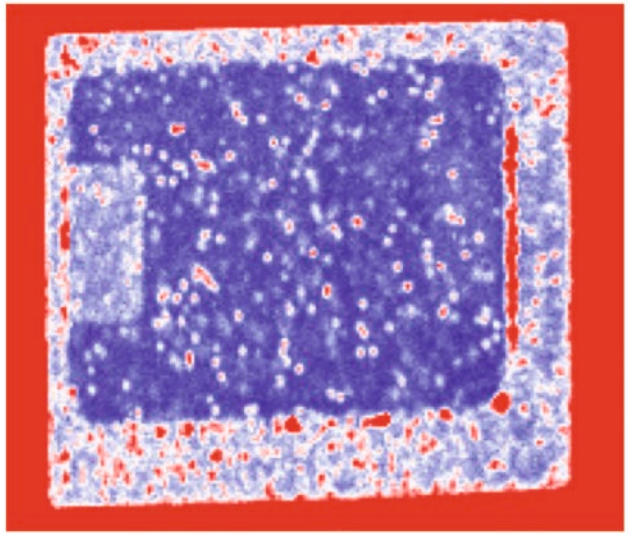


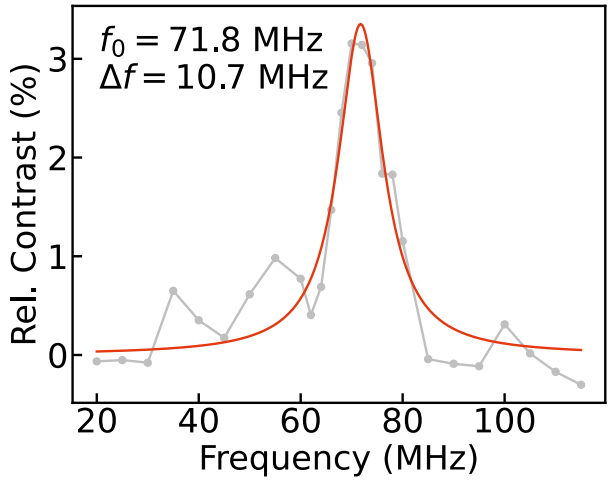
V_{Si} can be generated and measured with good SNR in lateral pin-diodes on 4H-SiC a-plane wafers

Conclusion and Vision

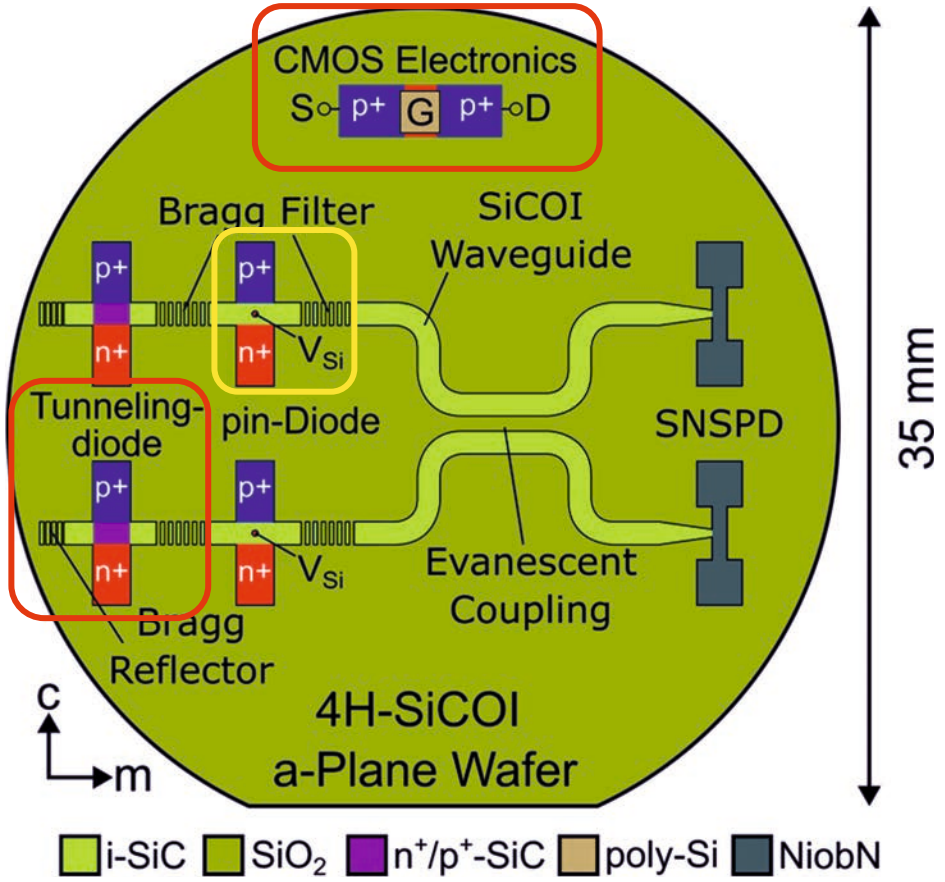








Quantum Integrated Photonik Circuit



Thank you for your kind attention!

Special thanks to all partners:

Fraunhofer IISB

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