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The Tunneling Field-Effect Transistor as Novel Device Concept for High-Frequency Hard-Switching Power Electronics

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Motivation and Device Concept

- Increasing converter power density → shrink energy storing passive components [1]

→ Faster switching to compensate smaller energy storing passive components

- Switching / dynamic loss is a function of the input capacitance of the power switch [2]

→ Goal: Device concept with comparable static and reduced dynamic loss

- Capacitance can be reduced by omitting the channel of a conventional MOSFET and replacing it by a gated p-n junction forming a switchable tunneling contact resembling a tunneling FET with drift zone → **Power-TFET**
- Static loss must be optimized to achieve similar R_{on} by tuning the tunneling junction towards $R_T = R_{ch}$ [3]

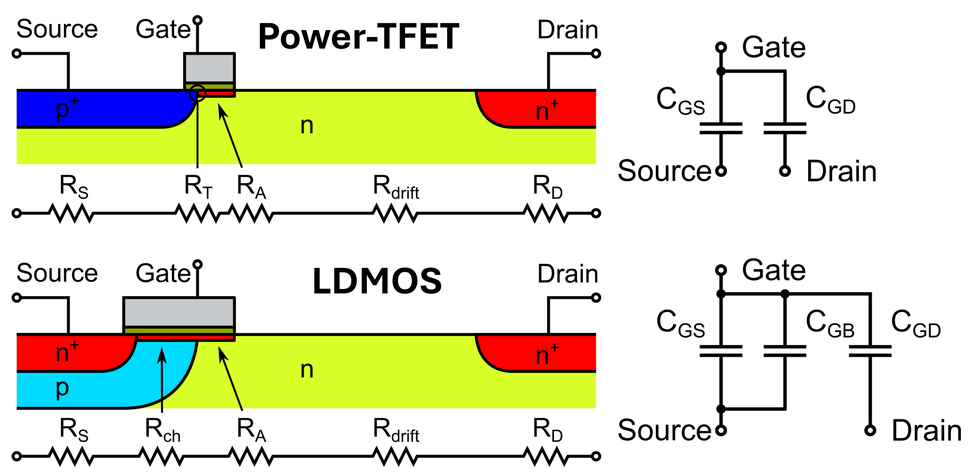

Fig. 1: Schematic of resistive and capaciticve components in a Power-TFET and in a LDMOS

Technology & Measured Electrical Characteristics

- Devices were built on the Fraunhofer IISB 2 µm SiC CMOS process [4]
- Device geometry resembles Fig. 1 with 12 µm drift zone and 2 µm channel
- Transfer characteristics show typical rounded behavior of a TFET [3, 5] (Fig. 2) and a incredibly low conductivity resulting from the tunneling through the 4H-SiC bandgap → Barrier height too high for low on-resistance
- Output characteristic of Power-TFET shows non-linear tunneling breakdown at low V_{DS} and saturation above V_{DS} = 13 V (Fig. 3)
- Breakdown of LDMOS and Power-TFET show similar shape of the characteristic and similar breakdown voltage (Fig. 4)

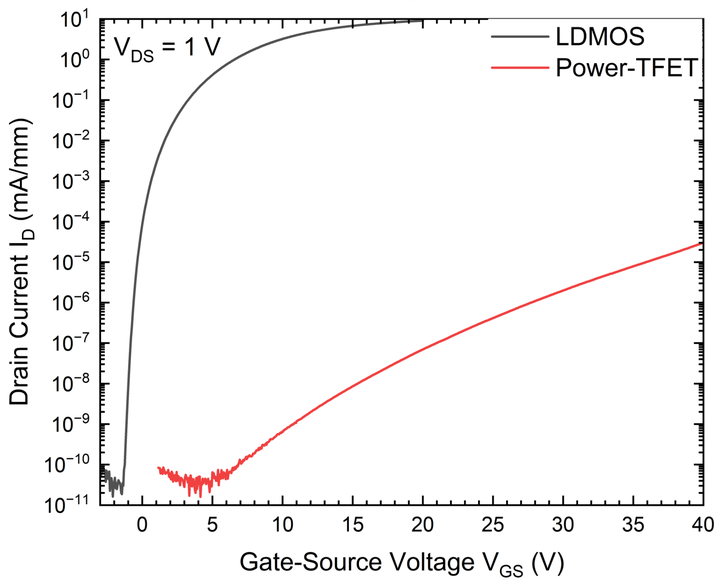

Fig. 2: Transfer characteristics at V_{DS} = 1 V

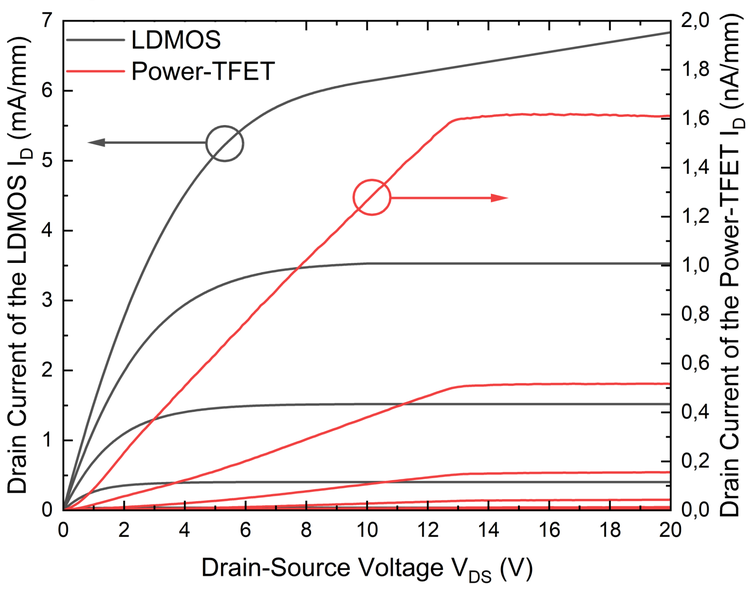

Fig. 3: Normalized output characteristics

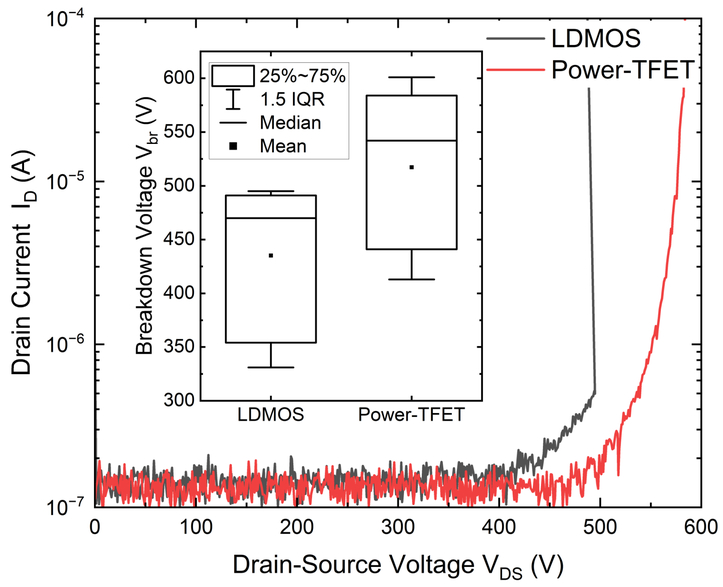

Fig. 4: Breakdown behavior of Power-TFET & LDMOS

Simulative Tunneling Barrier Optimization

- Tunneling through the bandgap of 4H-SiC leads to high tunneling resistance
- Solution: Tunneling at a Schottky barrier, since barrier height can be chosen by material combination → Additional recess of the semiconductor at the Schottky barrier is needed to achieve best field control of the gate underneath the metal
- Low Schottky barrier height leads to a larger leakage current, which can be countered by a junction-barrier-Schottky (JBS) structure, which fully depletes the semiconductor underneath the metal [6]
- Transfer characteristic of the Schottky Power-TFET shows steep subthreshold behavior attributed to the gate induced reduction of the depletion at the metal-semiconductor with subsequent rounded tunnel junction switch-on (Fig. 5)
- On-state current of the simulated Schottky-Power-TFET with 0.6 eV barrier height approaches the on-current of the simulated LDMOS

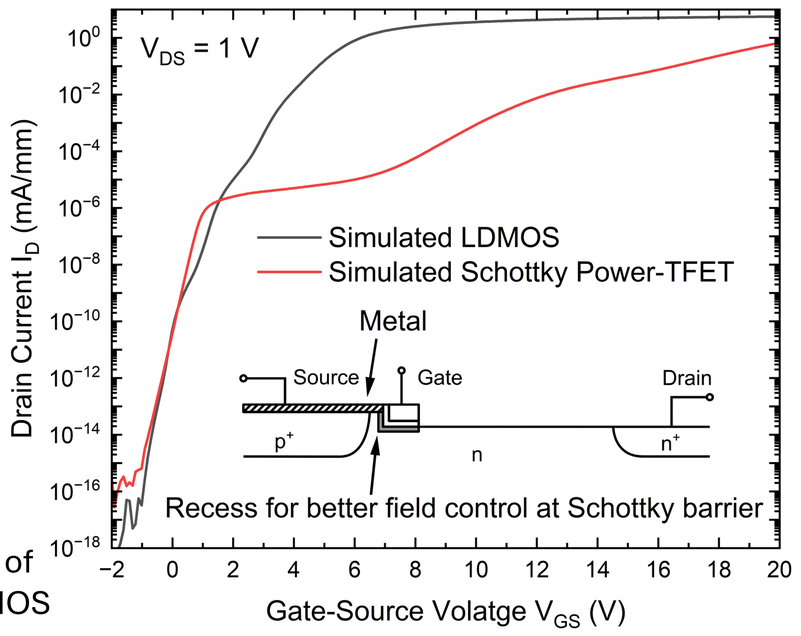

Fig. 5: Transfer characteristics of Schottky-Power-TFET and LDMOS

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