

# Reduction of Sidewall Roughness in SiC Trench Formation by Improvement of Photoresist Mask

Alesa Fuchs, Kevin Ehrensberger, Leander Baier, and Oleg Rusch

alesa.fuchs@iisb.fraunhofer.de

Fraunhofer Institute for Integrated Systems and Device Technology IISB, Schottkystrasse 10, 91058 Erlangen, Germany

## Motivation

- Sidewall roughness in SiC Trenches crucial factor for gate oxide reliability and mobility [1, 2]
  - Typical trench formation process:
    - Photoresist mask patterning, oxide hard mask etch, resist strip, SiC etch
    - Trench sidewall roughness can be influenced by every step and transfers from layer to layer
  - Commonly subsequent sidewall roughness reduction by high temperature annealing step [3]
    - Disadvantage: changing trench geometry → less geometry control
- Goal: Reduction of sidewall roughness from lithography step on

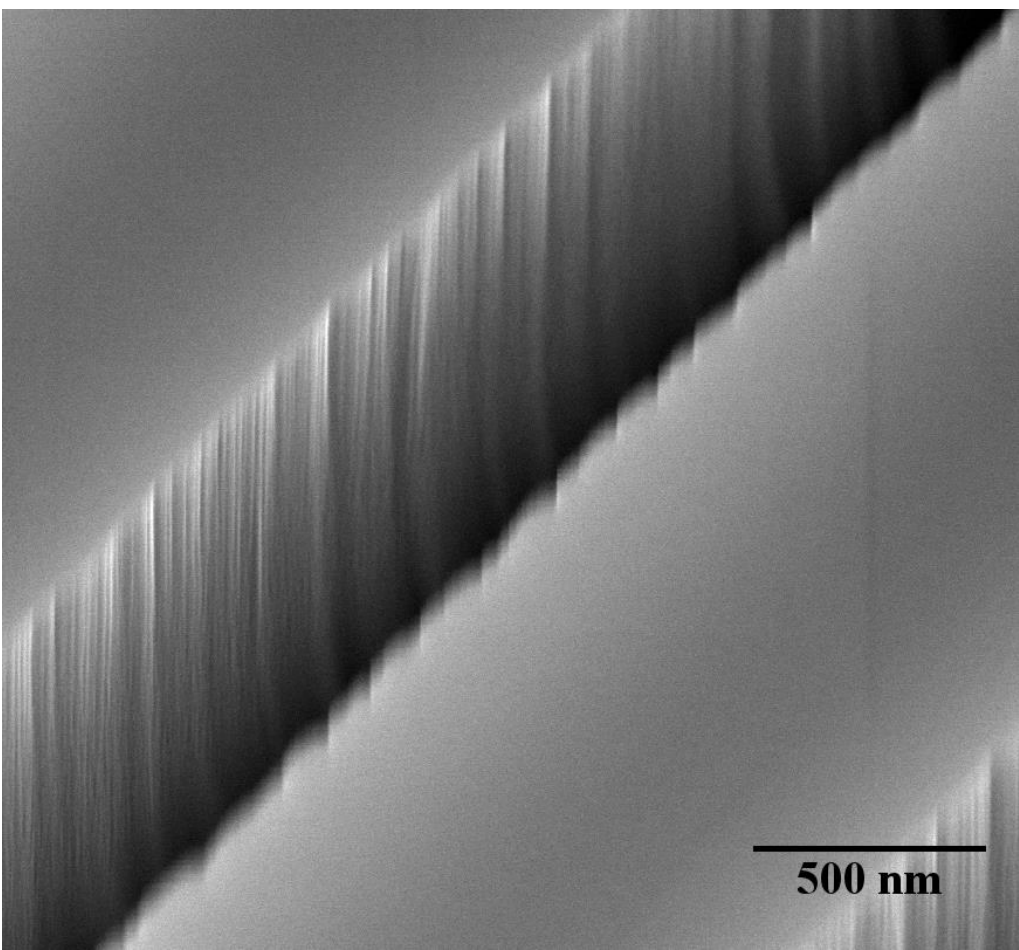


Fig. 1. Oblique view SEM image of SiC trench after dry etching and cleaning. The shown structures are 1 μm wide (drawn on mask).

## Processing

### Lithography

- i-Line exposure, resist thickness 1.5 μm:
  - DNQ-based resist: high resolution positive resist [4]:
    - Exposure dose: approx. 130 mJ/cm<sup>2</sup> (Mask aligner) approx. 170 mJ/cm<sup>2</sup> (Stepper)
  - PEB: 60 s @ 110°C
  - Chemically amplified resist (CAR): thinned i-line sensitive positive resist [5]:
    - Exposure dose: approx. 90 mJ/cm<sup>2</sup> (Mask aligner) approx. 80 mJ/cm<sup>2</sup> (Stepper)
    - PEB: 90 s @ 100°C

### Oxide Etch

- Reactive ion etching (CHF<sub>3</sub> / C3F<sub>8</sub> / Ar) of 1.5 μm TEOS oxide with end point detection

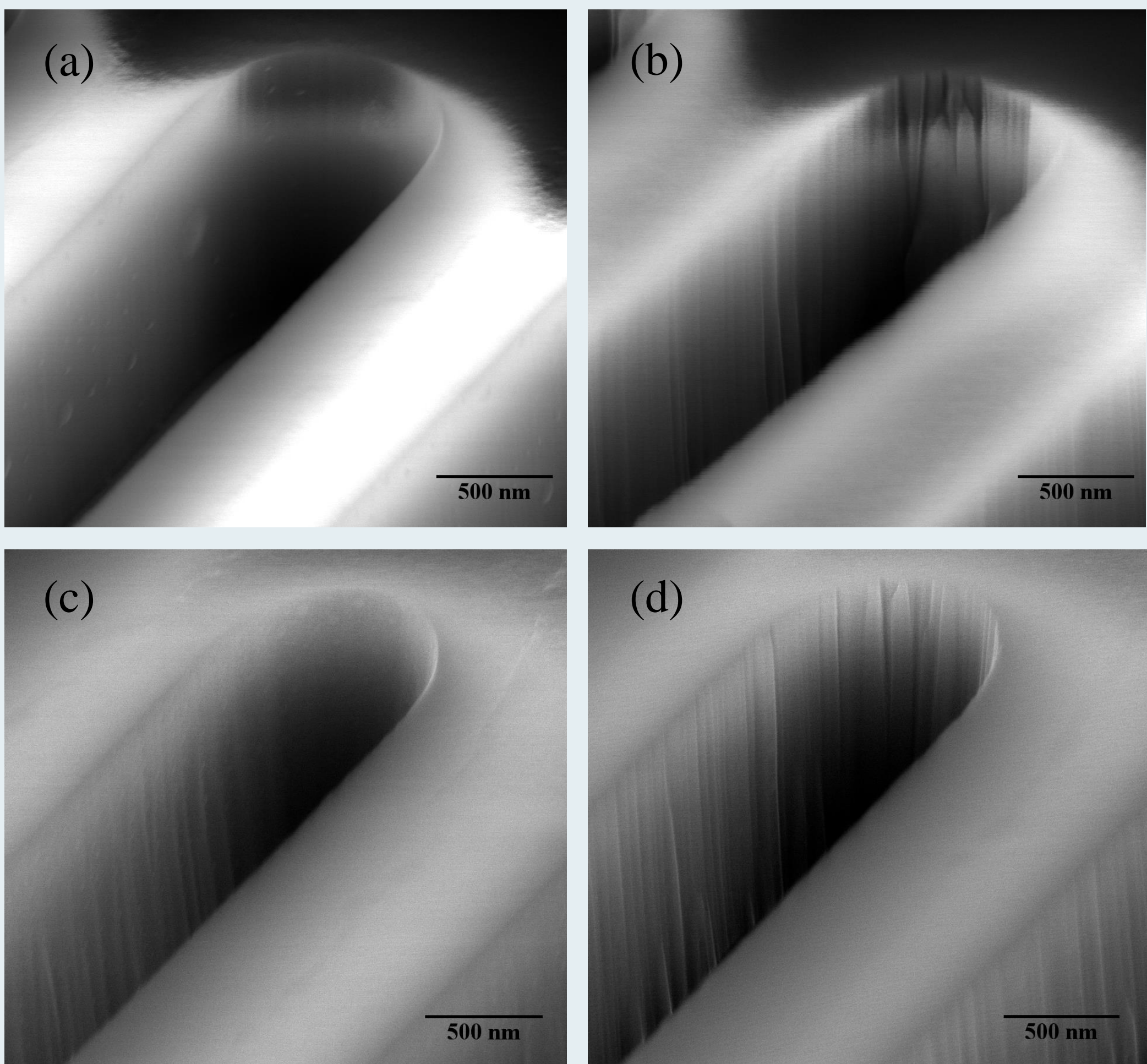


Fig. 2. SEM images of oxide hard mask after dry etching with (a), (c) CAR mask and (b), (d) DNQ-based resist mask (resist already removed) on SiC substrates. Exposure in (a) and (b) was done on a mask aligner, exposure in (c) and (d) was done on a stepper. The shown structures are 1 μm wide (drawn on mask). Oblique view (tilted and rotated) for better visualization of the sidewall roughness.

Table 1. Relative roughness (RR) values gained from profile image analysis of SEM surface images shown in Fig. 2.

	CAR		DNQ	
	Mask Aligner	Stepper	Mask Aligner	Stepper
Exposure Tool	Mask Aligner	Stepper	Mask Aligner	Stepper
Grayscale RR (A.U.)	2.3	9.0	4.8	9.8

## Evaluation

### Profile image analysis

- SEM surface images under 52° tilt
- Grayscale from profile analysis (see Fig. 3)
- Relative roughness (RR) from divergence of normalized grayscale [6]

### Data comparison

- RR compared to root mean square average roughness (R<sub>q</sub>) gained from AFM measurements on sidewalls of tilted samples (only measured on Si substrates, see Table 2)
- Results on Si substrates comparable to SiC, although not completely matchable due to optical properties causing differences in lithography

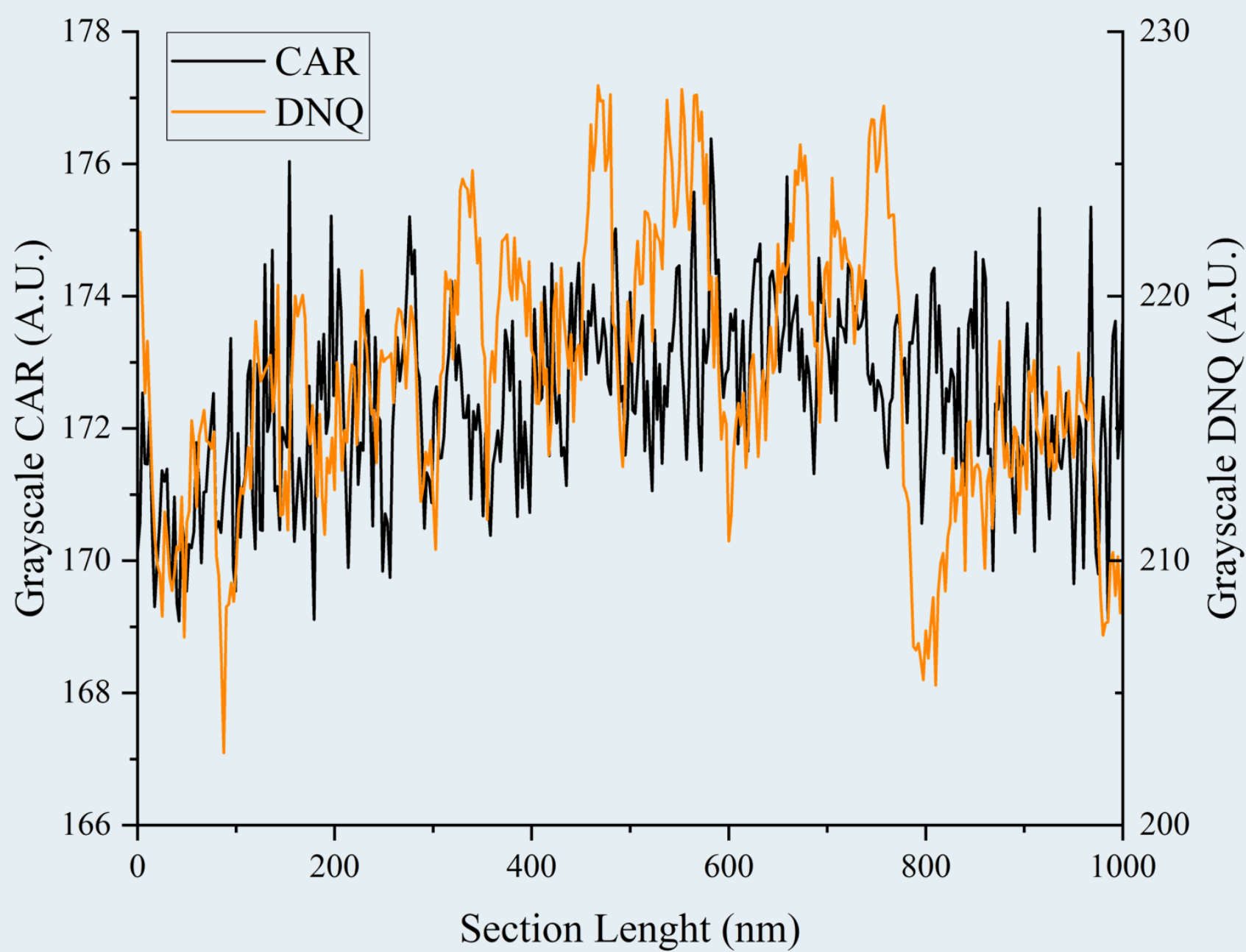


Fig. 3. Profile image analysis evaluation of oxide sidewall (section length 1 μm) of SEM surface images shown in Fig. 2 (a) and (b). Analysis was done in ImageJ.

## Comparison of sidewall roughness values

Table 2. Root mean square average roughness (R<sub>q</sub>) of sidewalls of resist masks and oxide masks (etched with respective resist) measured with AFM compared to relative roughness (RR) values gained from profile image analysis. Samples in this table are Si wafers.

	CAR		DNQ	
	Resist mask	Oxide mask	Resist mask	Oxide mask
AFM R <sub>q</sub> (nm)	4.7	2.2	17.0	18.6
Grayscale RR (A.U.)	-	4.4	-	8.3

## Summary & Outlook

- Reduced photoresist sidewall roughness leads to reduced sidewall roughness in oxide mask used for SiC trench etching
  - Sidewall roughness of CAR smaller than DNQ-based resist
  - Roughness characterization can be simplified by using profile image analysis of SEM images
- Combining oxide mask with reduced sidewall roughness with enhanced SiC etch creating bottom corner rounding [7], trench geometry can be optimized
  - Gentler annealing step enabled and therefore better trench geometry control
- Further characterization of resist- and SiC trench sidewall roughness remaining for deeper insights into roughness transfer in whole trench formation process

[1] K. Kutsuki et al., Jpn. J. Appl. Phys. Vol. 57 (2018), 04FR02.  
[2] T. Kimoto and J.A. Cooper, IEEE (2014), p. 320.  
[3] Y. Kawada et al., Jpn. J. Appl. Phys. Vol. 48 (2009), p. 116508.  
[4] [https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds\\_az\\_eci\\_3000\\_series.pdf](https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds_az_eci_3000_series.pdf)  
[5] [https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds\\_az\\_12xt\\_photoresist.pdf](https://www.microchemicals.com/dokumente/datenblaetter/tds/merck/en/tds_az_12xt_photoresist.pdf)  
[6] M. Barcellona et al., Materials Science in Semiconductor Processing Vol. 174 (2024), p. 108216.  
[7] B. Jones et al., SSP Vol. 359 (2024), p. 163.