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Extraction of trench sidewall capacitance by linear component separation towards wafer level evaluation

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Motivation

- Several gate-oxide processes have been proposed to reduce the density of interface states (D_{it}) [1-3], which decreases the channel resistance and $R_{DS(on)}$.
- Most GOX investigations have only had dielectric performance evaluated on planar MOS capacitors (MOSCap).
- ➔ A scalable method to individually evaluate the trench sidewall, bottom and edge capacitances is mandatory for device optimization.

Device Fabrication

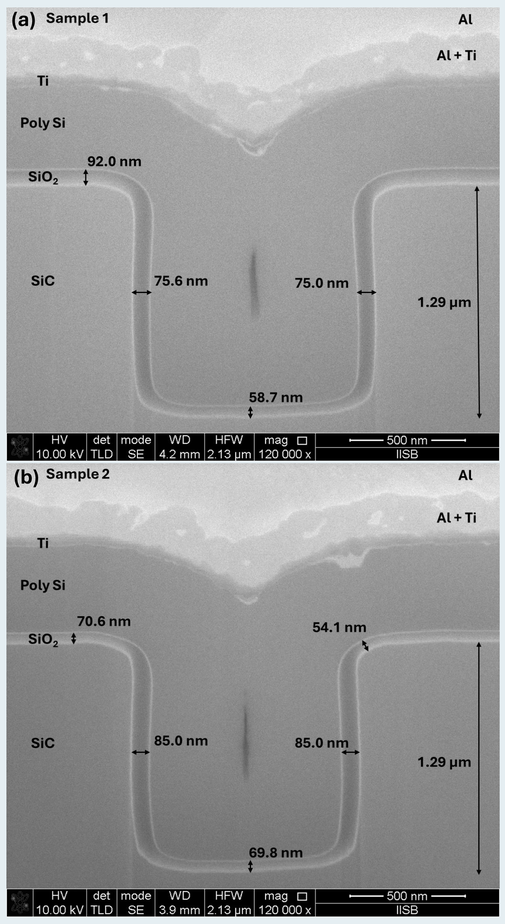

Fig. 1. Focused ion beam (FIB) cross-section SEM images of fabricated trench MOSCaps. a) Sample 1 LPCVD TEOS oxide and b) sample 2 with LPCVD polysilicon oxidized at 850 °C. Both samples were annealed in NO at 1300 °C for 1 h.

TZDB

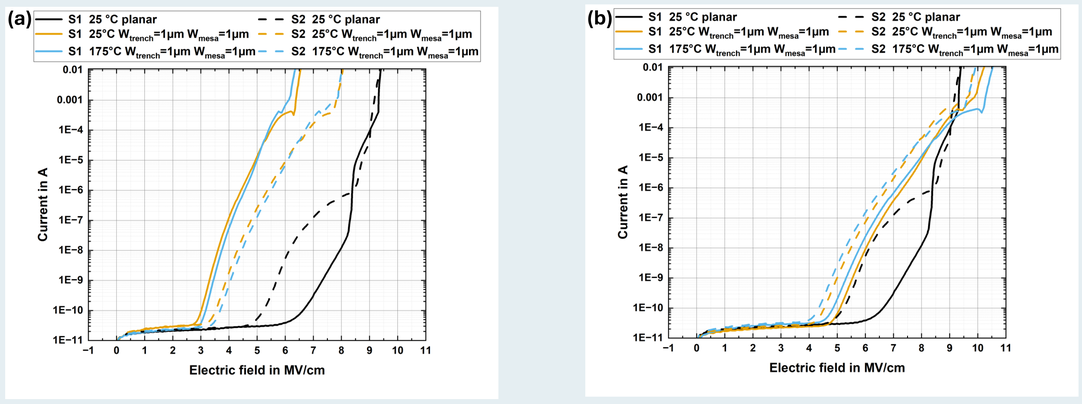

Fig. 2. Average leakage current-electric field curve of forty devices for different designs. a) The electric field for the planar and trench designs is calculated using the planar mesa oxide thickness measured by ellipsometry. b) The electric field for the trench designs is calculated using the lowest measured oxide thickness determined by focused ion beam cross-section SEM imaging instead.

- Using mesa oxide thickness measured by ellipsometry underestimates the trench MOSCap breakdown field.
- Using FIB-SEM oxide thickness is more accurate but still overestimates because it ignores electric-field/current crowding at the trench bottom.
- Accurate values require local t_{OX} and a 2D field/crowding correction.

Summary

- Separation of the different capacitance components of SiC trench MOSCaps is possible.
- The error of the fitting can be optimized by carefully selecting the areas of the fabricated devices.
- The method has to be further optimized by detailed geometric and physics modeling using TCAD.

Capacitance

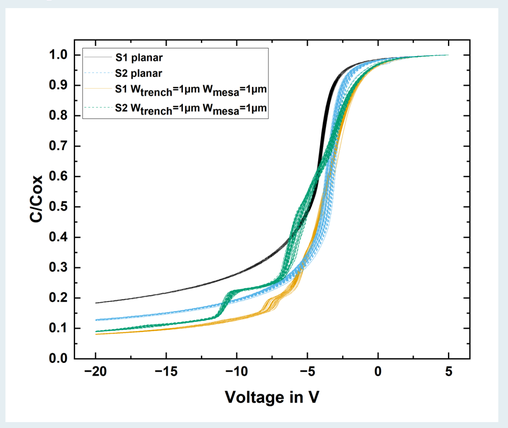

Fig. 3. Normalized capacitance–voltage (C–V) measurement at 100 kHz of 40 devices with planar and trench design on sample 1 (TEOS oxide) and sample 2 (oxidized poly Si).

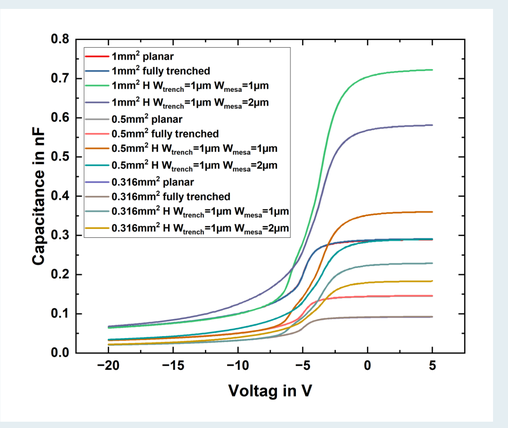

Fig. 4. Capacitance–voltage (C–V) measurement at 100 kHz of 12 different designs with varying area on sample 1.

- Trench MOSCaps differ notably from planar devices on the same wafer.
- Causes: oxide thickness variation, electric-field crowding at corners, space-charge region extension, charge trapping and flat-band voltage.

Linear Component Separation

Trench MOSCaps are modelled as three parallel components: mesa C_m, sidewall C_s, and bottom C_b. Knowing the respective areas allows for determination of the different capacitances by solving a linear system of equations [4]:

$$C(V) = A_m C_m(V) + A_s C_s(V) + A_b C_b(V).$$

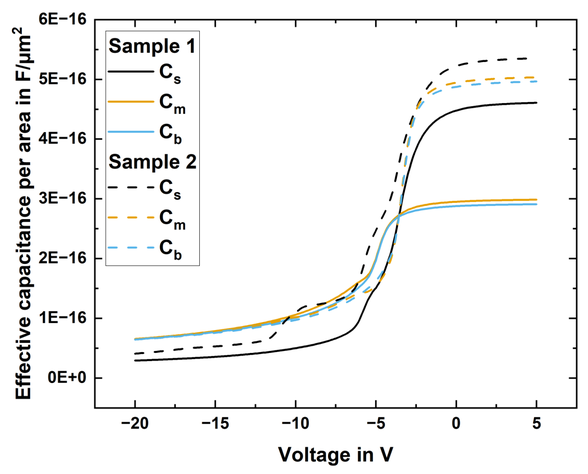

Fig. 5. Separated per area capacitance calculated via pointwise least-square fit of a linear system of equations consisting of the C-V measurements of 12 different design types displayed in Fig. 4 with varying capacitor component areas.

Determination of D_{it}

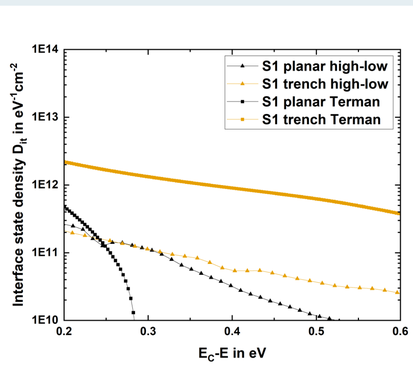

Fig. 6. Average D_{it} of four devices determined by the high-low and Terman method for a planar and trench design with 1 µm trench width and 1 µm mesa width and an area of 1 mm² on sample 1.

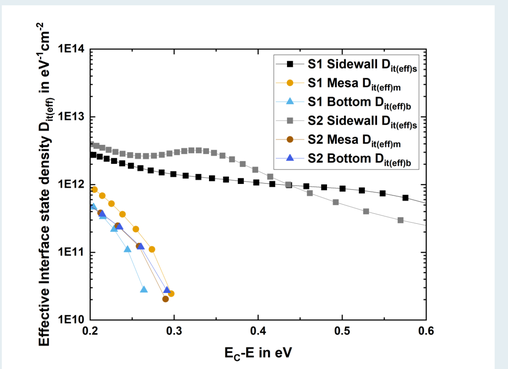

Fig. 7. Effective D_{it} calculated from the effective capacitance depicted in Fig. 6 using the Terman method for the top, bottom and trench sidewall for sample 1 and 2.

- The effective D_{it} is not yet quantitatively accurate.
- However the effective D_{it} mesa and bottom correlates to the measured D_{it} for the planar devices and the effective D_{it} for the trench to the sidewall.
- It is well suited for ranking gate-oxide processes and wafer-to-wafer trends.
- Main limitations are area calibration, local t_{OX} non-uniformity, and unmodeled 2D crowding/fringing.

1 T. Keita et al. Appl. Phys. Express. 13 121002 (2020).
2 T. Kobayashi et al. Appl. Phys. Express 13 091003 (2020).
3 MW. Lim et al. MSF. 1004, 535–40 (2020).
4 Z. Guo et al. IEEE Trans. Electron Devices, vol. 68, no. 6, pp. 2879-2885 (2021).