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IISB² Topology for 48 V to 1 V Point of Load Applications

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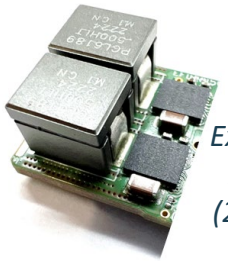
Application example: Point of Load (PoL) DC/DC converter for Server & Memory in data centres

How much energy is needed?

2022		2030		
Gross elect. power consumption Germany 2022 [1]	ca. 550 TWh	Estimated elect. power consumption 2030 [5]	ca. 655 TWh	
ICT energy demand [*] in 2015… 2025 [2]	ca. 45 TWh	Assumption for 2030: ICT needs ca. 10 % [**]	ca. 65 TWh	
ICT infrastructure in Jahr 2022 [3]	ca. 24 TWh	ICT infrastructures in 2030 [3]	ca. 18…**30**…58 TWh	
power grid [3]	ca. 6 TWh	power grid [3]	ca. 4 TWh	
data centre [3] [4]	ca. **18 TWh**	**data centre** [3] [4]	~~ca. **26 TWh**~~	**32 TWh** [6]
Server & Memory [4]	**ca. 11 TWh**	**Server & Memory** [4]	~~**ca. 16 TWh**~~	**20 TWh** [6]

~~+45~~ **+81%**

relevant for PoL



Example for a typ. 12 V → 1 V PoL (2x 40 $A_{cont.}$ units)

[*] Gebäudeversorgung, Öffentlichkeit, IKT Haushalte, IKT Arbeitsplatz, Telekommunikation, Rechenzentren
[**] with data from [2]
[1] AGEB Energieverbrauch in Deutschland im Jahr 2023
[2] Stobbe et al.: Entwicklung des IKT-bedingten Strombedarfs in Deutschland, FhG IZM & Borderstep Institut, 2015
[3] Büro für Technologiefolgenabschätzung beim Deutschen Bundestag: Energieverbrauch der IKT-Infrastruktur, TAB-Fokus Nr. 35 zum Arbeitsbericht Nr. 198, 2022
[4] Bitcom e.V.: Rechenzentren in Deutschland Aktuelle Marktentwicklungen – Update 2023
[5] Pressekonferenz des Wirtschaftsministers Peter Altmaier am 13.7.2021
[6] Bitkom: Rechenzentren in Deutschland, Aktuelle Marktentwicklungen – Stand 2024

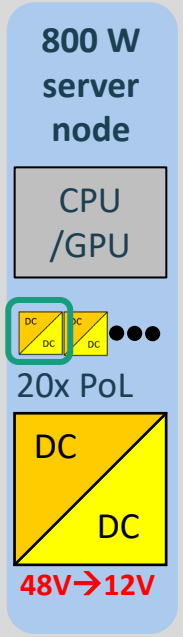
Application example: Point of Load (PoL) DC/DC converter for Server & Memory in data centres

1x Rack ≈ up to 36x 800 W server nodes with ≈ 36x20x PoL

Rack input power ≈ 34 kW

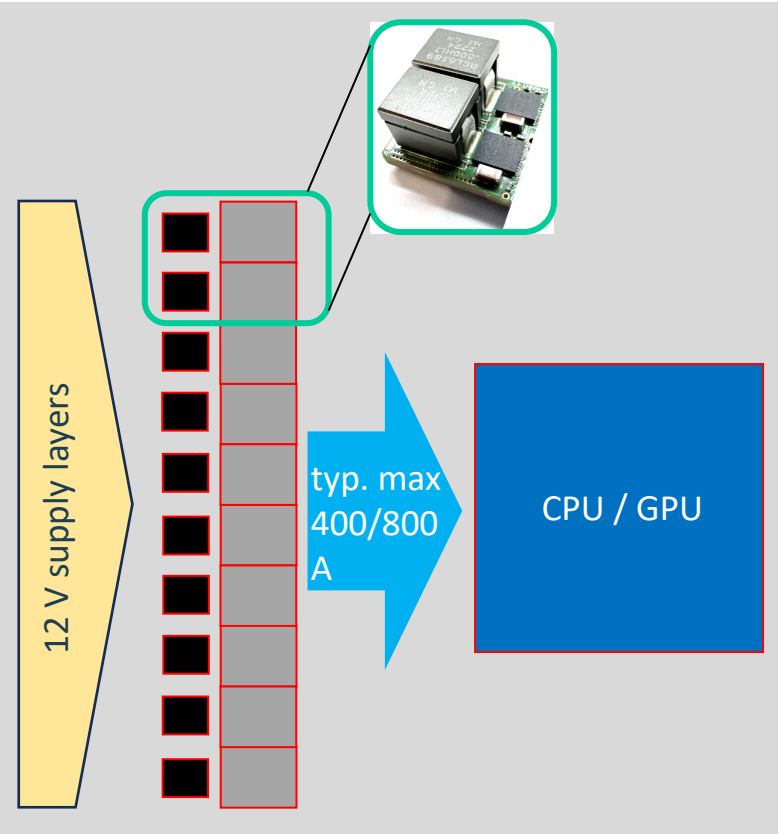
≈ 675 A @ 48 V

1x 800 W server node ≈ 2x CPU or 1x GPU with ≈ 20x PoL



Server nodes supplied with 48 V in high density rack server (blade server)

up to ≈ 400 A for CPU or ≈ 800 A for GPU ≈ 10x PoL for 1 CPU or 20x PoL 1 GPU



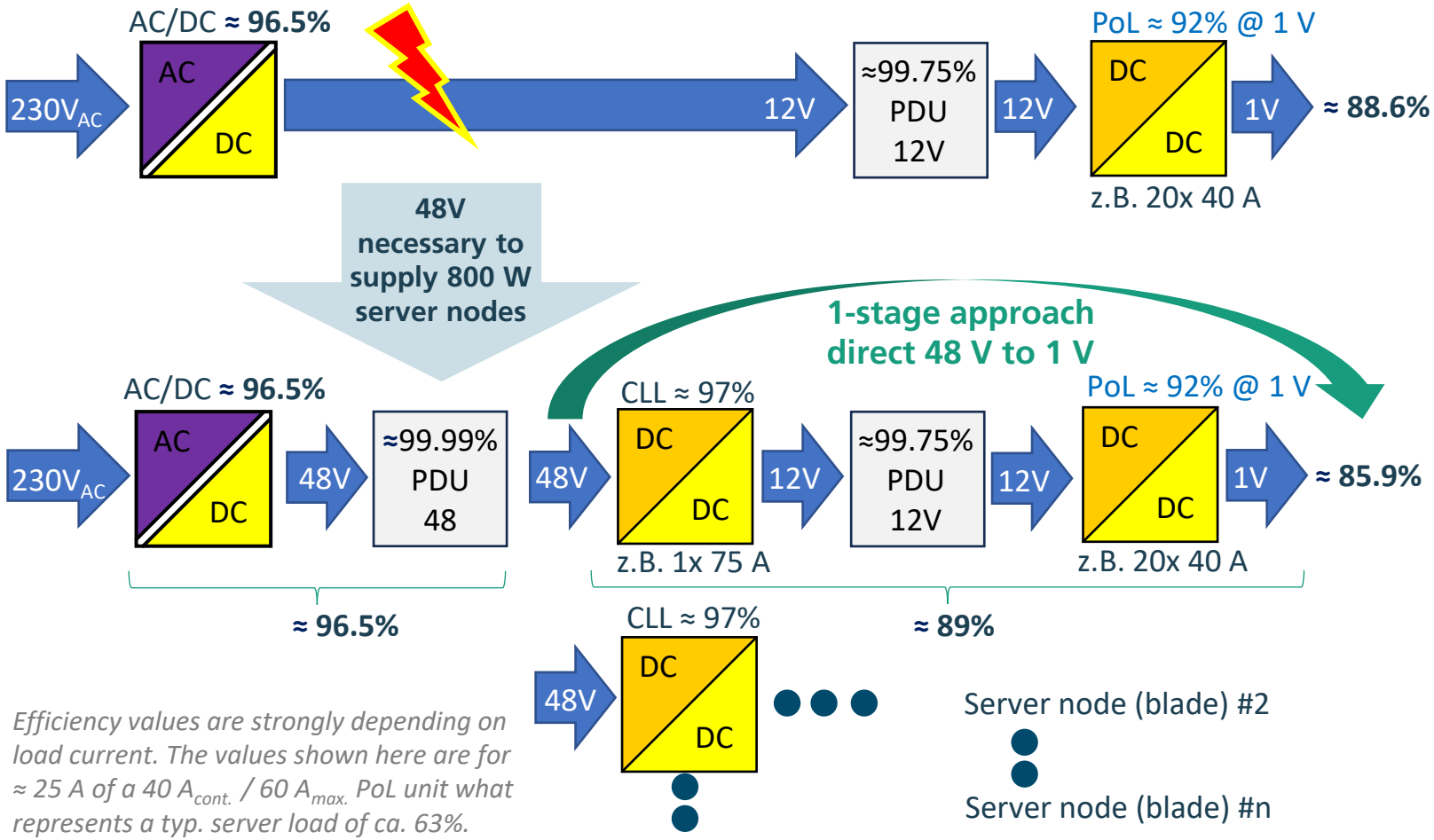
to supply so many server nodes 48 V necessary

→ 230 V_{AC} → **48 V_{DC}** → **12 V_{DC}** → **1 V_{DC}**

greenict Forschungsfabrik Mikroelektronik Deutschland
Bundesministerium für Bildung und Forschung
Fraunhofer IISB

Application example: Point of Load (PoL) DC/DC converter for Server & Memory in data centres

Typical approach: 2 conversion stages 48 V → 12 V & 12 V → 1 V



Efficiency values are strongly depending on load current. The values shown here are for ≈ 25 A of a 40 $A_{cont.}$ / 60 $A_{max.}$ PoL unit what represents a typ. server load of ca. 63%.

Typical approach to save energy (by increasing efficiency)

→ **direct 48 V to 1 V conversion**

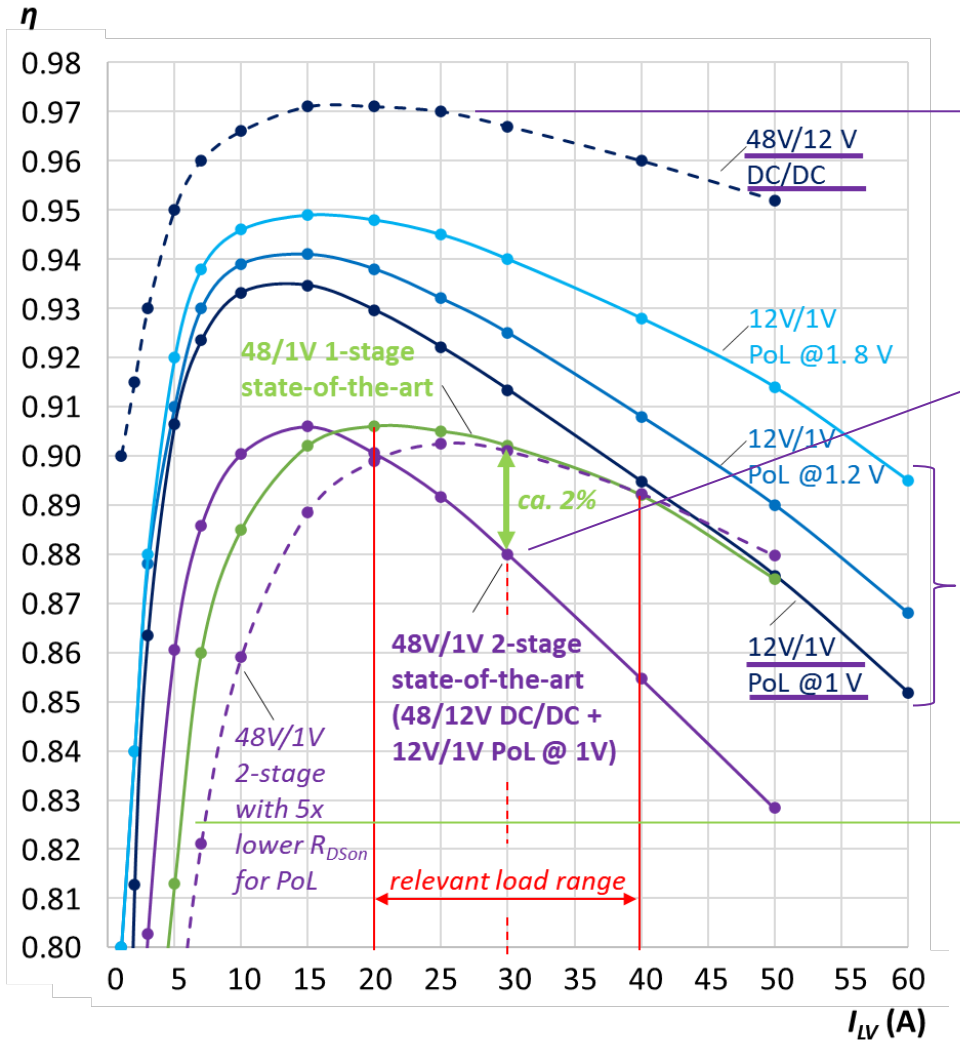
Many examples for direct 48 V to 1 V PoL solutions are known.

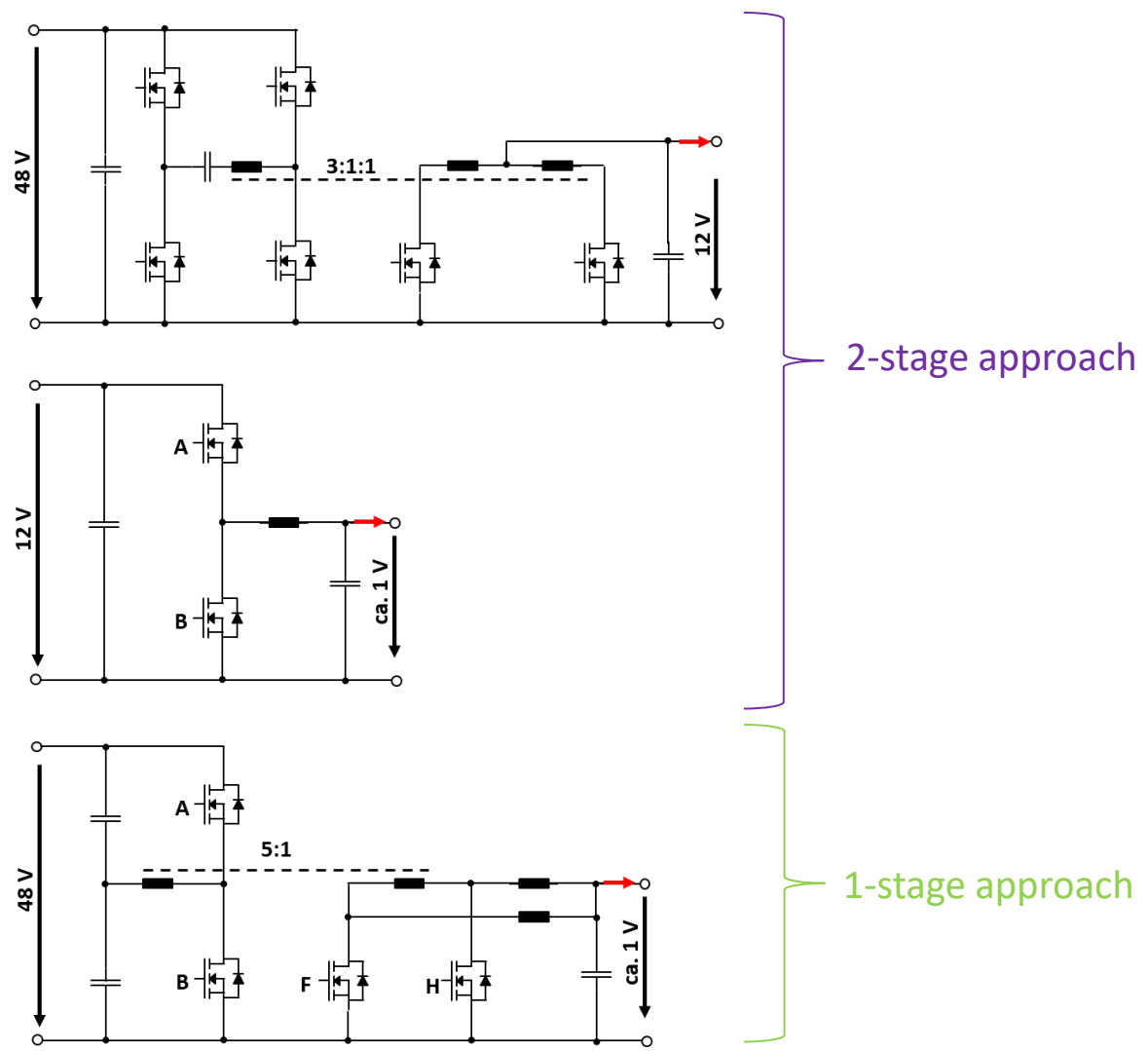
State-of-the-art solutions are based on topologies using a half-bridge and a current doubler rectifier.

Some problems:

- available area and volume
- costs
- voltage range necessary
- high dynamic requirements

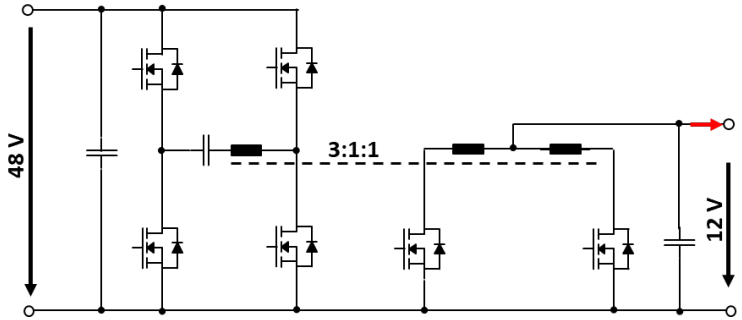
State-of-the-art 2-stage and 1-stage approaches



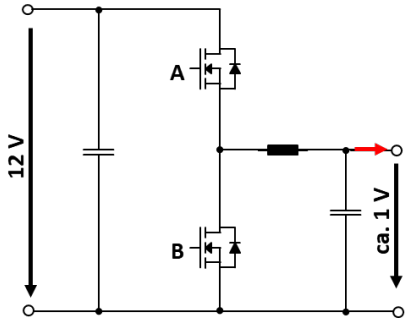


State-of-the-art 2-stage approach

1x 48 V → 12 V



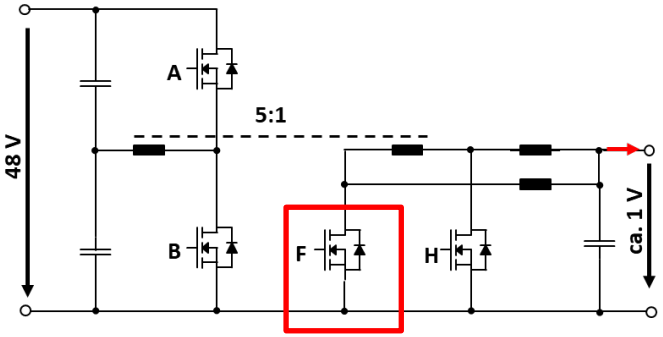
plus 20x 12 V → 1 V



2-stage solution			1-stage solution			
Qty	**1x 48V/12V + 20x 12V/1V, 40A → 800A @ 1V**	**Sum**	**Qty**	**16x 48V/1V, 50A → 800 A @ 1V**	**Sum**	**Ratio 1-stage/ 2-stage**
4	EPC 2619 100 V, 4.2 mOhm, GaN; Die: 2.5x1.5 mm	15 mm²	16	LMG5200 80 V, 15 mOhm, GaN (6x8 mm); est. 3.6x less area due 3.6x higher Rdson →2x(2.5x1.5) /3.6 =2.1 mm²+2.5 mm³ for driver	16x 4.6 mm² =74 mm²	74/ (15+5+ 56+2+ 10) =0.84≈1
2	UP1966P (pri. Gatedriver); Die ca. 1.6x1.6 mm	estim. 5 mm²				
6	EPC 2067 40 V 1.55 mOhm; Die: 2.85 x 3.25 mm	56 mm²	-	-	-	
2	LMG1020 (sec. Gatedriver) Die Size: ?	estim. 2 mm²				
1	dsPIC33CK64MP 105 FAMILY in 4x4 mm Package	estim. 10 mm²	-	-	-	
1	Transformer 3:1:1 for 83 A @ 12 V with 2x ML91S and 4x ML95S Ferrit cores @ ca. 1.6 MHz	estim. 10 g	16	Transformer 5:1 for 50 A @ 1 V with 2x ER18/3.2/ 10-3F36-S Ferrit cores @ 600 kHz	16x 3.2 g =51 g	51/10 = 5.1
14	22 nF resonant capacitor		-	-	-	
20	e. g. MP86957 BOT MOSFET ca. 1.6 mOhm, Si (6x5 mm)		16x 4 =64	4x EPC2023 30 V, 1.3 mOhm, GaN (6.05x2.3 mm)		0.325 /16 /(1.6/20) = 0.25
20	e.g.PGL6076.131 130 nH max. 60 A, 0.16 mOhm @ 500 kHz (7.6x7.6x12 mm)		16x 2 =32	e.g. Würth 744308025, 250nH, 27 A, 0.37 mOhm, (10x7x6.8 mm)		

State-of-the-art 1-stage approach

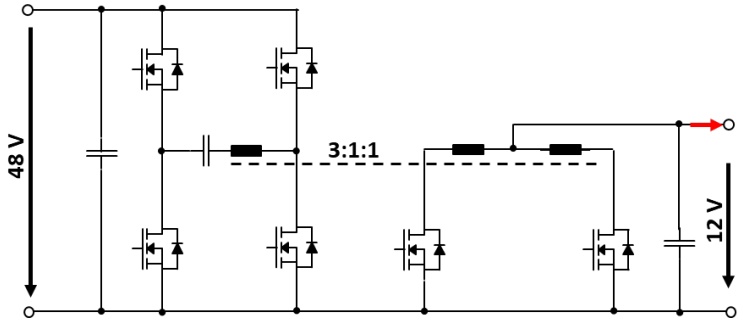
16x 48 V → 1 V



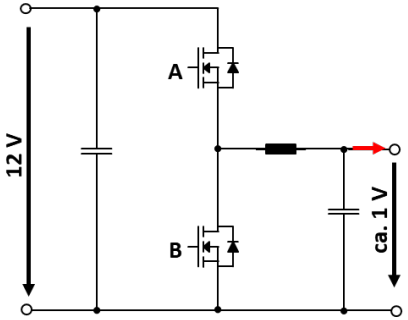
0.65 mOhm
GaN

State-of-the-art 2-stage approach

1x 48 V → 12 V



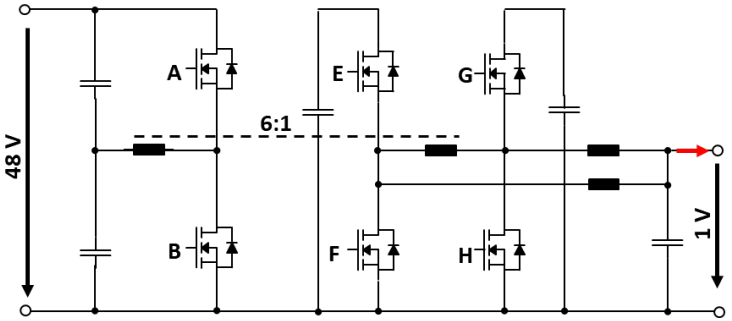
plus 20x 12 V → 1 V

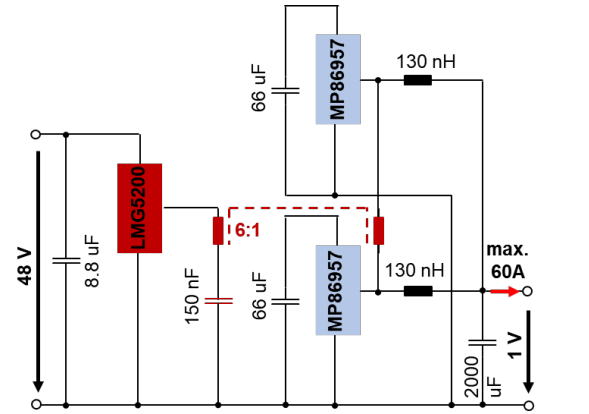


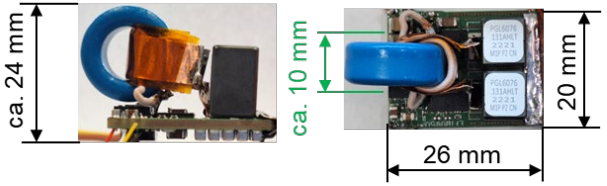
2-stage solution			1-stage iib² solution			Ratio 1-stage/ 2-stage
Qty	**1x 48V/12V + 20x 12V/1V, 40A → 800A @ 1V**	**Sum**	**Qty**	**20x 48V/1V, 40A → 800 A @ 1V**	**Sum**	
4	EPC 2619 100V, 4.2 mOhm, GaN; Die: 2.5 x 1.5 mm	15 mm²	20	LMG5200 80V, 15 mOhm, GaN (6x8 mm); estim. 3.6x less area due 3.6x higher R_{dson} →2x(2.5x1.5)/3.6 = 2.1 mm² + 2.5 mm² for driver	20x 4.6 mm² =92 mm²	92/ (15+5+ 56+2+ 10) =1.05≈1
2	UP1966P (pri. Gatedriver); Die ca. 1.6 x 1.6 mm	estim. 5 mm²				
6	EPC 2067 40V 1,55 mOhm; Die: 2.85 x 3.25 mm	56 mm²	-	-	-	-
2	LMG1020 (sec. Gatedriver) Die Size: ?	estim. 2 mm²				
1	dsPIC33CK64MP 105 FAMILY in 4x4 mm Package	estim. 10 mm²	-	-	-	
1	Transformer 3:1:1 for 83 A @ 12 V with 2x ML91S and 4x ML95S Ferrit cores @ 1.6 MHz	estim. 10 g	20	Transformer 6:1 for 50 A @ 1 V with R16x9.6x6.3, N49 @ 410 kHz	20x 3.7 g =74 g	74/10 = 7.4
14	22 nF resonant capacitor		20	150 nF resonant capacitor		20/14 =1.4
20	e. g. MP86957 BOT MOSFET ca. 1.6 mOhm, Si (6 x 5 mm)		20x 2 =40	e. g. MP86957 BOT MOSFET ca. 1.6 mOhm, Si (6x5 mm)		(1.6/40)/ (1.6/20 = 0.5
20	e.g. PGL6076.131 130 nH max. 60 A, 0.16 mOhm @ 500kHz (7.6x7.6x12 mm)		20x 2 =40	e.g. PGL6076.131 130 nH max. 60 A, 0.16 mOhm @ 410 kHz *possible with 2x 30 A inductors*		40/20 = 2 *40*0.5/ 20 = 1*

1-stage IISB² approach

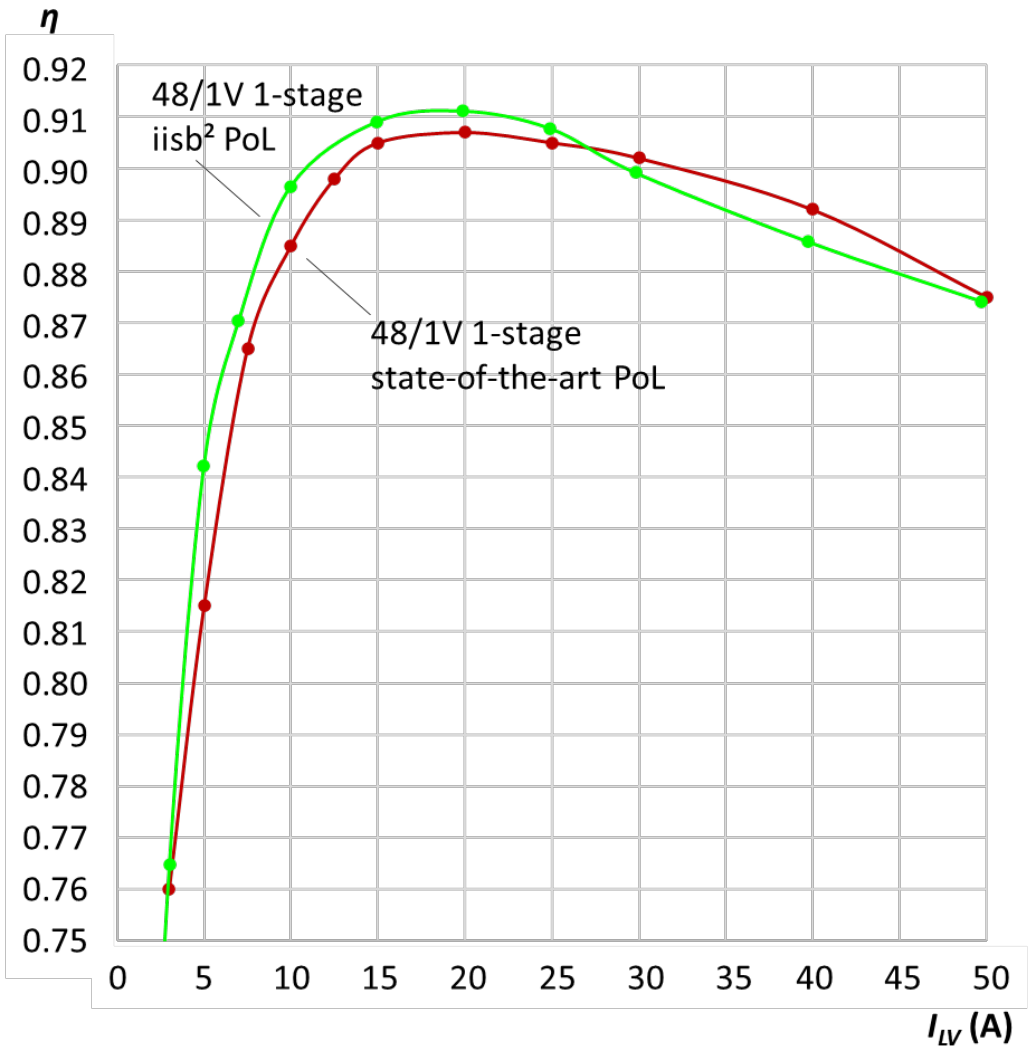
20x 48 V → 1 V





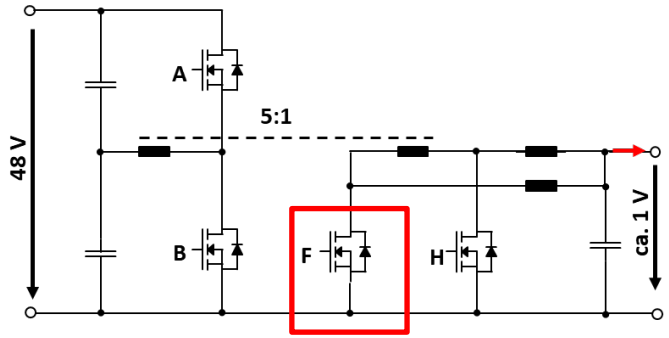


Direct comparison



State-of-the-art 1-stage approach

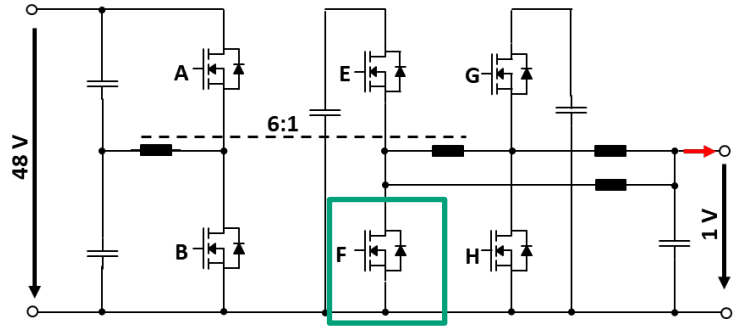
48 V → 1 V



0.65 mOhm GaN

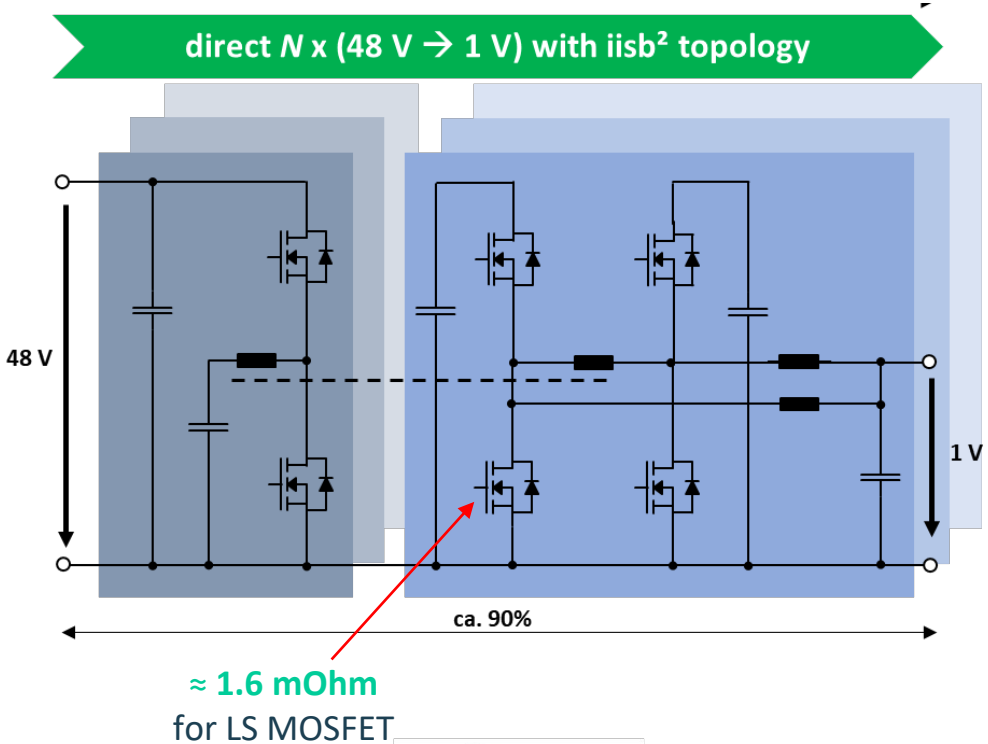
1-stage IISB² approach (integrated, galvanically isolated, separated buck/boost topology)

48 V → 1 V



1.6 mOhm Si

Application example: Point of Load (PoL) DC/DC converter for Server & Memory in data centres



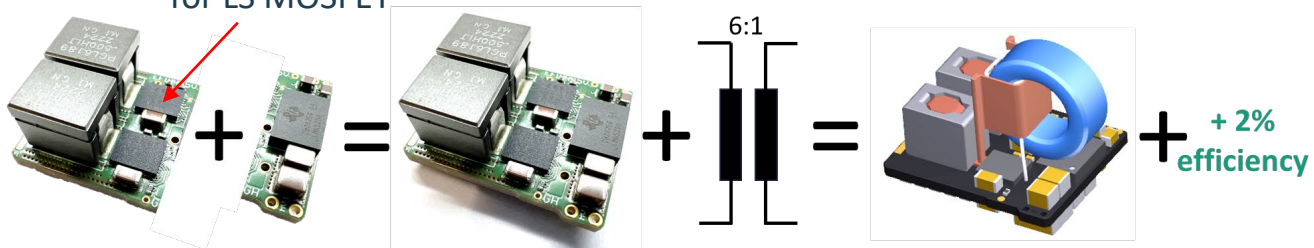
Advantage:
+2% efficiency compared with typ. 2-stage approach (as expected).

But compared with 1-stage state-of-the-art hard-switched half-bridge with current doubler rectifier using 2x 30 V GaN with 1.3 mOhm parallel = **0.65 mOhm**

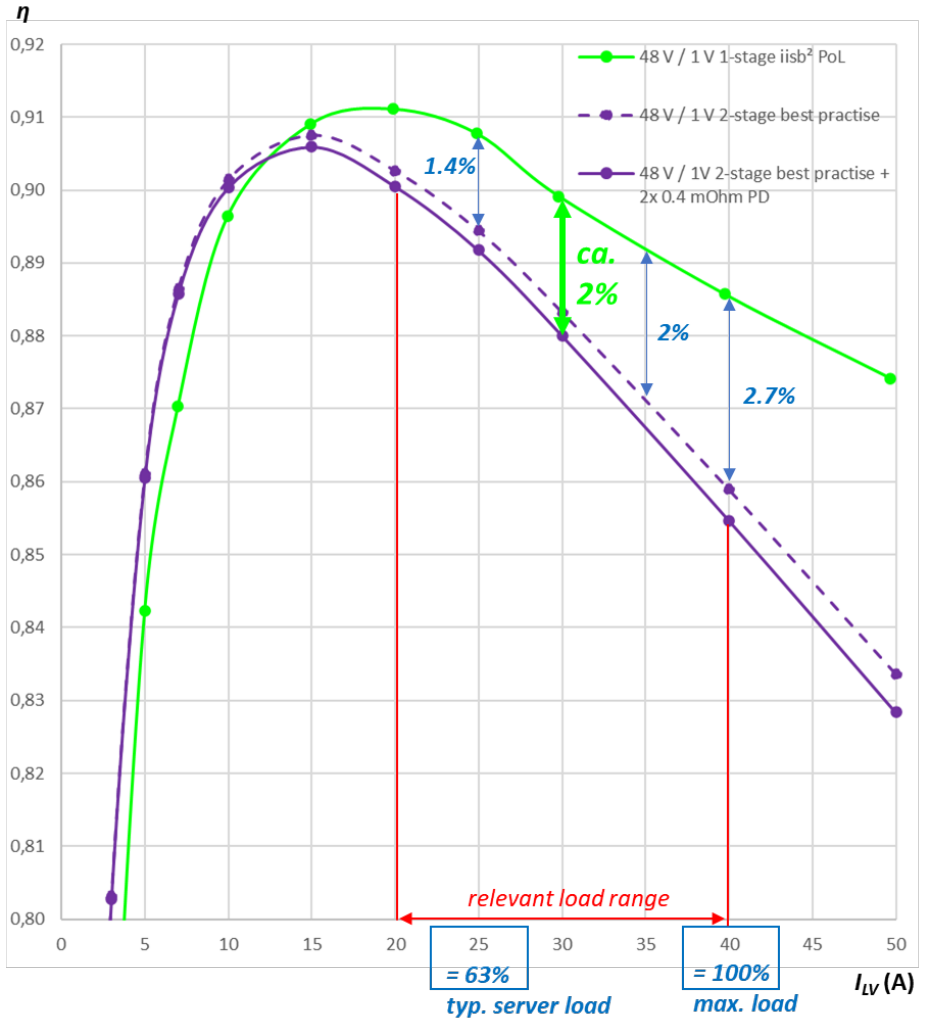
less semiconductor area needed
≈ 50% *)

iisb² topology works with only
≈ 1.6 mOhm for LS MOSFET

*) if same semiconductor technology is used



state-of-the-art PoL units | state-of-the-art half-bridge unit | transformer | **iisb²** circuit topology (**i**ntegrated, galvanically **i**solated, **s**eparated **b**uck/**b**oost topology)



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Thank you for the attention!

I‘m pleased to answer your questions.
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