Mauro Keck*,§, Norman Boettcher*,§, Ruth Domes*, Jonas Lindner*, Hubert Rauh*, Joerg Schulze*,§
*Fraunhofer Institute for Integrated Systems and Device Technology (IISB), Erlangen, Germany
§Friedrich-Alexander University, Chair of Electron Devices (LEB), Erlangen, Germany

TCAD Study on Parallel SiC Two-Pole SSCB Chips Integrated Into a 900 V Power Module

Fraunhofer IISB

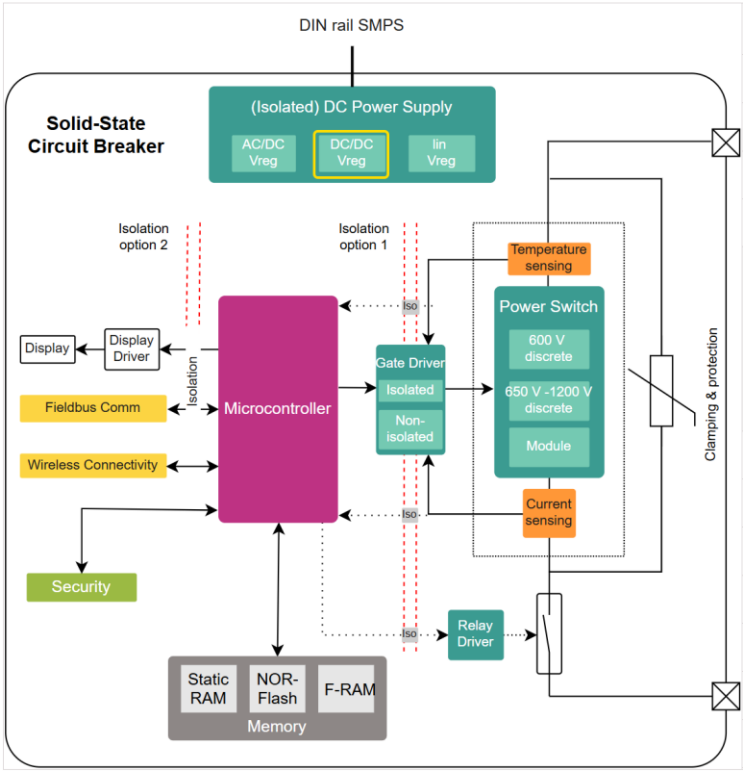
Fraunhofer Institute for Integrated Systems and Device Technology IISB

DC Circuit Breakers Today

You can have simple circuit breaker modules…

https://viox.com/mcb/

…or microsecond protection…

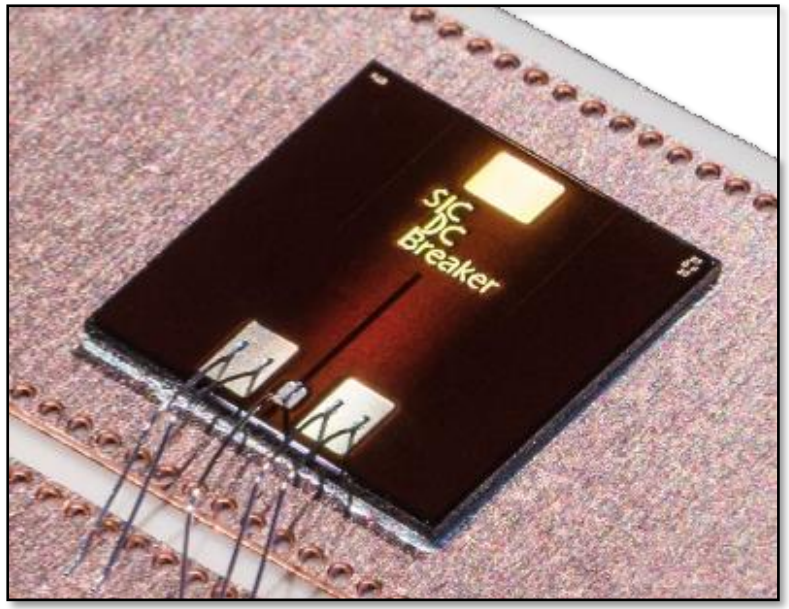


Source: https://www.infineon.com/application/solid-state-circuit-breaker?ftab=02#block-diagram

© Fraunhofer IISB

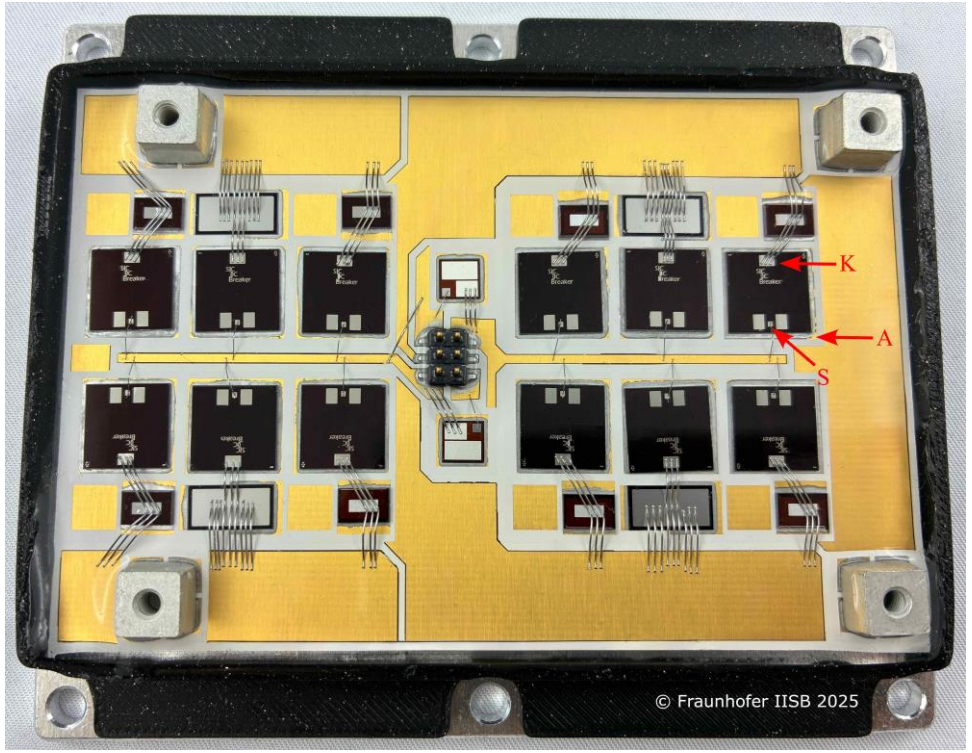
Breaking the Trade-Off: Nanosecond Protection in a Simple DC Circuit Breaker Power Module

We aim for both.



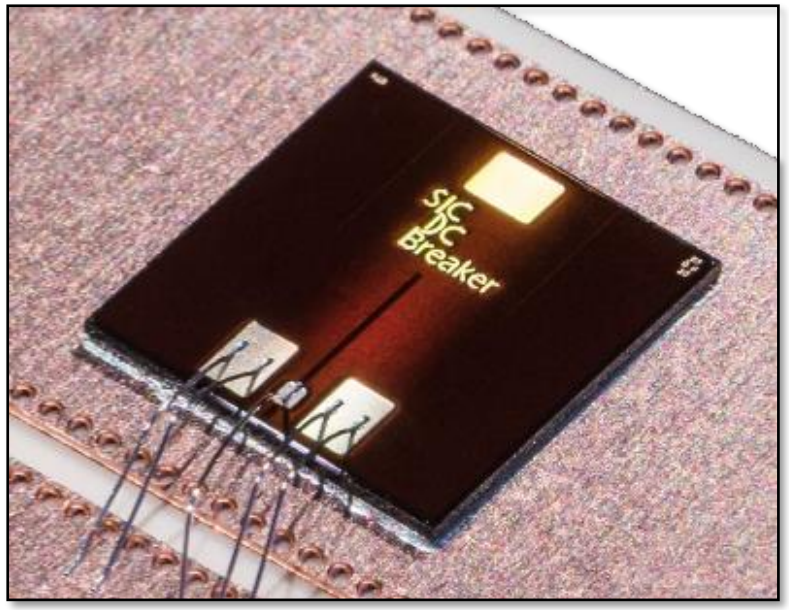
- Monolithically integrated **2-pole SiC SSCB**
- **Measured clearance time of ~120 ns**

Bidirectional 900 V 120 A Power Module

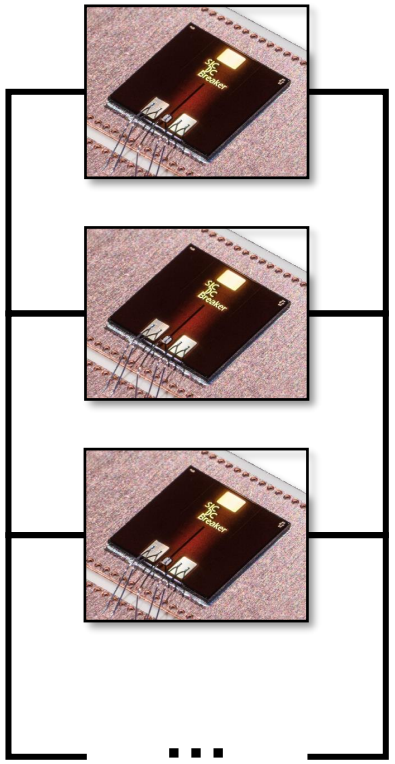


© Fraunhofer IISB

Breaking the Trade-Off: Nanosecond Protection in a Simple DC Circuit Breaker Power Module



1. How does the DC-Breaker Chip work?

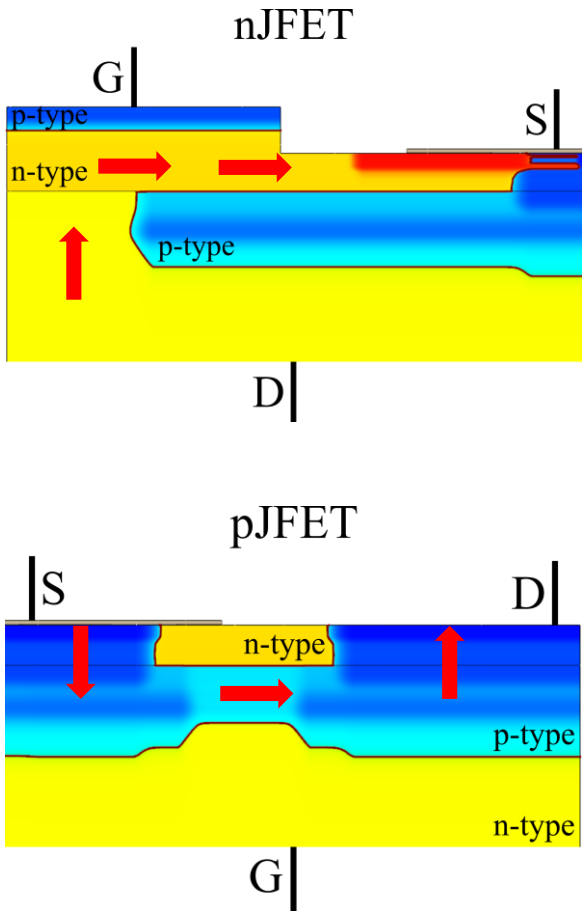


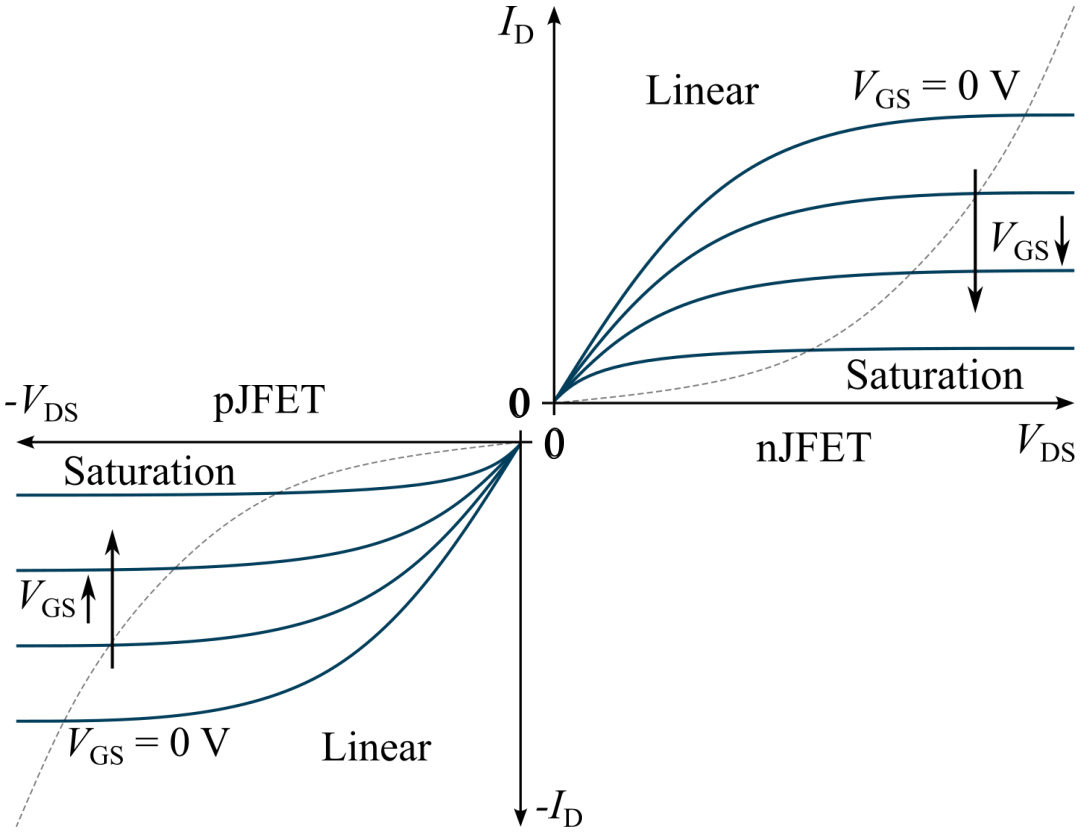
2. TCAD Simulation: How do they perform in parallel?

© Fraunhofer IISB

The “Inverse Thyristor” (iT) Topology

SiC JFETs

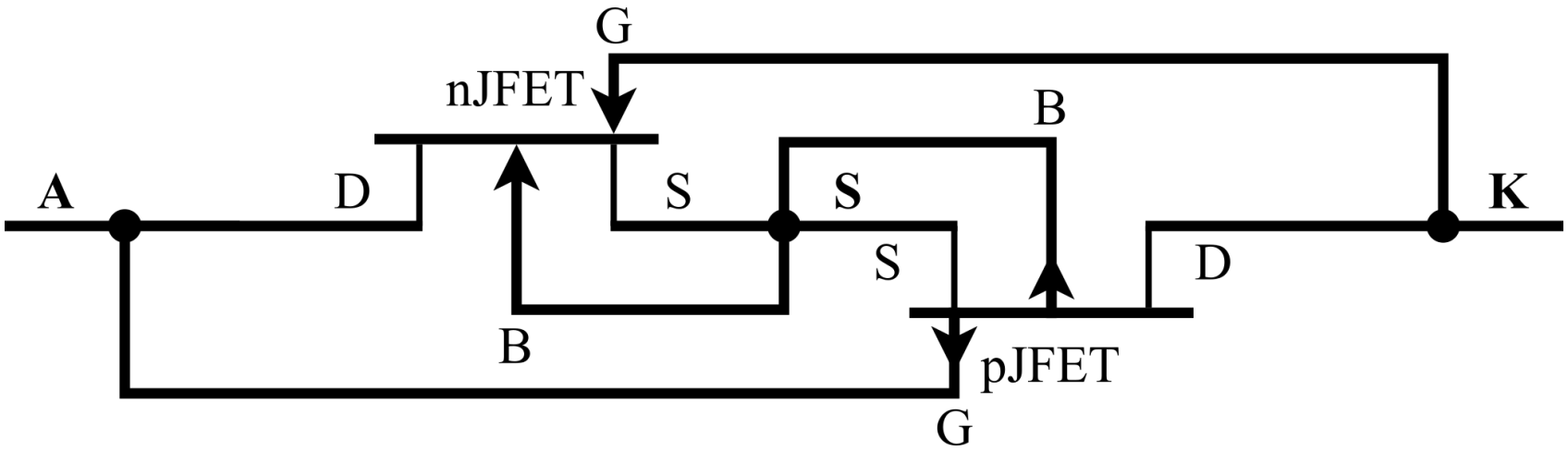




© Fraunhofer IISB

The “Inverse Thyristor” (iT) Topology

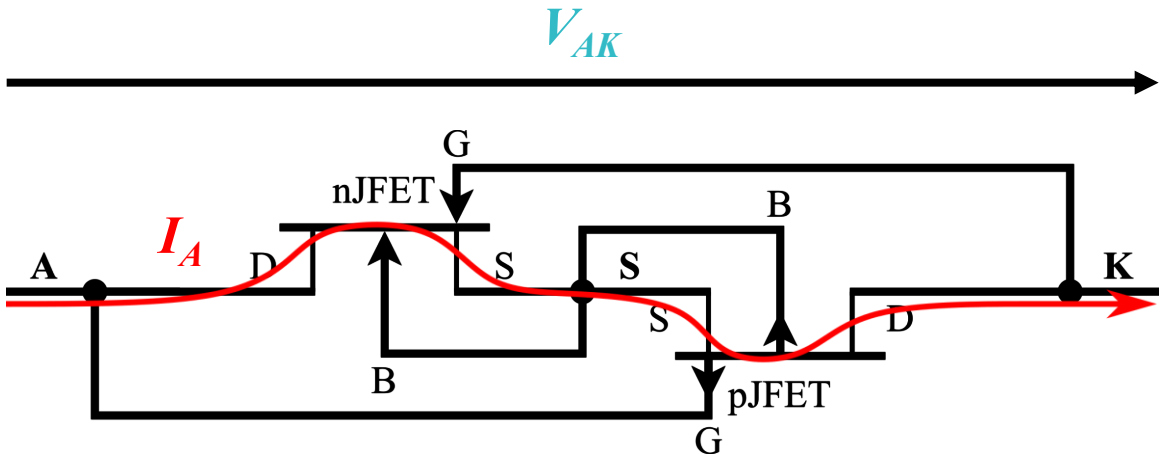
SiC JFETs in Antiseries

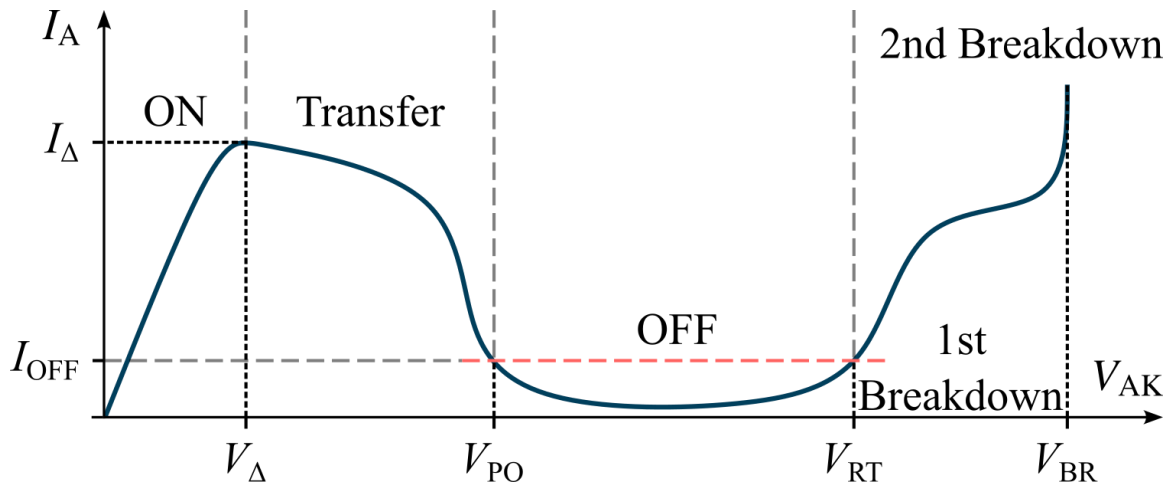


© Fraunhofer IISB

The “Inverse Thyristor” (iT) Topology

SiC JFETs in Antiseries

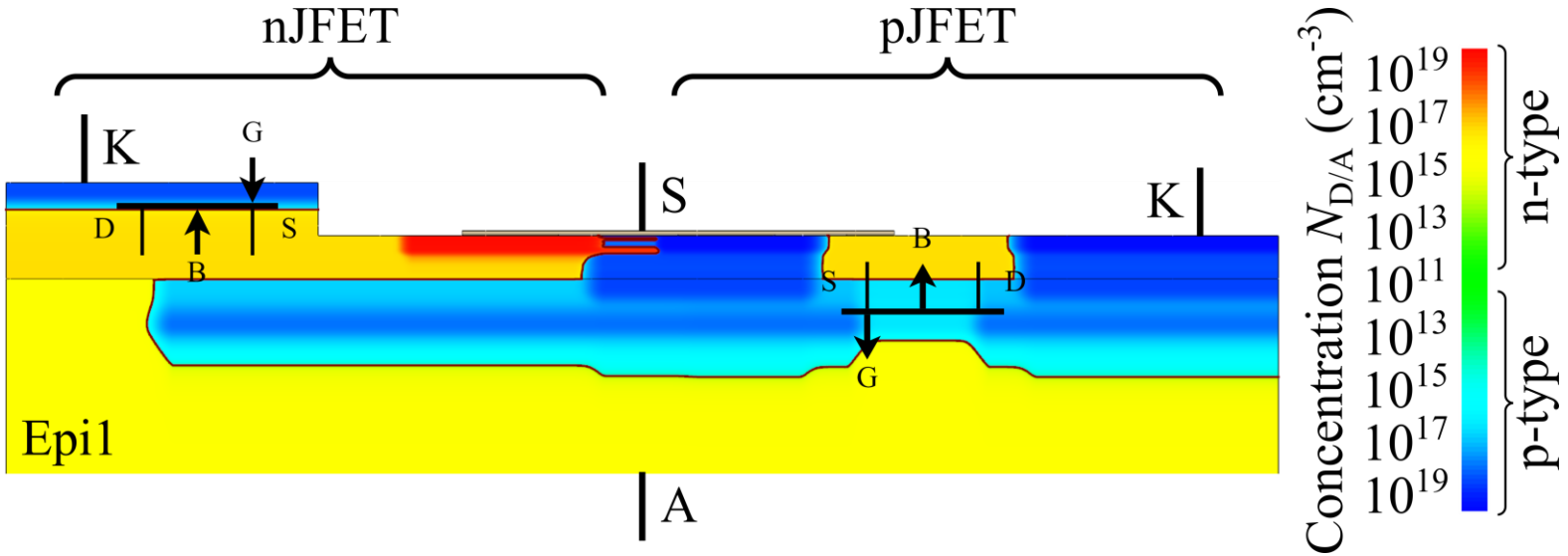


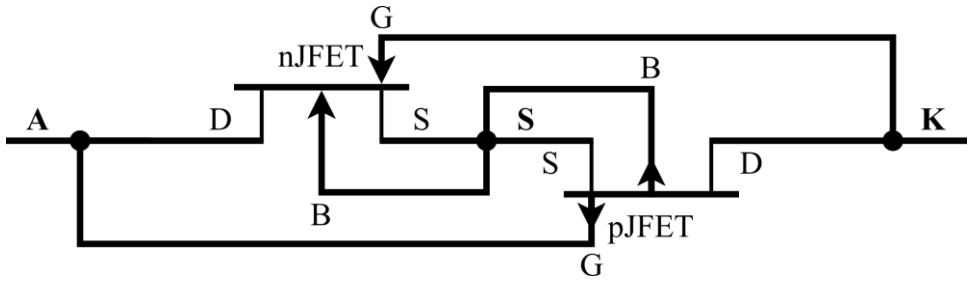


© Fraunhofer IISB

Monolithic Integration of the “Inverse Thyristor” – SiC DC-Breaker

From SiC JFETs to integrated SiC Circuit Breaker



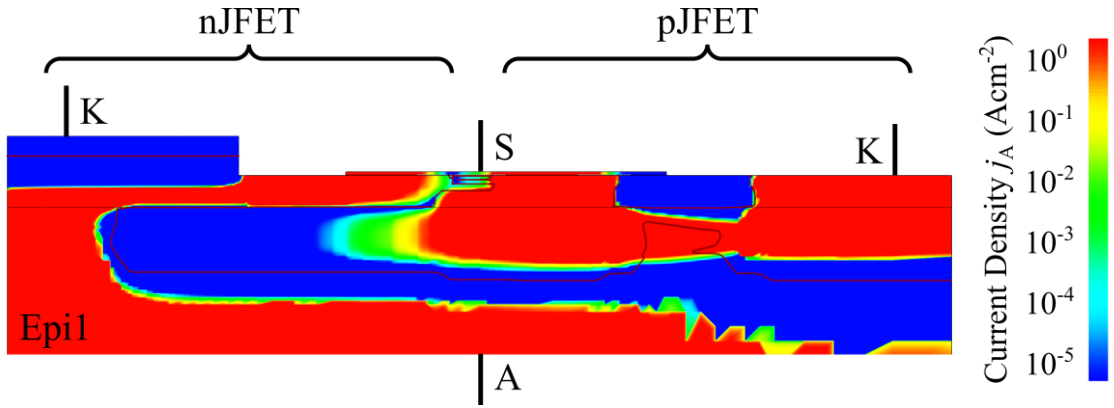


Phyiscal TCAD Model

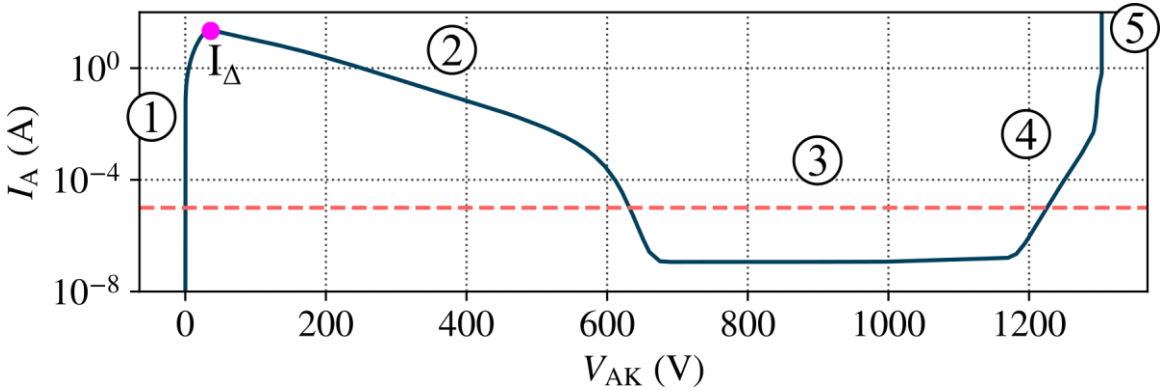
© Fraunhofer IISB

Monolithic Integration of the “Inverse Thyristor” – SiC DC-Breaker

From SiC JFETs to integrated SiC Circuit Breaker



Phyiscal TCAD Model

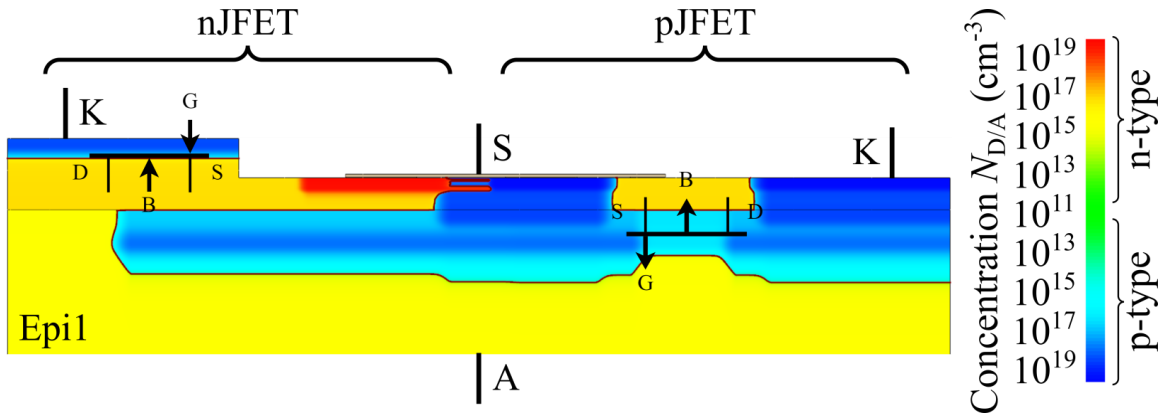


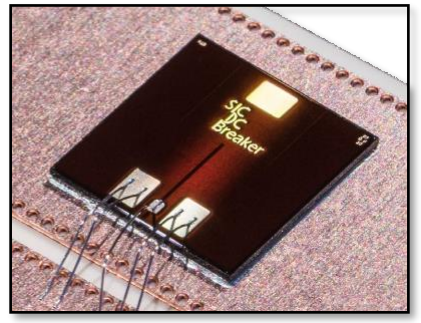
Simulated quasistationary IV-Characteristics

© Fraunhofer IISB

Monolithic Integration of the “Inverse Thyristor” – SiC DC-Breaker

From SiC JFETs to integrated SiC Circuit Breaker

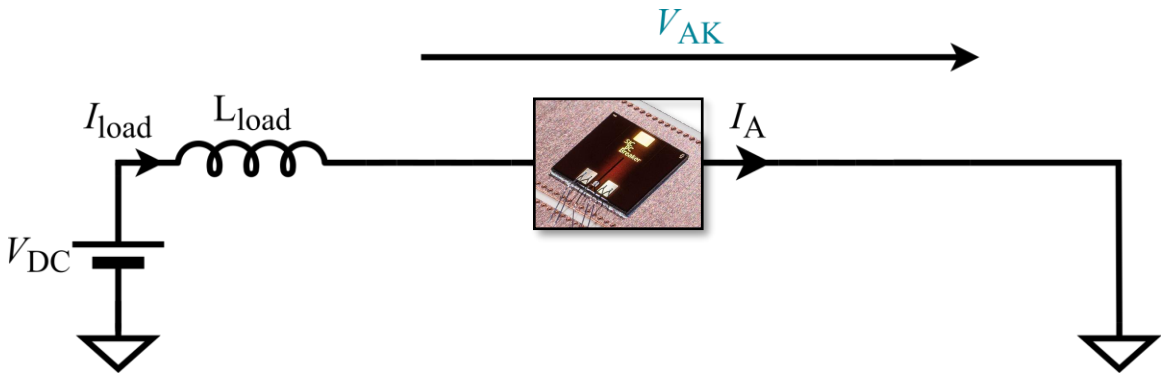


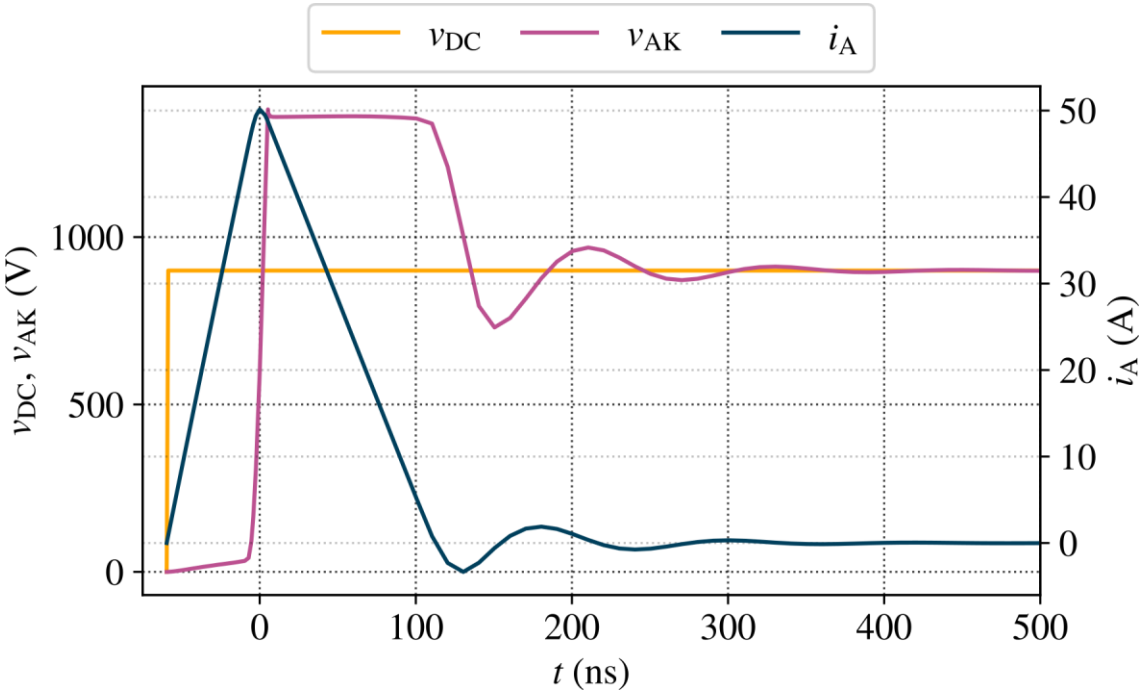


© Fraunhofer IISB

Unclamped Inductive Switching – One DC-Breaker Chip

Anode Current I_A and Anode-Cathode Voltage V_{AK} Over Time During Failure Current Scenario



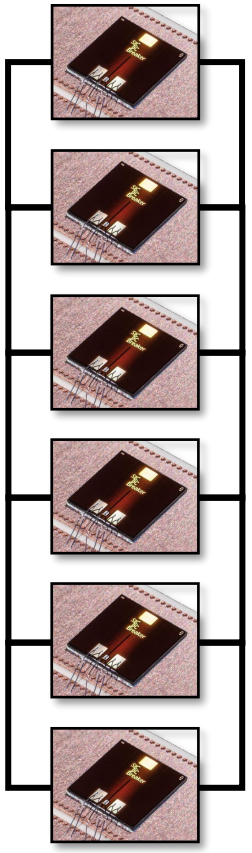


$\mathbf{L_{load} = 1\ \mu H}$

© Fraunhofer IISB

Six Parallel DC-Breaker (iT) Chips

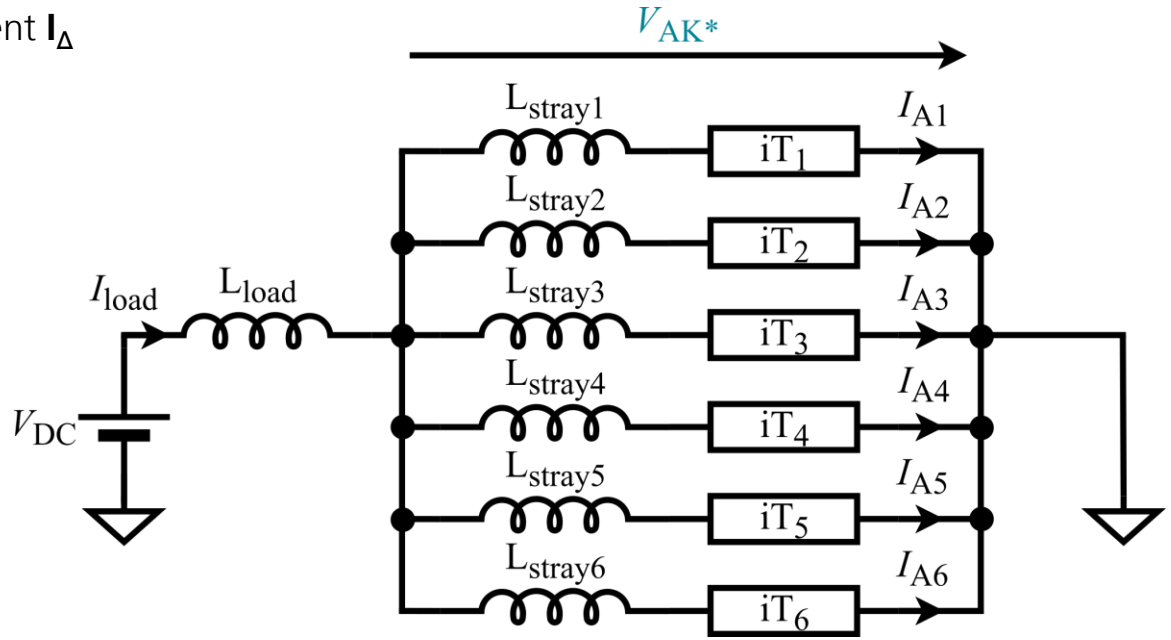
Lumped Element Model



Goal: 900 V 120 A Power Module

- → Six **900 V** Chips with **25 A** Trigger Current $\mathbf{I_\Delta}$
- → Module with $\mathbf{I_\Delta = 150\ A}$

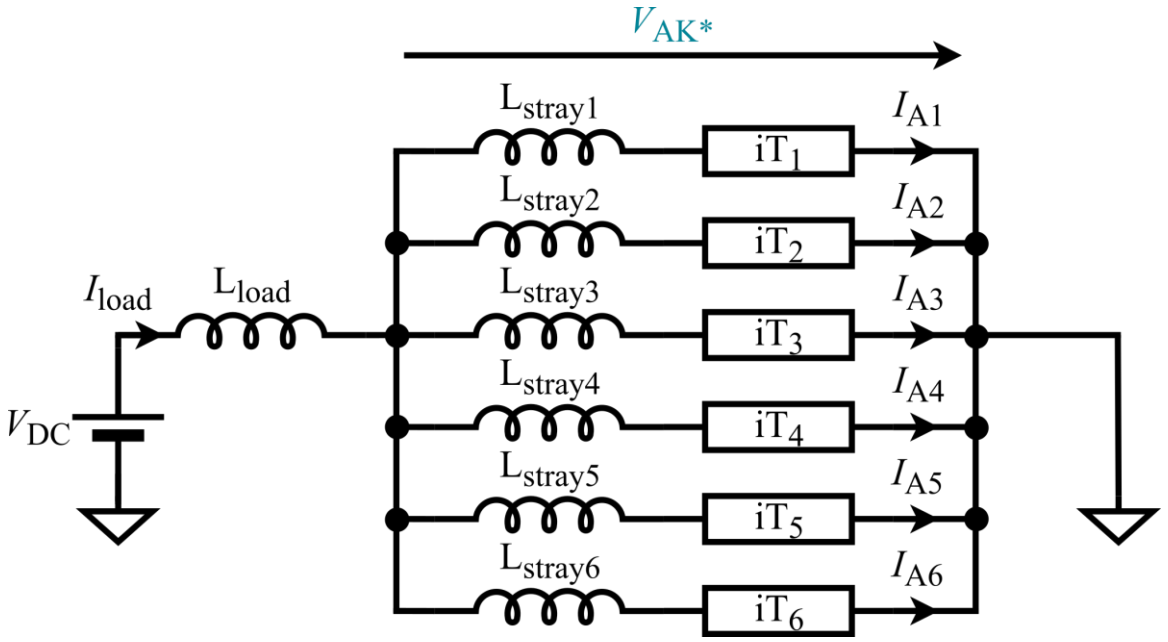
Electro-thermal mixed-mode simulations in TCAD



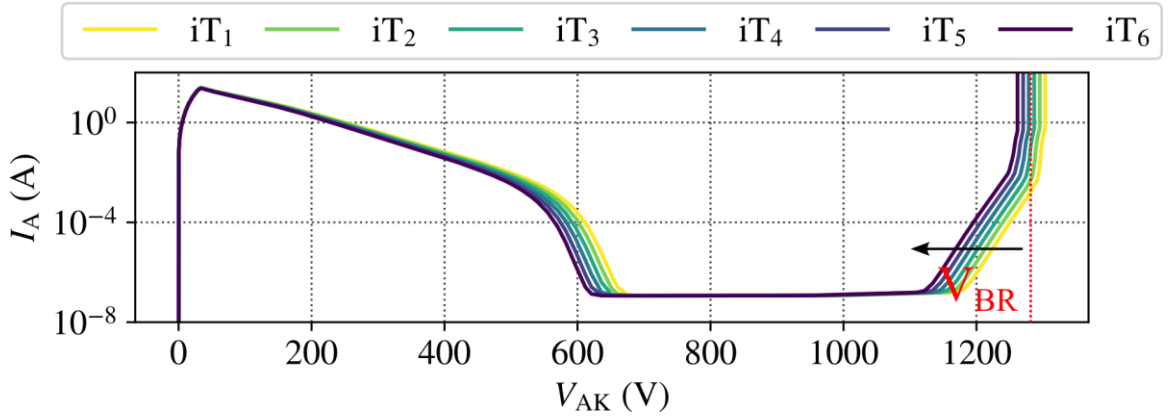
© Fraunhofer IISB

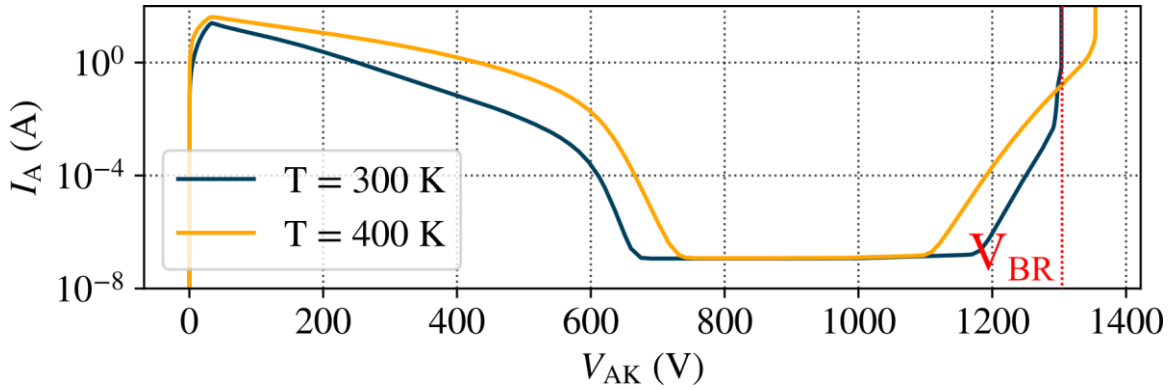
Six Parallel DC-Breaker Chips

Six Chips with Different Avalanche Breakdown Voltages V_{BR}



$L_{stray1} = L_{stray4} \approx 3.23$ nH
$L_{stray2} = L_{stray5} \approx 3.56$ nH
$L_{stray3} = L_{stray6} \approx 3.91$ nH

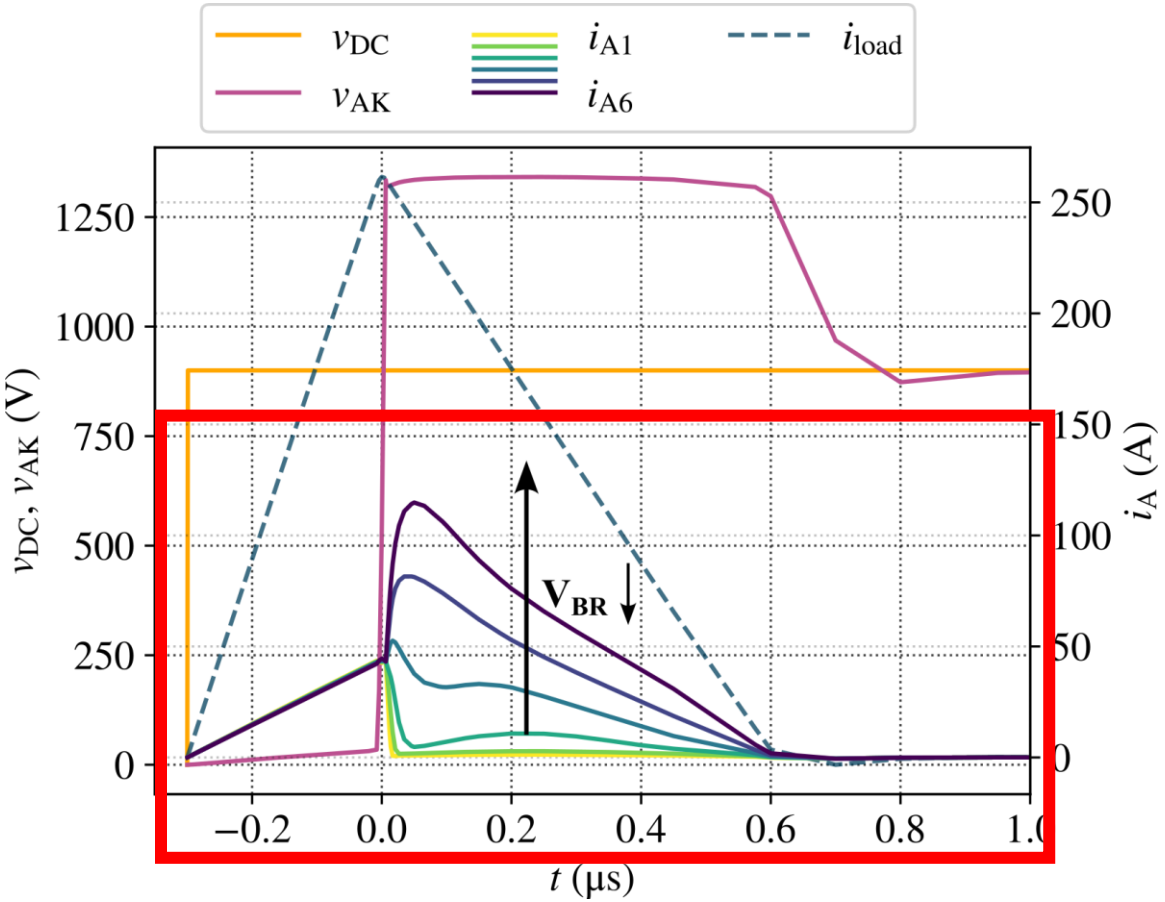




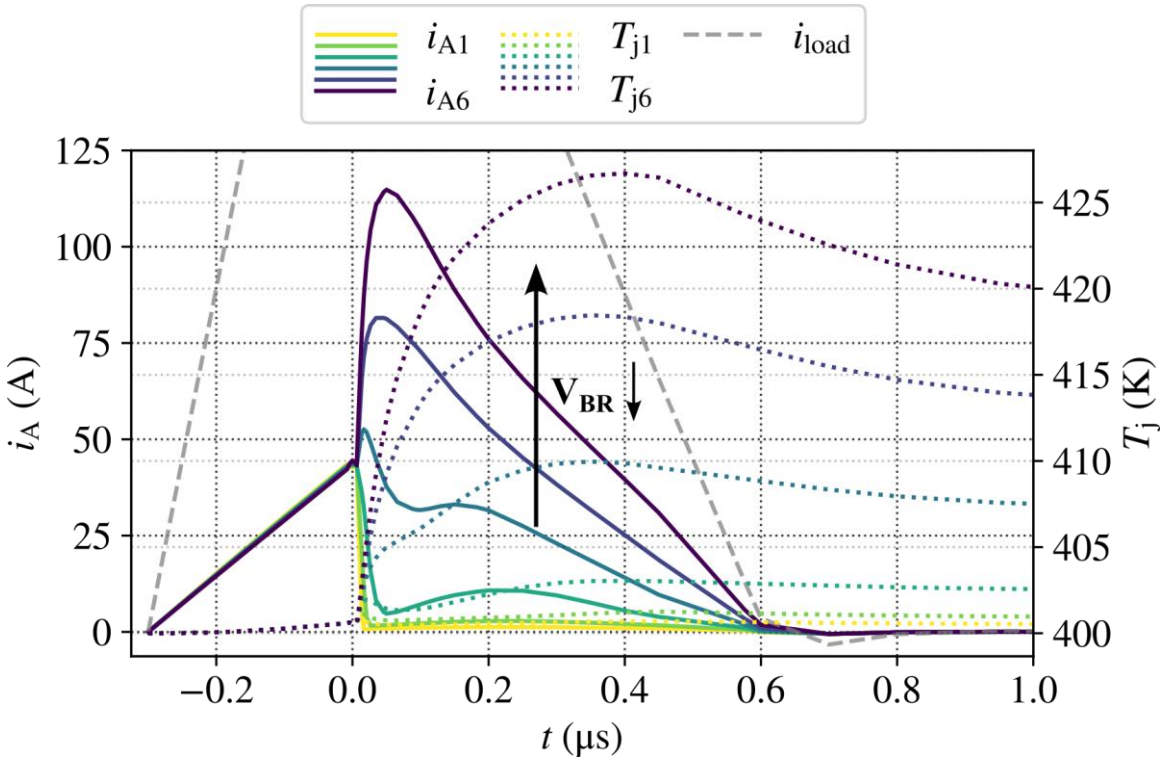
© Fraunhofer IISB
Public

Unclamped Inductive Switching – Six Parallel DC-Breaker Chips

I_A,V_{AK} and Junction Temperatures T_J Over Time During Failure Current Scenario



$L_{load} = 1\ \mu H$

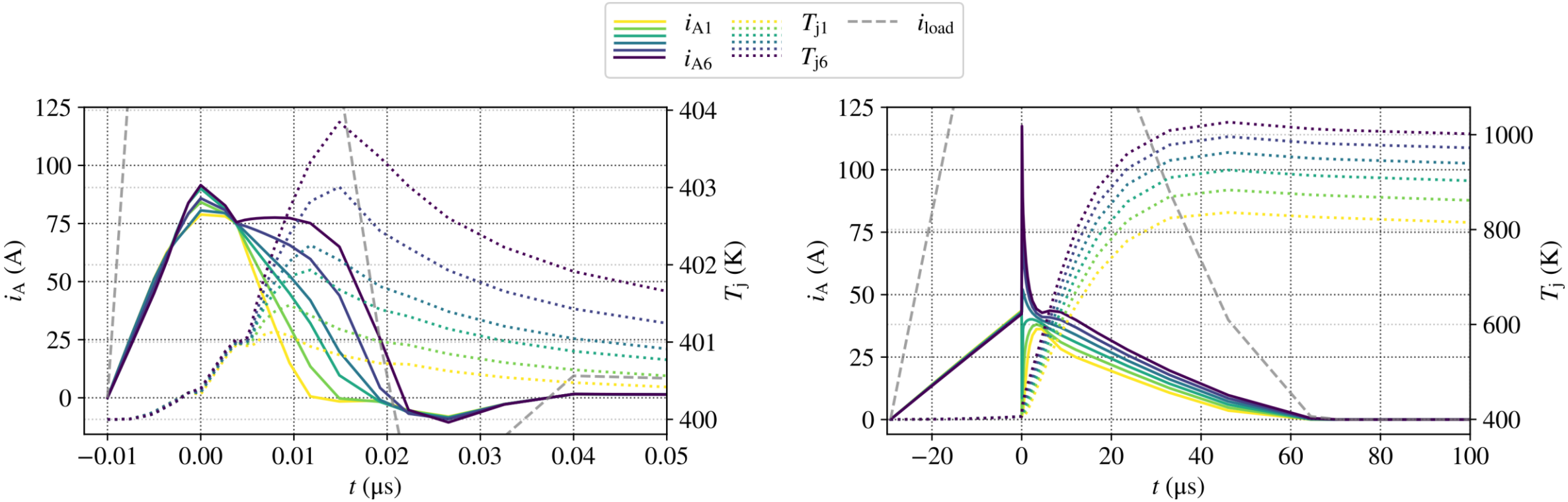


$L_{load} = 1\ \mu H$

© Fraunhofer IISB Public

Unclamped Inductive Switching – Six Parallel DC-Breaker Chips

Variation of Load Inductances L_{load}



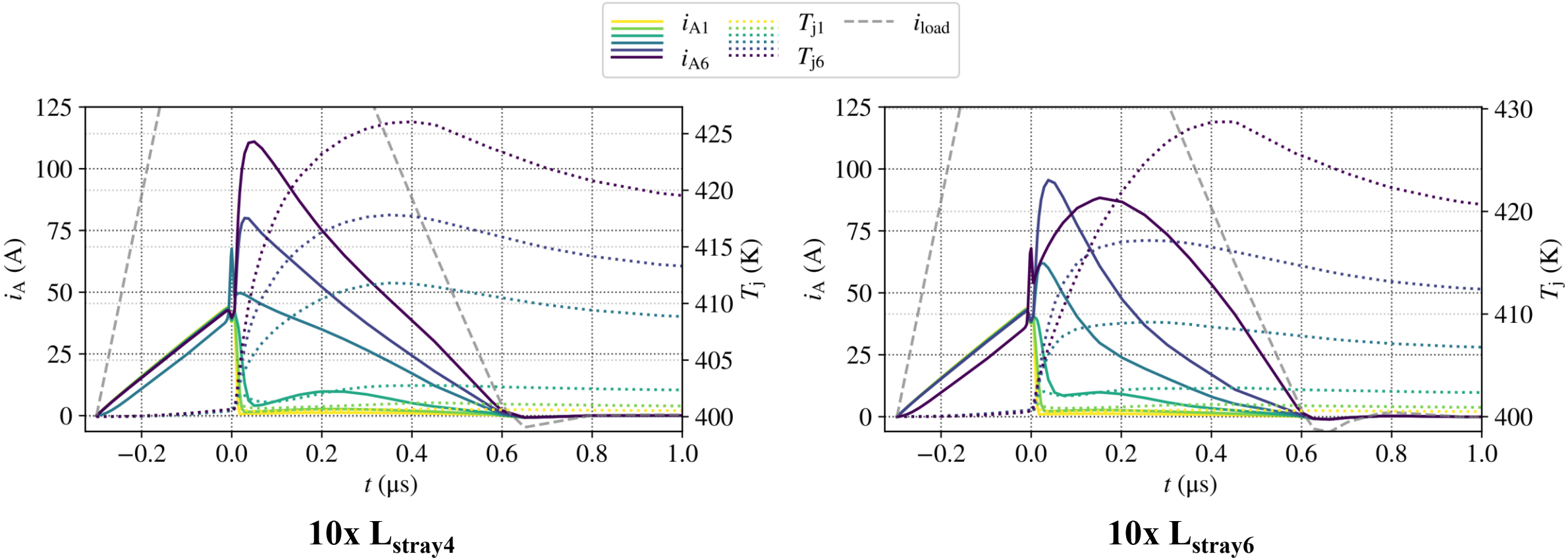
$\mathbf{L_{load} = 10\ nH}$

$\mathbf{L_{load} = 100\ \mu H}$

© Fraunhofer IISB Public

Unclamped Inductive Switching – Six Parallel DC-Breaker Chips

Variation of Stray Inductances L_{stray}



10x L_{stray4}

10x L_{stray6}

© Fraunhofer IISB

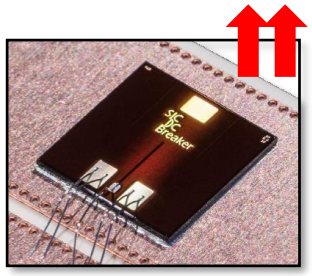
Discussion of Simulation Results

Further Development and Analysis Should Enable new Kinds of Power Modules

Current module design needs FWDs for loads > 1 µH

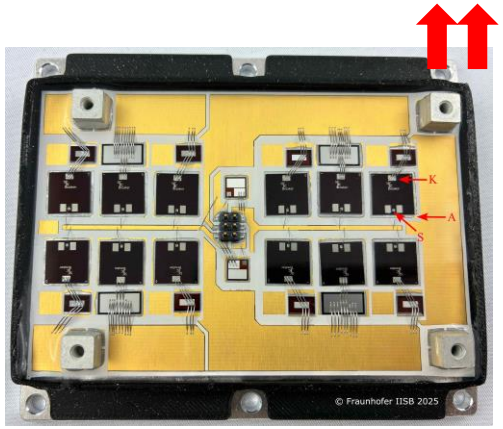
Stray inductance tuning can reduce current peaks

Stray inductance tuning does not affect current sharing



Device Level

New chips with reduced $R_{DS(ON)}$



Module Level

Module design taking into account V_{BR} variations

Module Level

More chips in parallel

→ **Further measurements and analysis needed**
→ **After optimizations: Simple and fast SSCB modules should be feasible**

© Fraunhofer IISB

Fraunhofer
IISB

Fraunhofer Institute for Integrated
Systems and Device Technology IISB

Thank you for your attention!