

Plasma-Enhanced Atomic Layer Etching of AlGa_N/Ga_N: Process Optimization, Stability Analysis, & Recess Etching Of Gate Structures

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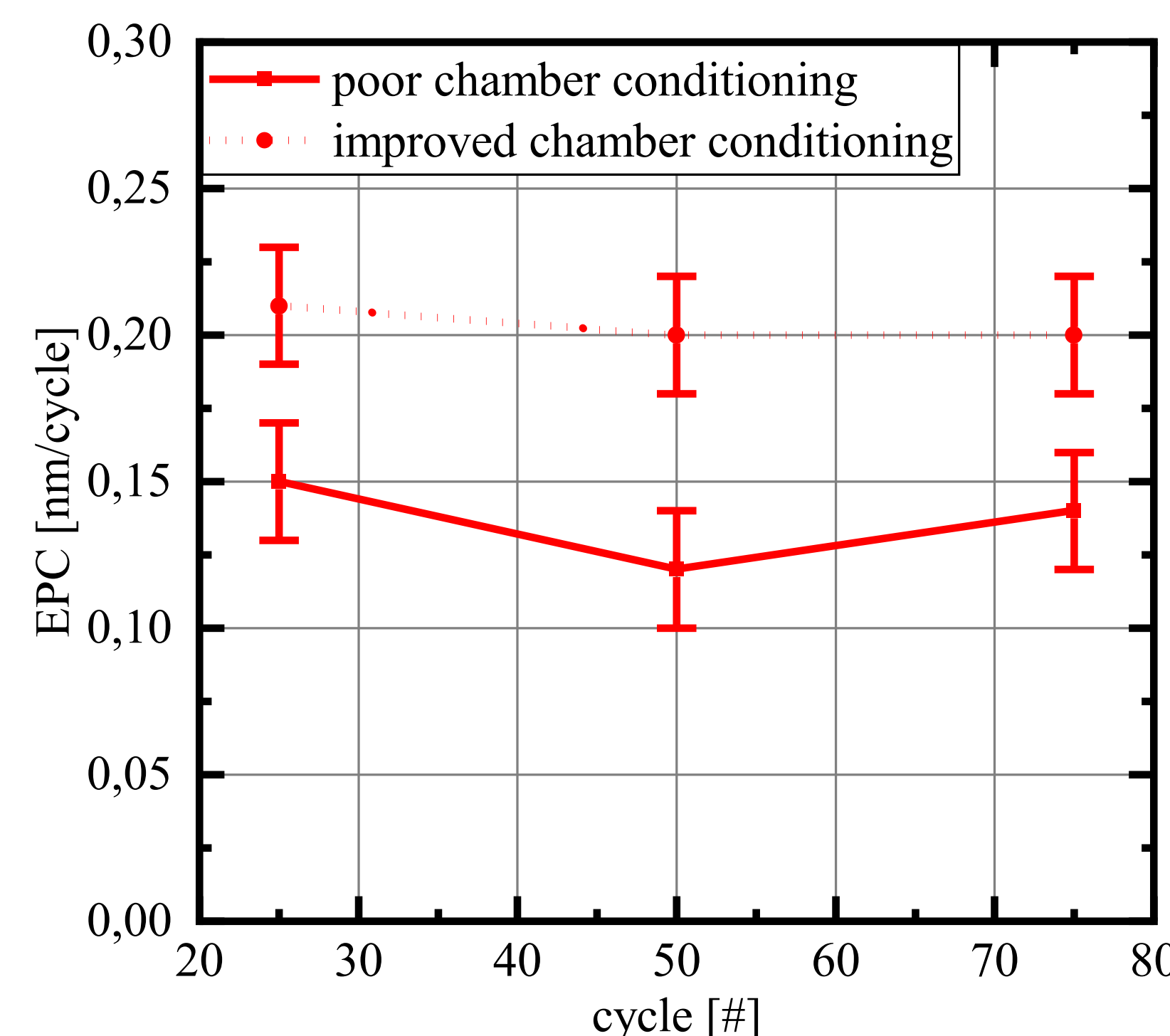
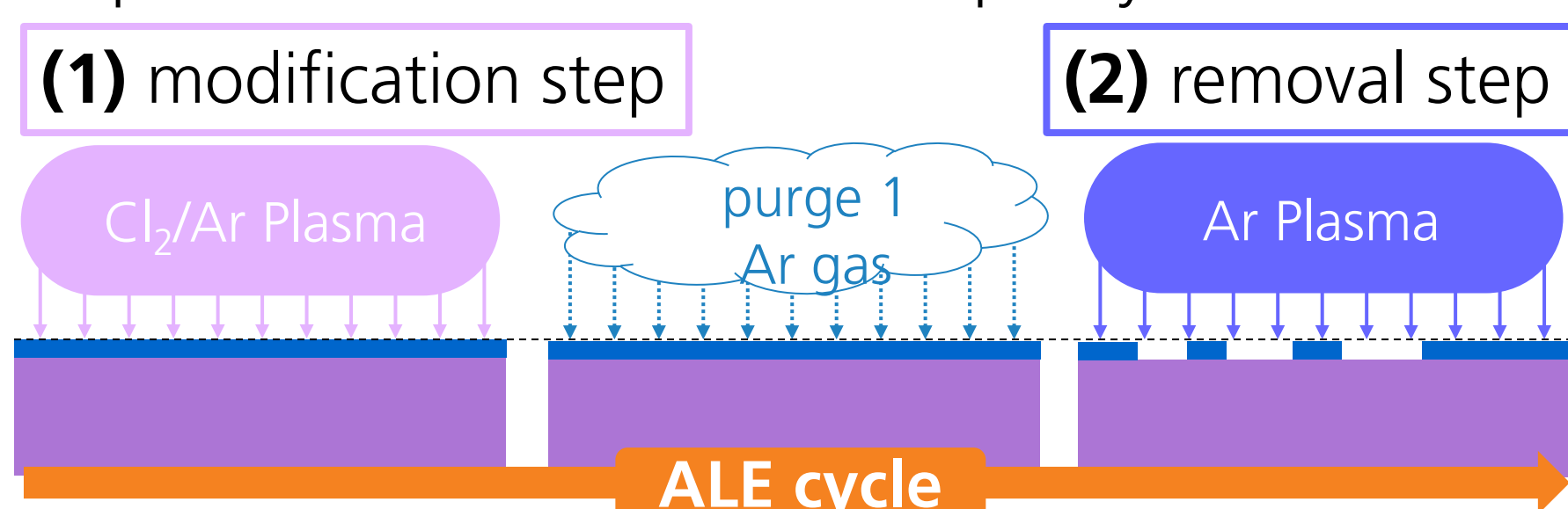
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Introduction

- advanced AlGa_N/Ga_N devices require highly precise, low-damage etching technologies
- plasma-enhanced ALE offers atomic-scale control of etch depth and surface quality
- process principle: Cl₂ plasma surface modification step **(1)** + low-energy Ar ion removal step **(2)**
- self-limiting reactions enable high precision and reproducibility
- purge steps improve selectivity but increase processing time and cost
- **goal:** increase ALE efficiency while maintaining process control and surface quality

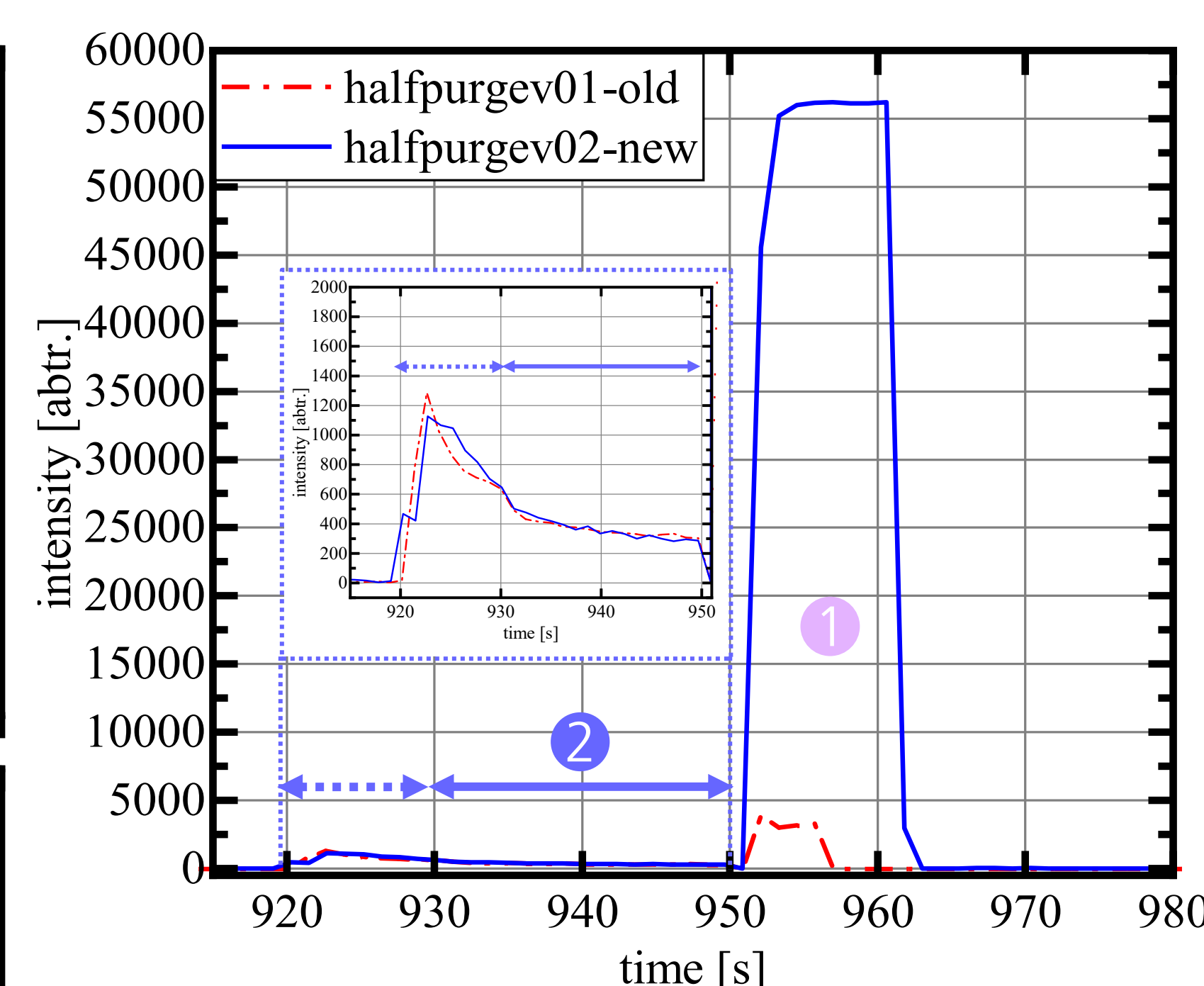
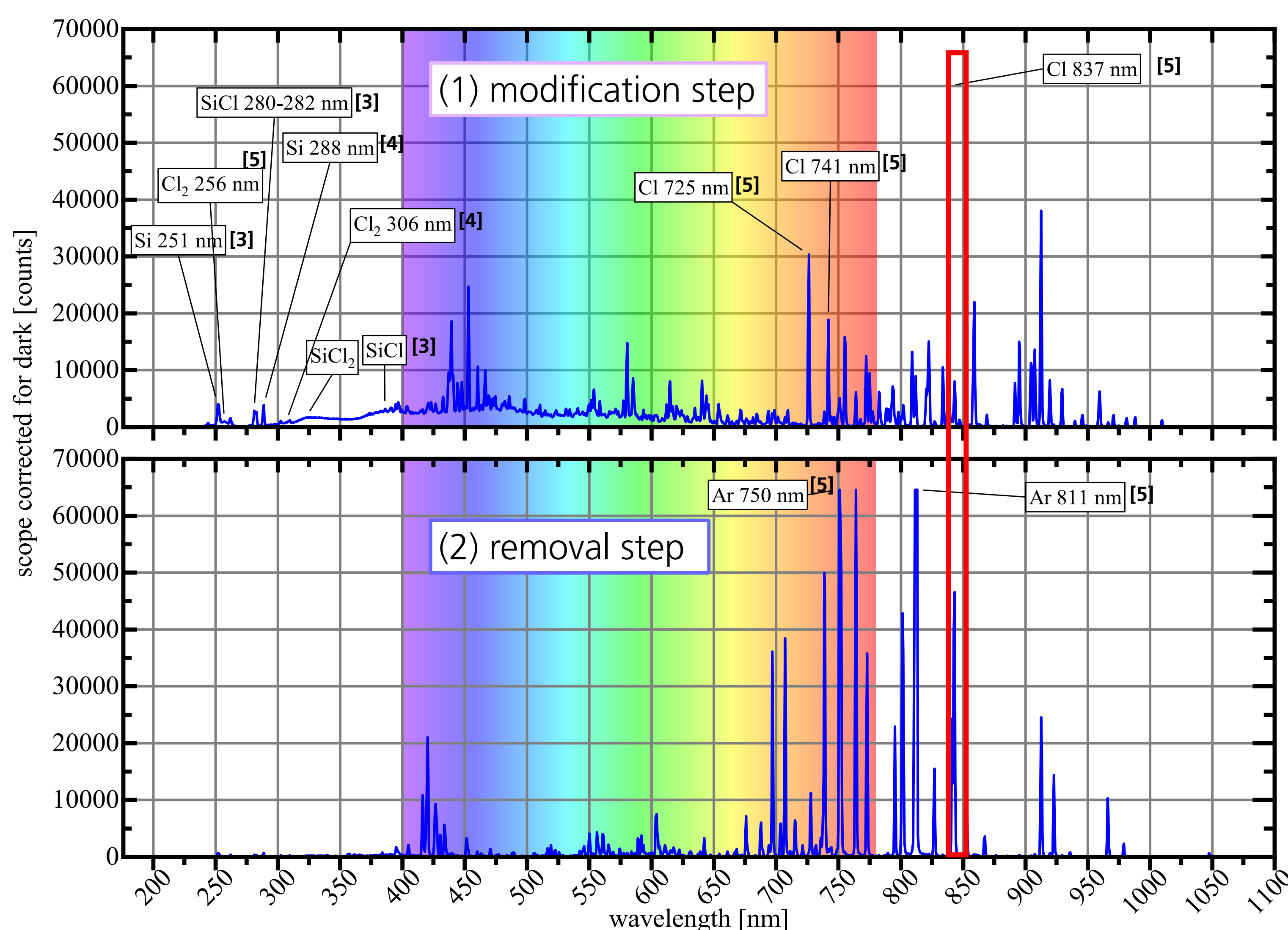


- EPC after poor chamber conditioning recipe → **0.11 nm/cycle**
- EPC after improved chamber conditioning and recipe → **0.25 nm/cycle**
- chlorine residues desorbing from chamber wall during removal step **(2)**

Chamber cleaning procedure / monitoring

- primary cleaning with sapphire carrier wafer:
 1. SF₆/Cl₂ plasma → Ga-, Al-, SiOCl compounds
 2. SF₆/O₂ plasma → SiCl_x-, SiOCl compounds
 3. O₂/Ar plasma → carbon residues
- H₂ etching effects chamber condition:
 - H₂ plasma reduces AlCl_x and GaCl_x on wall
 - drastic drop in the EPC
- consistent initial condition by implementing hydrogen as 4. step in cleaning procedure
- time-resolved monitoring of specific emission lines → optimization & control of ALE process, chamber cleaning and conditioning
- increasing Cl radical concentration → more effective surface chlorine saturation

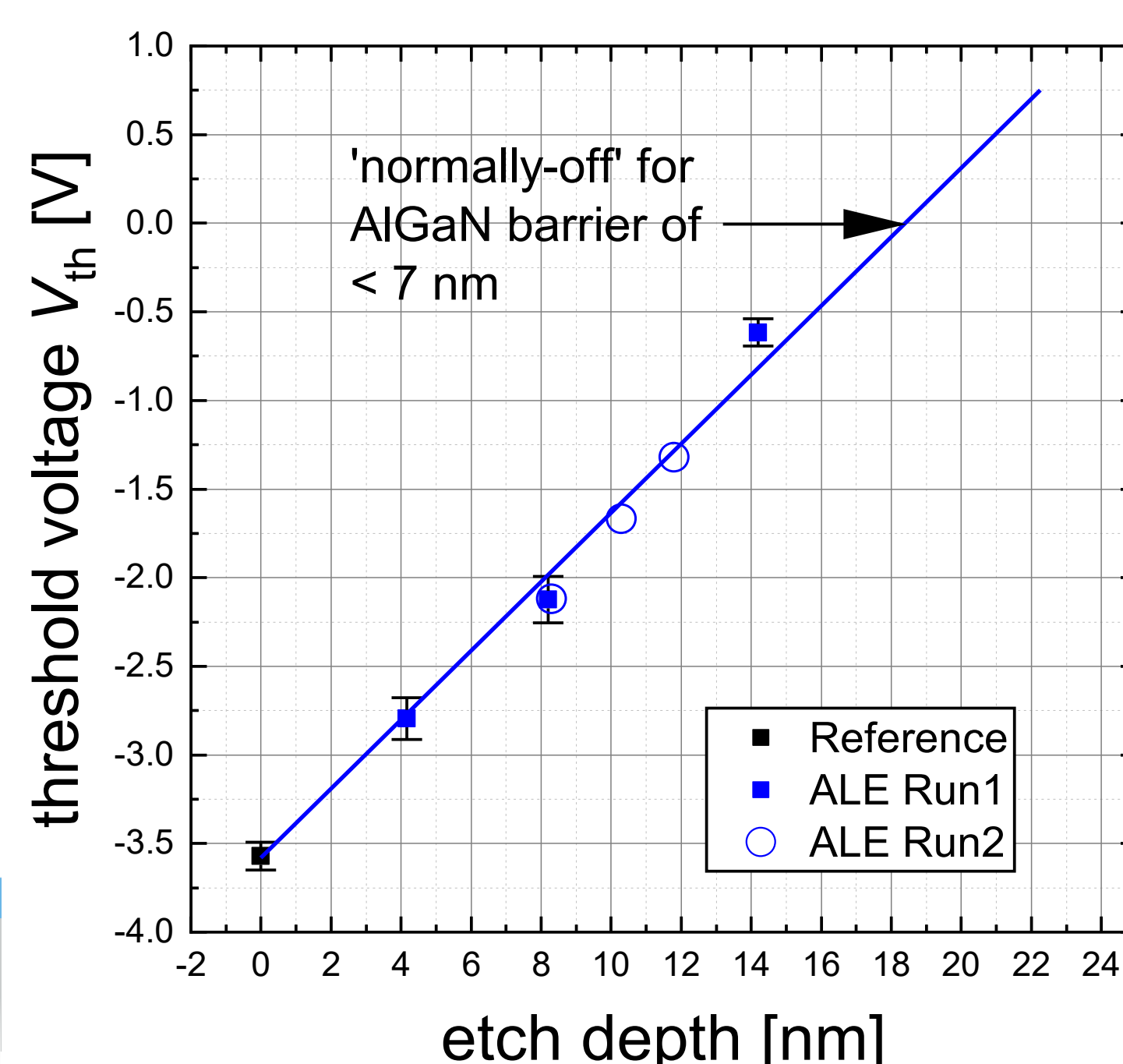
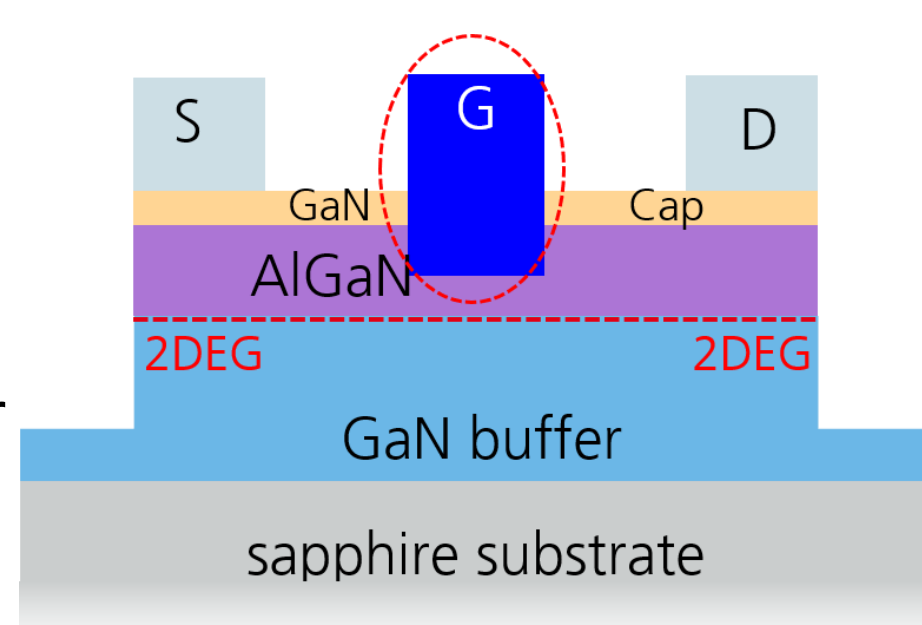
Inline process monitoring using OES



- optical emission spectra during modification **(1)** and removal **(2)** step
- Cl radical (725 nm, 741 nm, **837 nm**) associated with chemical modification **(1)**
- additional emission lines: AlCl from chamber wall reaction, SiCl_x from silicon-carrier
- Ar ion lines (750 nm, 811 nm) characteristic of the removal step **(2)**
- chlorine residues during the Ar removal step **(2)** → decrease in self-limitation → longer Ar times increases parasitic etching
- factors for minimizing parasitic etching:
 - conditioning
 - Cl₂/Ar ratio
 - flow rates
 - pressure
 - ICP power
 - modification and removal time

Gate recess etching

- HEMT processing including ALE gate recess with different etch depths
- linear shift of threshold voltage with increasing etch depth → decreasing AlGa_N barrier thickness
- e-mode HEMT (normally-off) at <7 nm AlGa_N barrier thickness
- reproducible over different process runs



Summary

- mixed etch chemistries shift chamber conditions
- frequent cleaning and conditioning restore a reproducible baseline
- in-line OES enables monitoring and optimization of ALE, cleaning, and conditioning
- optimized Cl-radical concentration improves surface saturation, increasing EPC to 0.25 nm/cycle
- with improved conditioning, a reproducible linear threshold-voltage shift can be observed as gate-recess etch depth increases

References:

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