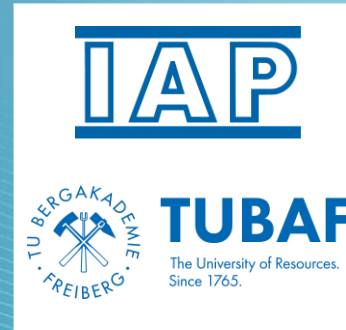




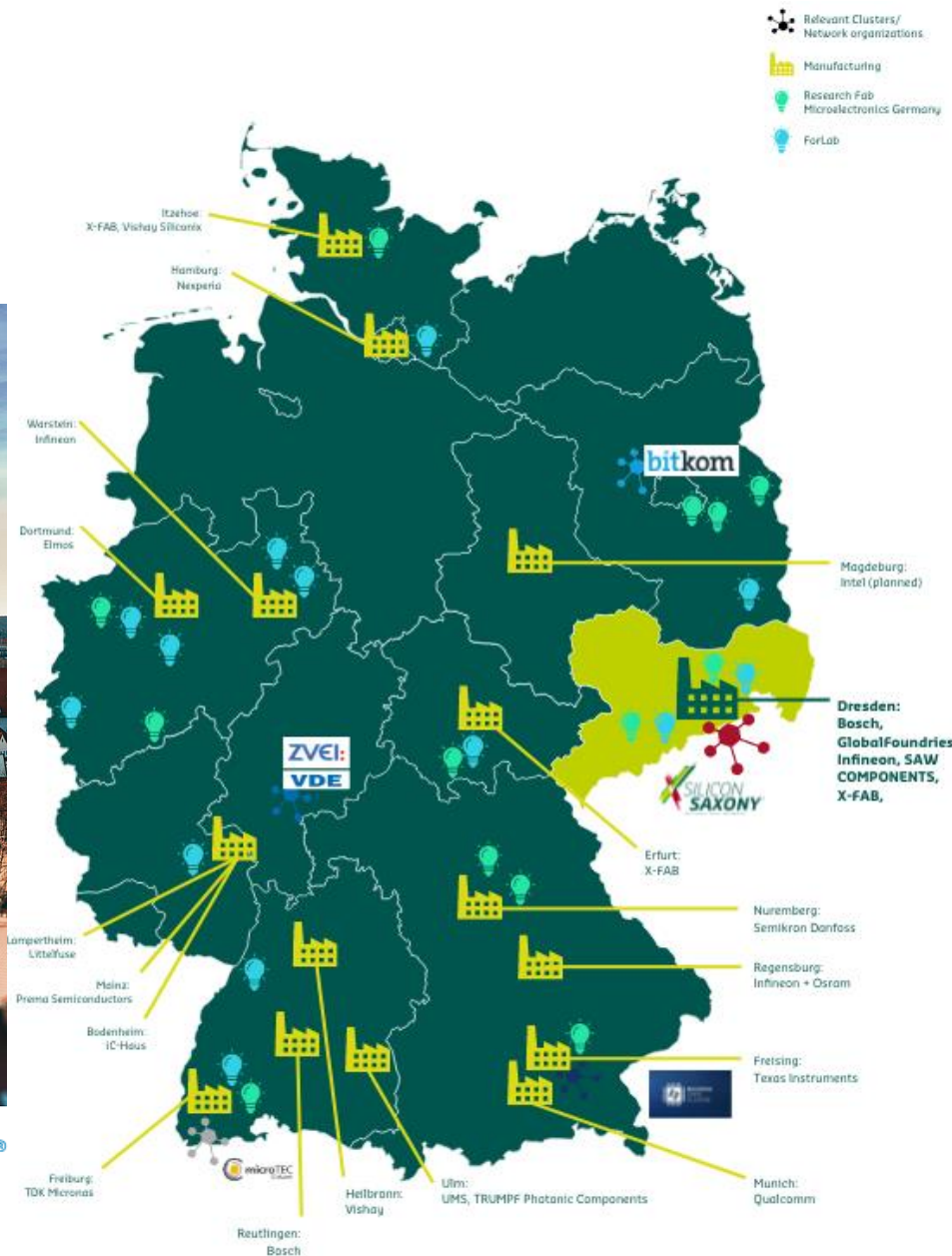
Plasma enhanced Atomic Layer Etching on Nitrides and SiC for high power and photonic application

Franziska C. Beyer, Christian Miersch, Sarah Seidel, Martin Siebert, Gregor Praedel and Johannes Heitmann
GADEST 2026, Venice

Freiberg



www.silberstadt.de
www.silicon-saxony.de

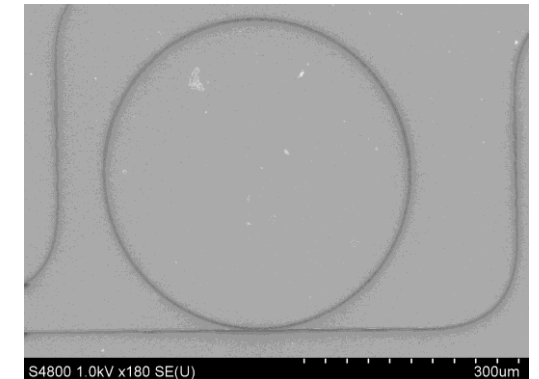
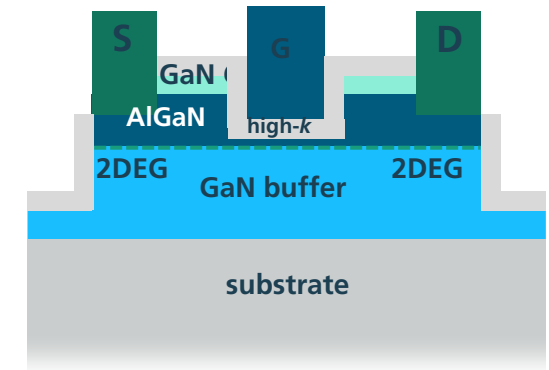


Outline

Atomic Layer Etching on Nitrides and SiC for high power and photonic application

Nitrides

- Development of process modules for enhancement-mode (e-mode) HEMT fabrication
 - Implementation of an ALE process using in situ monitoring (preconditioning and chamber cleaning)
 - Optimization of the ALE process for improved time efficiency (ALE window and different operating modes)
 - Source/drain and gate recess etching to achieve e-mode HEMT operation
 - Extension to Al-rich AlGaN and AlN layers, as well as block-copolymer patterning



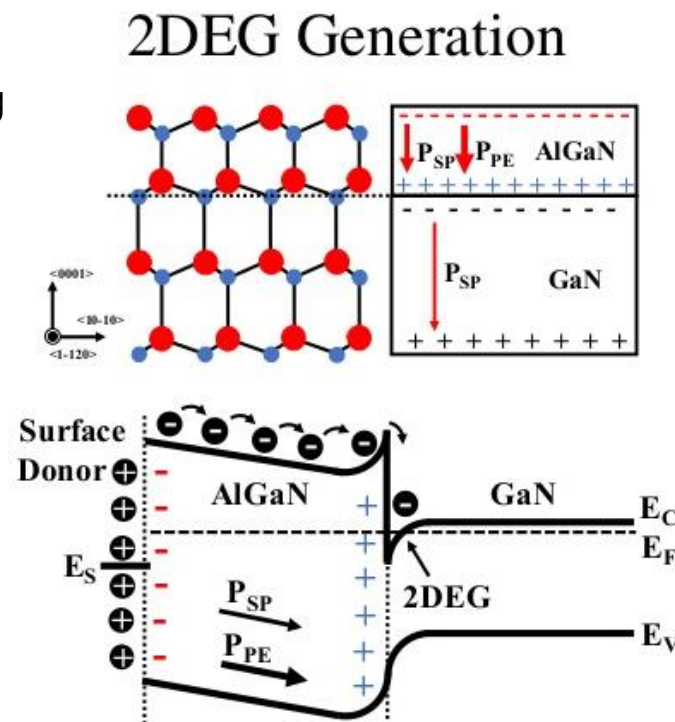
SiC

- Development of device fabrication processes for photonic and quantum-electronic applications
 - Development and application of ALE processes
 - Detection of sidewall roughness

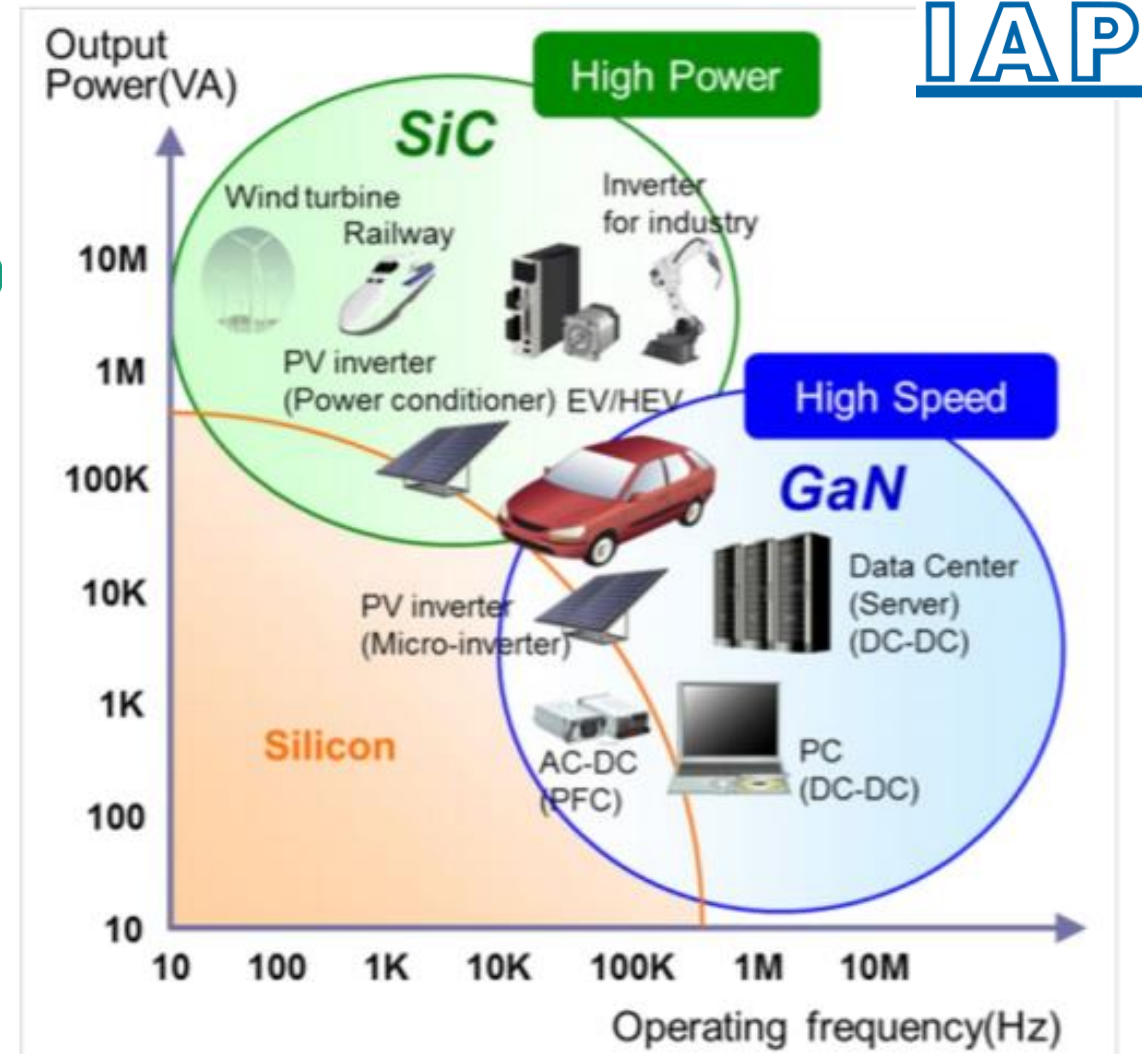
Nitride devices

AlGaN/GaN - High Electron Mobility Transistor (HEMT)

- High Breakdown voltage
- High frequency switching
- Compact size



<https://www.slideshare.net/PojungLin/gan-epitaxy-grown-on-si-substrate>

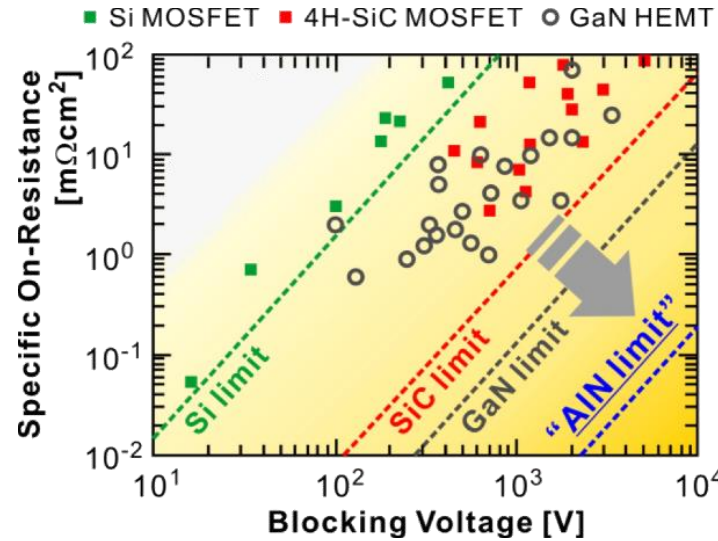


<https://tw.tek.com/blog/look-back-apec-thoughts-gan-products>

Atomic Layer Etching (ALE)

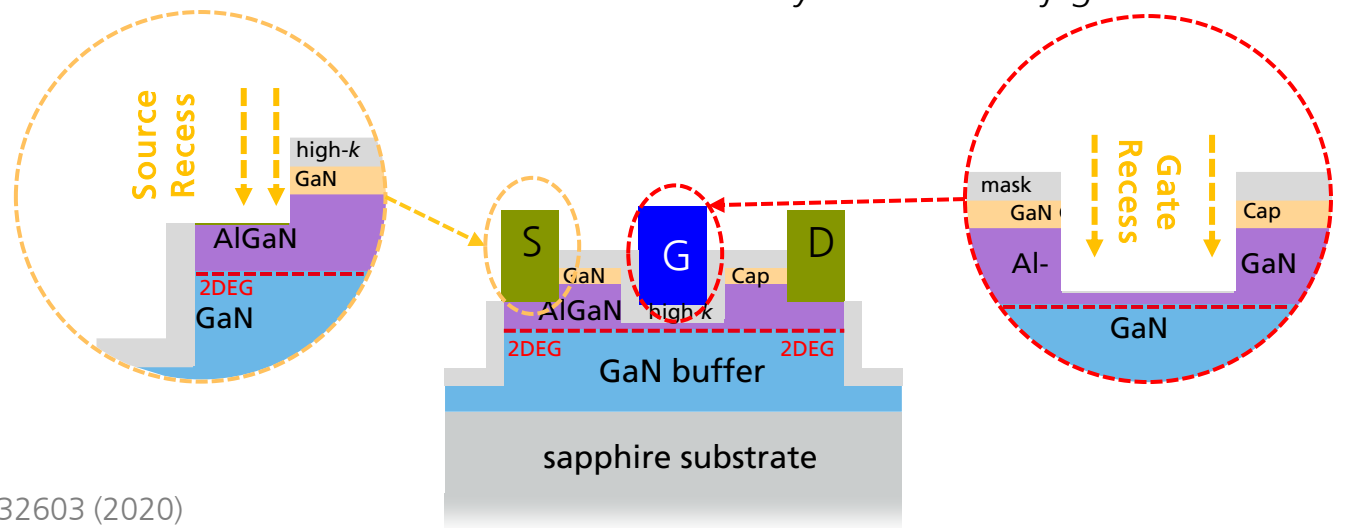
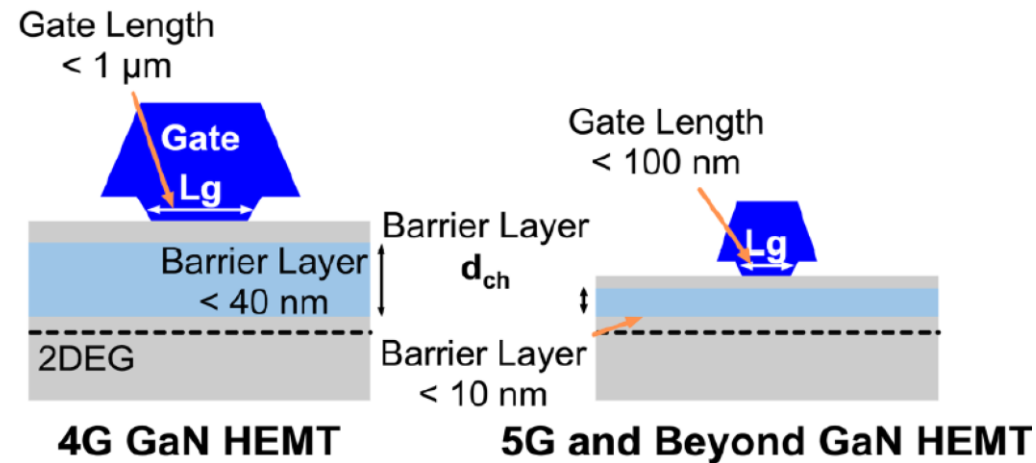
Motivation

- fast development in semiconductor industry
 - decreasing structure size (thinner layer, few nm) → low etching rates needed
 - increasing requirements to precise etching processes (low damage & surface roughness)
 - etching on a atomic layer level



(<http://www.inrel-npower.eu/node/21>)

- Optimizing process time for more sustainable fabrication
- using AlGaN/GaN HEMT as test device
 - improving contact resistance by recess etch
 - reach **enhanced mode** (e-mode) / *normally-off* HEMT by gate recess



D. Ohori et al., *J. Vac. Sci. & Tech. A: Vacuum, Surfaces, and Films* **38**, p. 32603 (2020)

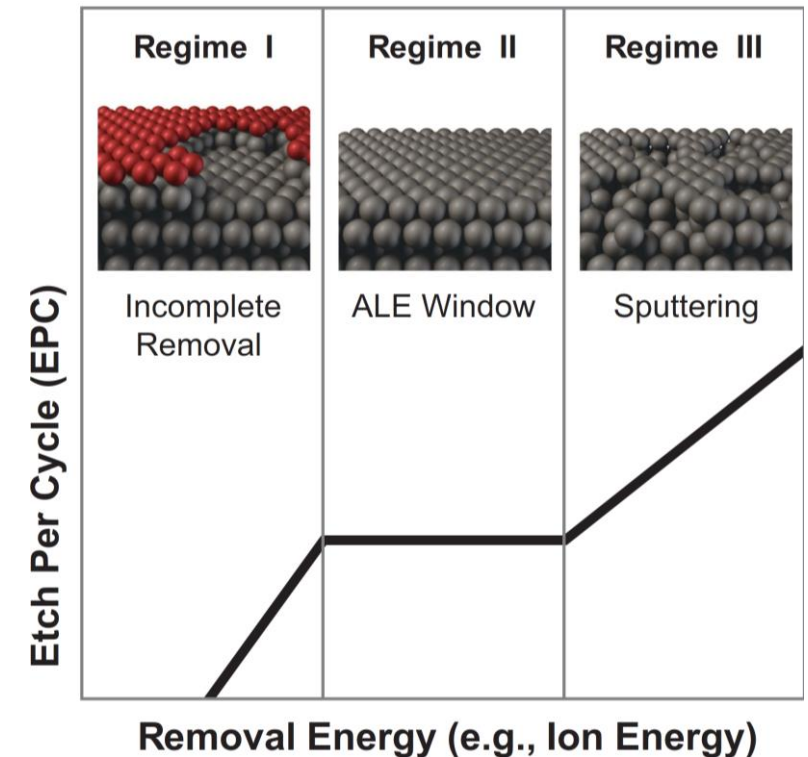
Principle of atomic layer etching (ALE)

Surface modification + energy-selective removal

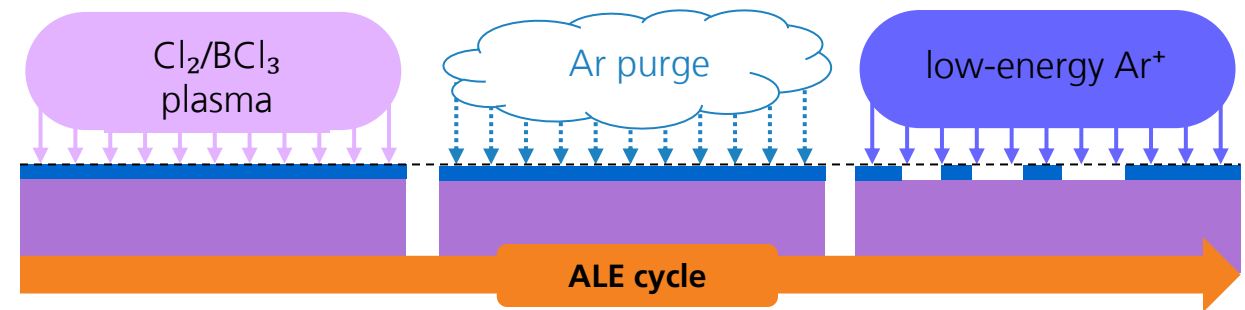
- **Definition** | ALE removes ultrathin layers through sequential, self-limiting surface reactions.
- **1. Modify** | Change only the near-surface chemistry (e.g. Cl_2/BCl_3 plasma for III-nitrides).
- **2. Remove** | Use low-energy Ar^+ ions to selectively remove the modified layer.
- **ALE window** | Ion energy is above the removal threshold but below bulk sputtering.
- **Outcome** | Repeatable etch per cycle (EPC), high synergy, reduced damage and potential surface smoothing.

Kanarik et al., *J. Vac. Sci. Technol. A* **35**, 05C302 (2017)

Guan et al., *J. Semicond.* **43**, 113101 (2022).



Kanarik et al., *J. Vac. Sci. Technol. A* **33**, 020802 (2015)
doi:10.1116/1.4913379

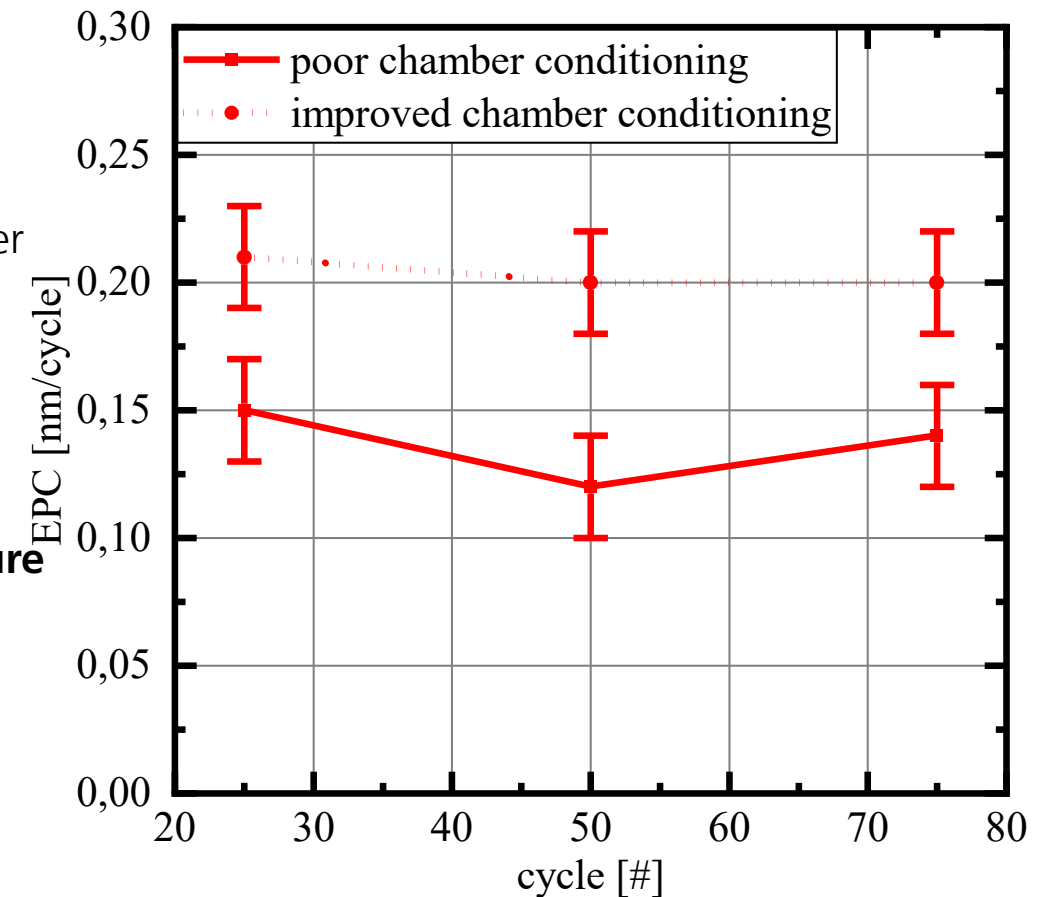


Impact of H₂ on our standard ALE processes

Importance of chamber conditioning

- chamber condition changed after implementing H₂ etching processes
 - H₂ plasma reduces chlorine compounds on the chamber wall
 - our established ALE recipe showed drastic drop in EPC
- primary cleaning procedure including three steps using a sapphire carrier wafer has to be expanded by 4th step
 1. SF₆/Cl₂ plasma removes Ga-, Al-, SiOCl compounds
 2. SF₆/O₂ plasma removes SiCl_x-, SiOCl compounds
 3. O₂/Ar plasma removes carbon residues
 4. **implementing hydrogen as fourth step in cleaning procedure**
→ ensures consistent initial process condition
- EPC for poor chamber conditioning recipe → **0.11 nm/cycle**
- EPC for improved chamber conditioning and recipe → **0.25 nm/cycle** [*]

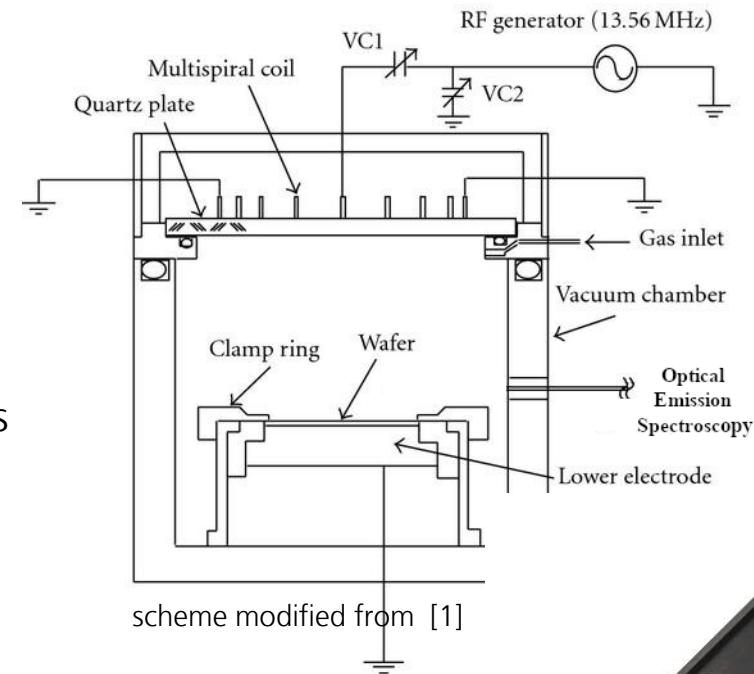
[*] equates 1 Bi-Layer of Ga(Al)-N



Optical Emission Spectroscopy (OES)

Application in ALE and RIE

- **OES:** non-invasive, in-situ analysis of plasma emission and composition.
- **Gas chemistry:** identifies etch species and reaction products (e.g. Cl, Cl⁺, SiCl_x).
- **Quantification:** estimates absolute or relative species densities.
- **Process monitoring:** tracks endpoints, chamber conditioning, contamination and drift.
- **ALE cycles:** resolves modification/removal steps and memory effects to optimize self-limitation.



[1] T. Okumura, Physics Research International 2010 (2010).

OES for inline process monitoring

Full spectra tracking during each ALE process

- full optical emission spectra during **(1)** modification and **(2)** removal step

- detection of specific emission lines:

1. modification step (1)

- Cl radical (725 nm, 741 nm, **837 nm**)
- additional emission lines: AlCl from chamber wall reaction, SiCl_x from silicon-carrier

2. removal step (2)

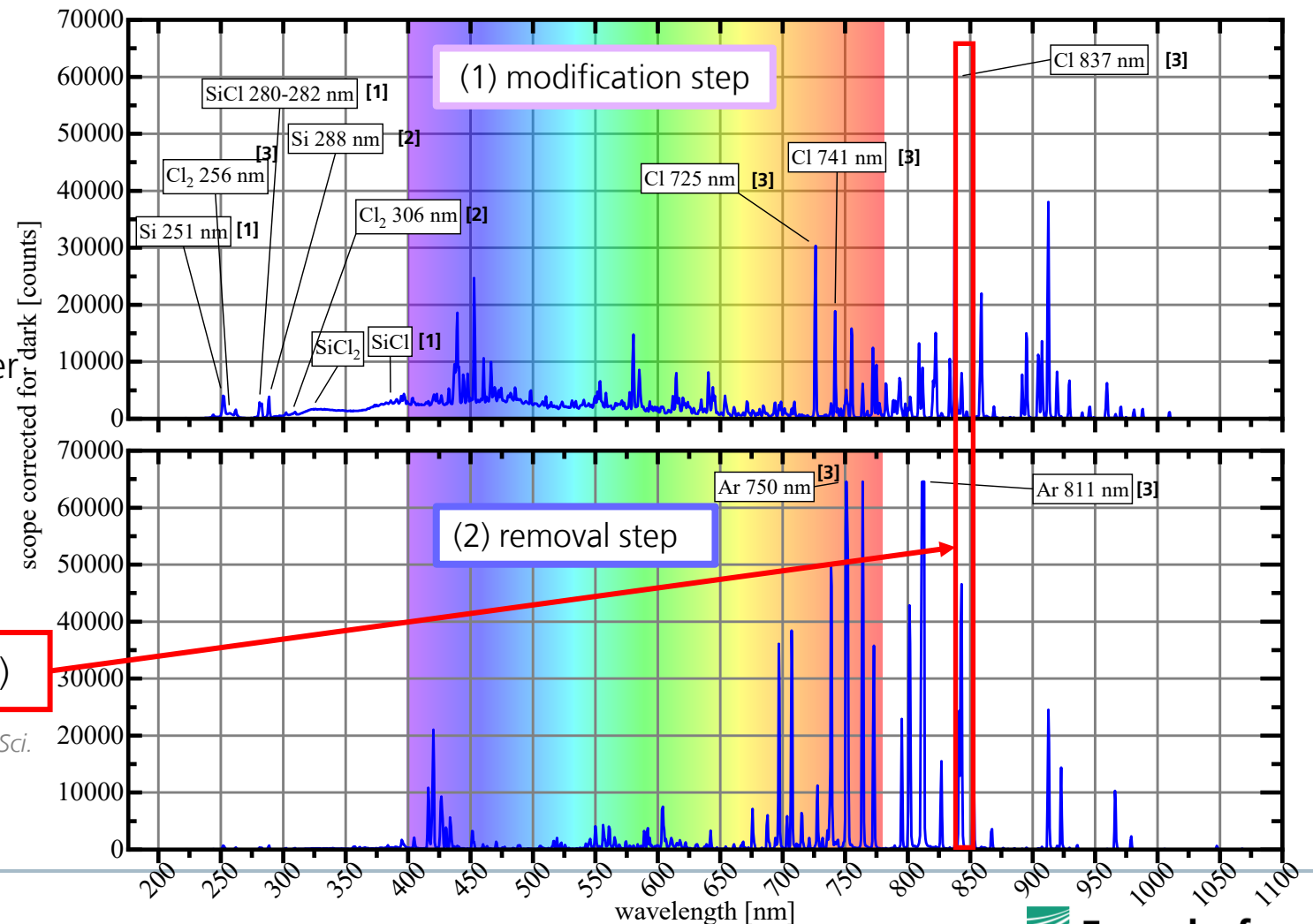
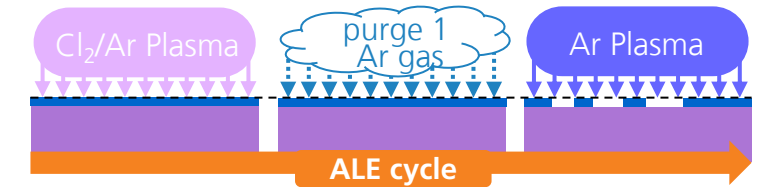
- Ar ion lines (750 nm, 811 nm) most intensive lines

- separation of specific Cl emission line (837 nm)

[1] Q. Hao, P. Kim, S. K. Nam, S.-Y. Kang, and V. M. Donnelly, *J. Vac. Sci. Technol. A* **41** (2023)

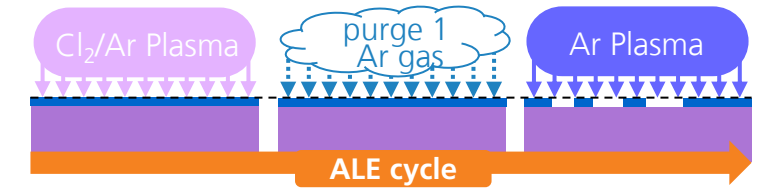
[2] T. Ma, T. List, and V. M. Donnelly, *J. Vac. Sci. Technol. A* **35** (2017)

[3] A. V. Dunaev and T. A. Zhukova, *Russ Microelectron* **51**, 76 (2022)

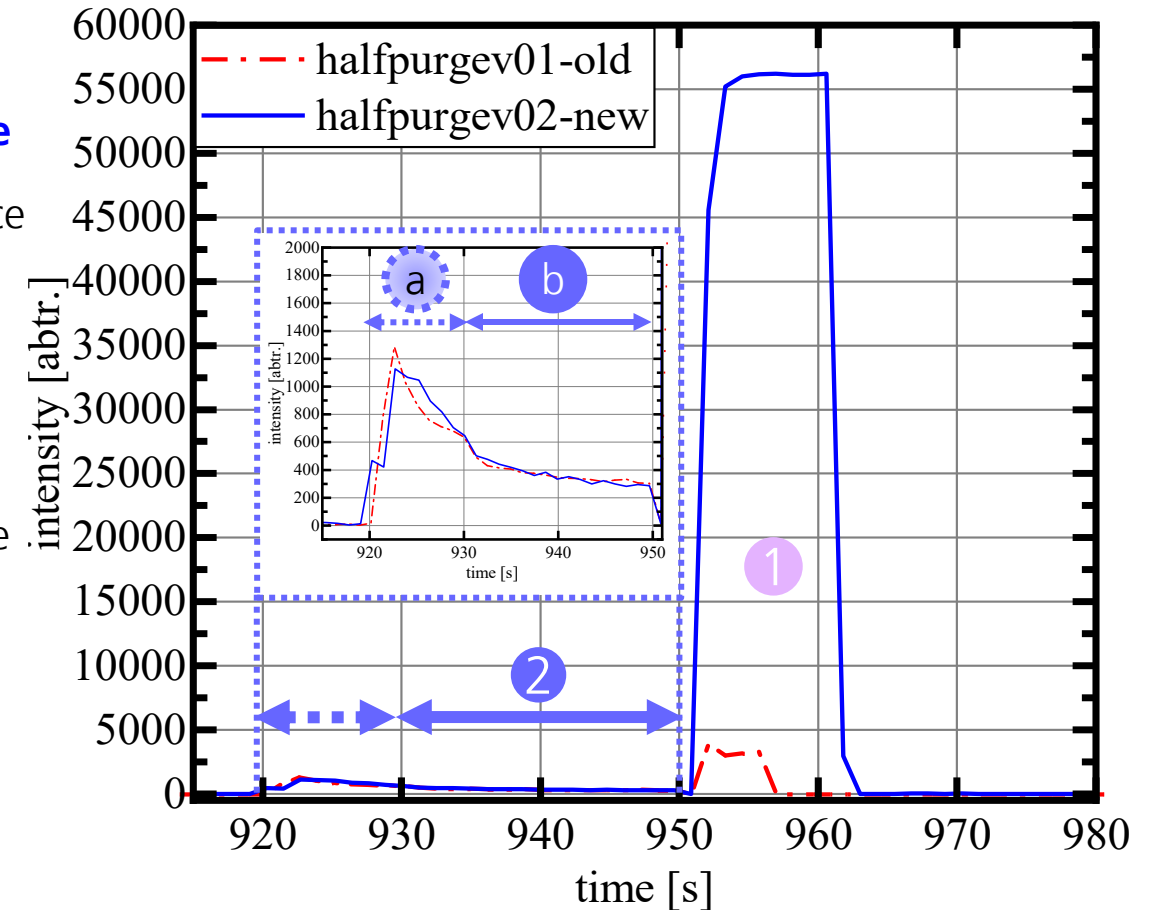


AlGaIn/GaN process optimization using OES

Observation of separated emission line for single ALE cycle



- Time-resolved OES of separated **Cl radical (837 nm)** for **(1)** modification & **(2)** removal step of single ALE cycle for both recipes **poor chamber** vs. **improved chamber condition recipe**
- increasing Cl radical concentration in **(1)** for more effective surface chlorine saturation (>15 times higher intensities) by
 - increasing Cl₂ flow rate
 - increasing ICP power
 - adding Ar to modification step
- detection of chlorine residues during removal step **(2)** → decrease in self-limitation → longer Ar times increases parasitic etching
 - a** Ar plasma without bias (stabilization time), Cl intensity at same level → probably memory effect (parasitic etching)
 - b** Ar plasma with bias
 - purging with Ar plasma potentially be more effective

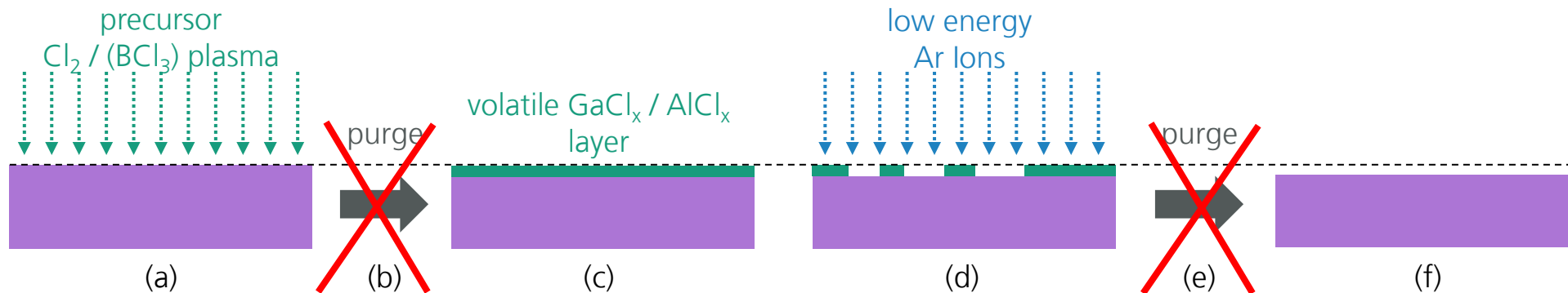


PEALE principle

General process for **full purge**, **half purge** and **purge free ALE mode**

▪ ICP reactor from Sentech at RT

1. **surface modification** by a chemical precursor (fig. a-c): **Cl₂/ BCl₃ plasma**
→ producing volatile GaCl_x and AlCl_x products
2. **removal of modified layer** (d-f) by low energy **Ar ions with bias**



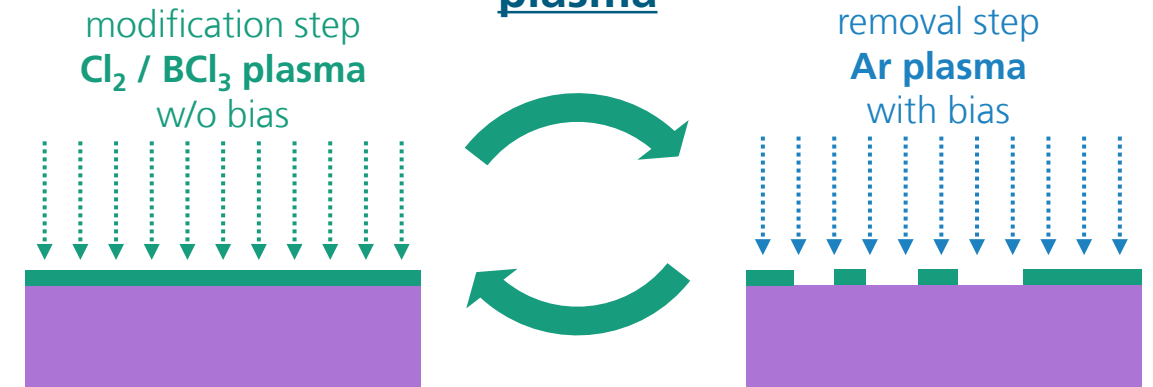
C. Miersch et al. *J. Vac. Sci. Technol. A* **43**, 042603 (2025)

PEALE modes

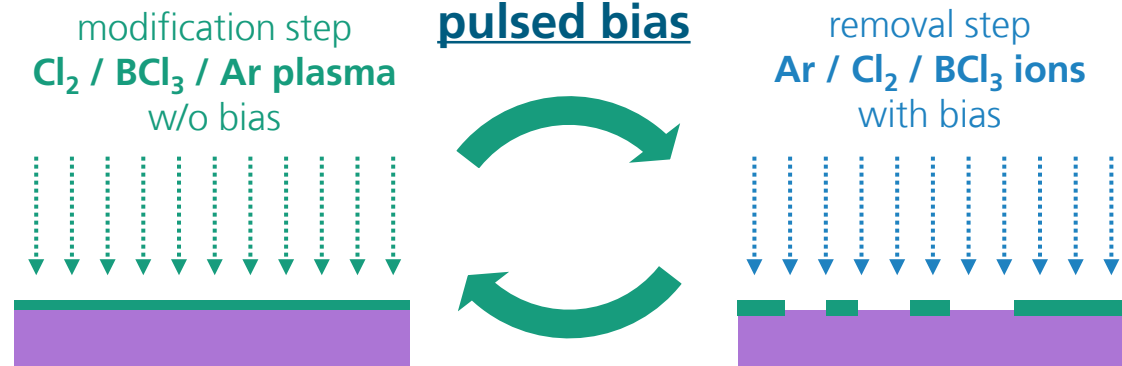
ALE process scheme for **pulsed bias** and **continuous plasma**

- modification by **separated gas chemistry** in continuous plasma
- removal of modified layer by accelerated low energy **Ar ions**

continuous plasma



pulsed bias



- modification by **unseparated gas chemistry** in continuous Cl₂/BCl₃/Ar plasma
- removal of modified layer by **pulsing RF bias** by accelerated **Ar/Cl₂/BCl₃ ions**

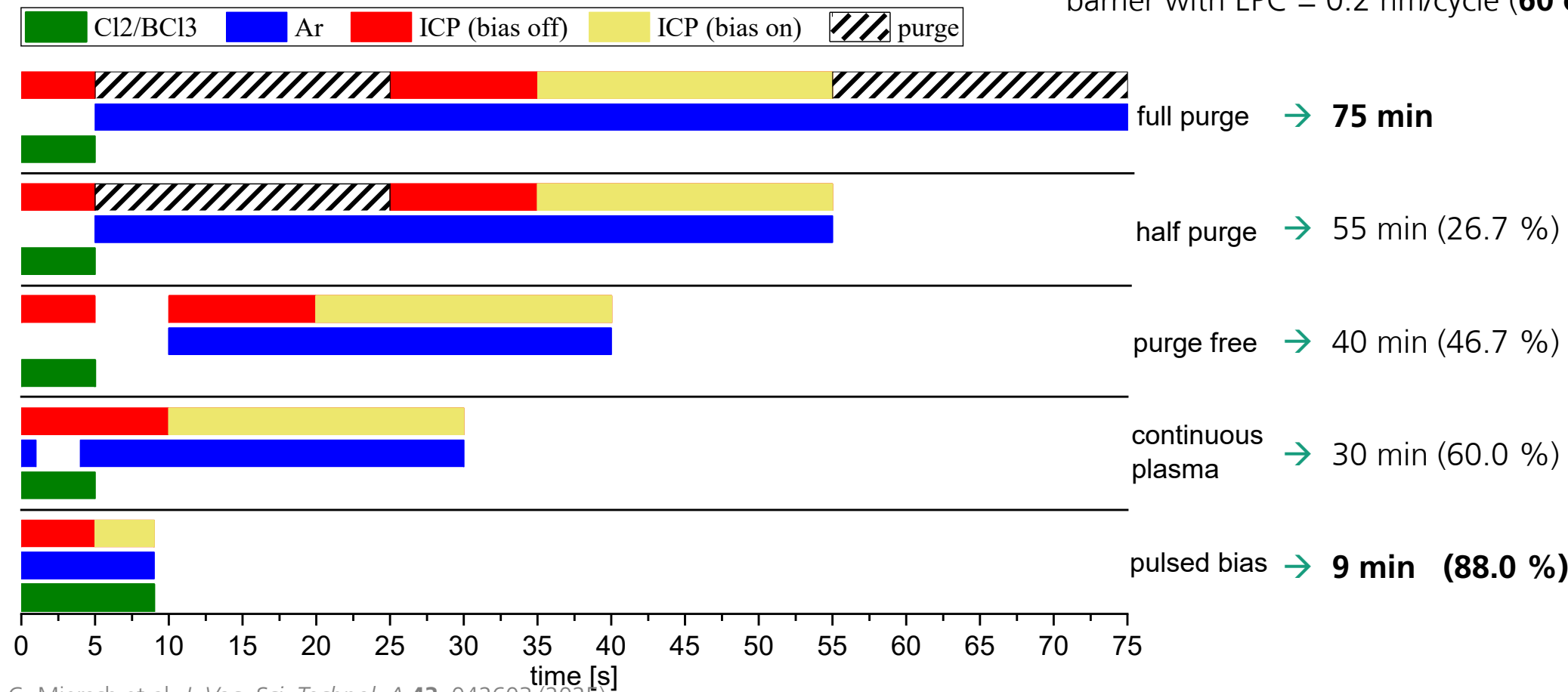
C. Miersch et al. *J. Vac. Sci. Technol. A* **43**, 042603 (2025)

J. A. Michaels, N. Deegan, Y. Tsaturyan, J. R. Renzas, D. D. Awschalom, J. G. Eden, and F. J. Heremans, *J. Vac. Sci. Technol. A* **41**, 032607 (2023).

PEALE mode time reduction

Comparison of 5 ALE modes cycle times

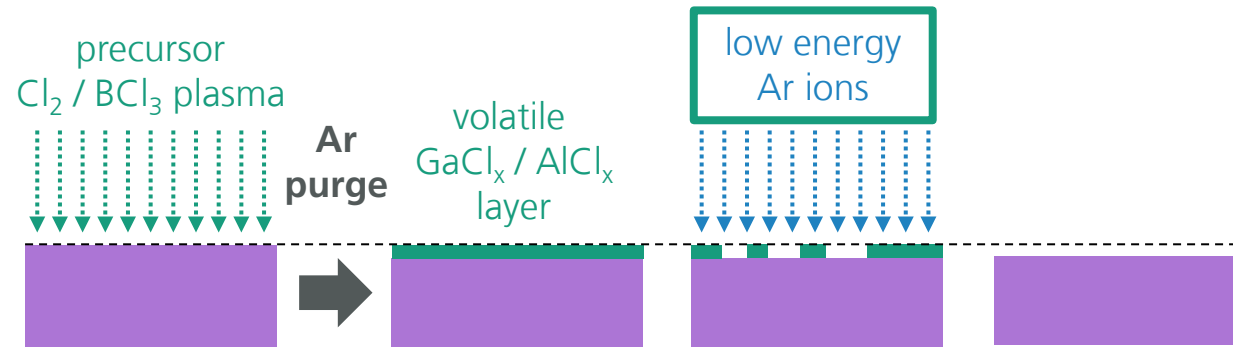
example: 50% recess etching of a 24 nm AlGaIn barrier with EPC = 0.2 nm/cycle (**60 cycles**)



C. Miersch et al. *J. Vac. Sci. Technol. A* **43**, 042603 (2025)

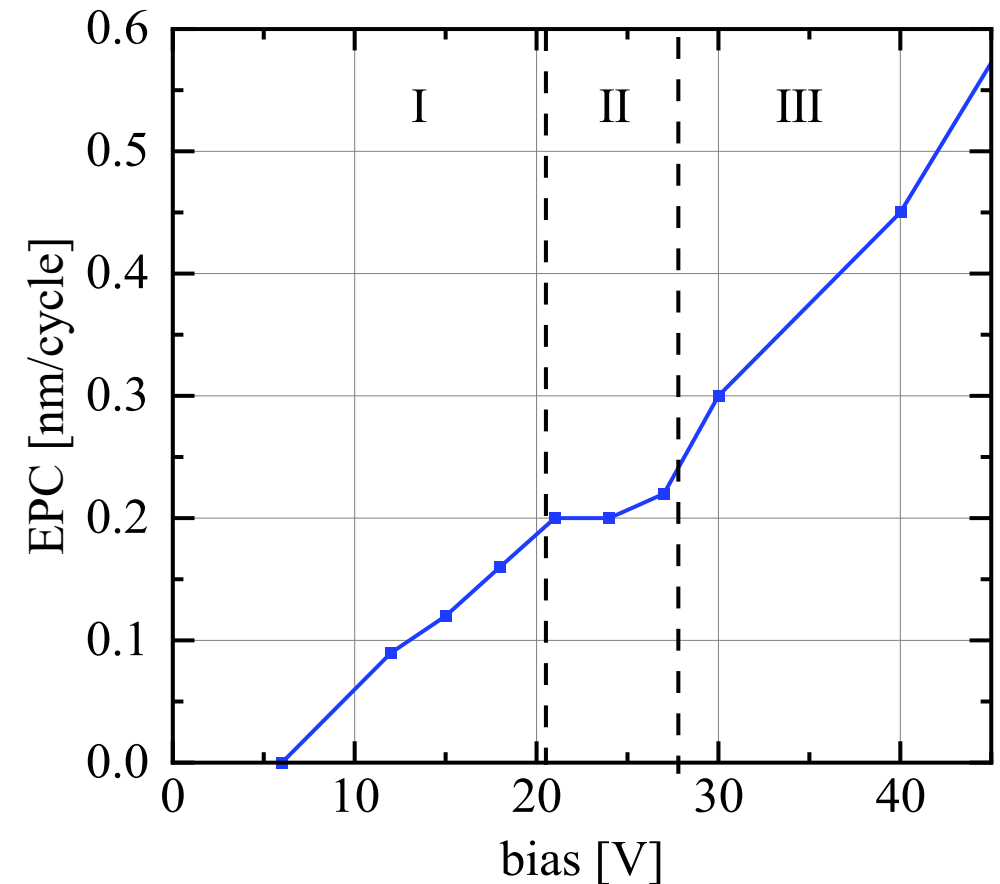
Optimization of present recipe using half purge as standard ALE mode

Energy scan



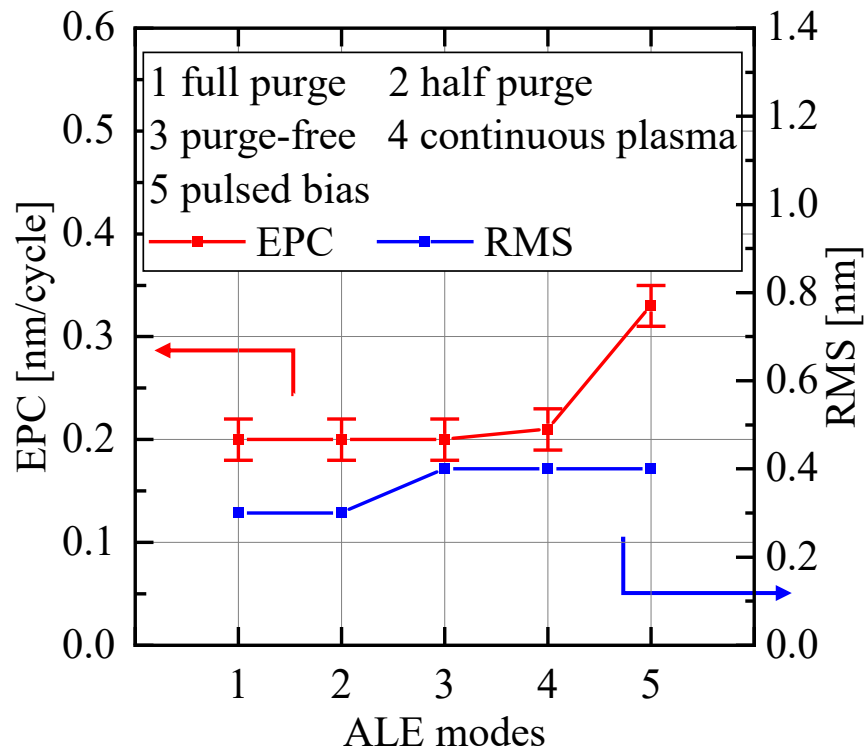
■ half purge mode as standard ALE mode

- I. no sufficient removal of etching products
- II. plateau / **ALE window** for bias range between **21 - 27 V**
→ **24 V** for standard recipe
- III. increasing EPC → sputtering unmodified layer



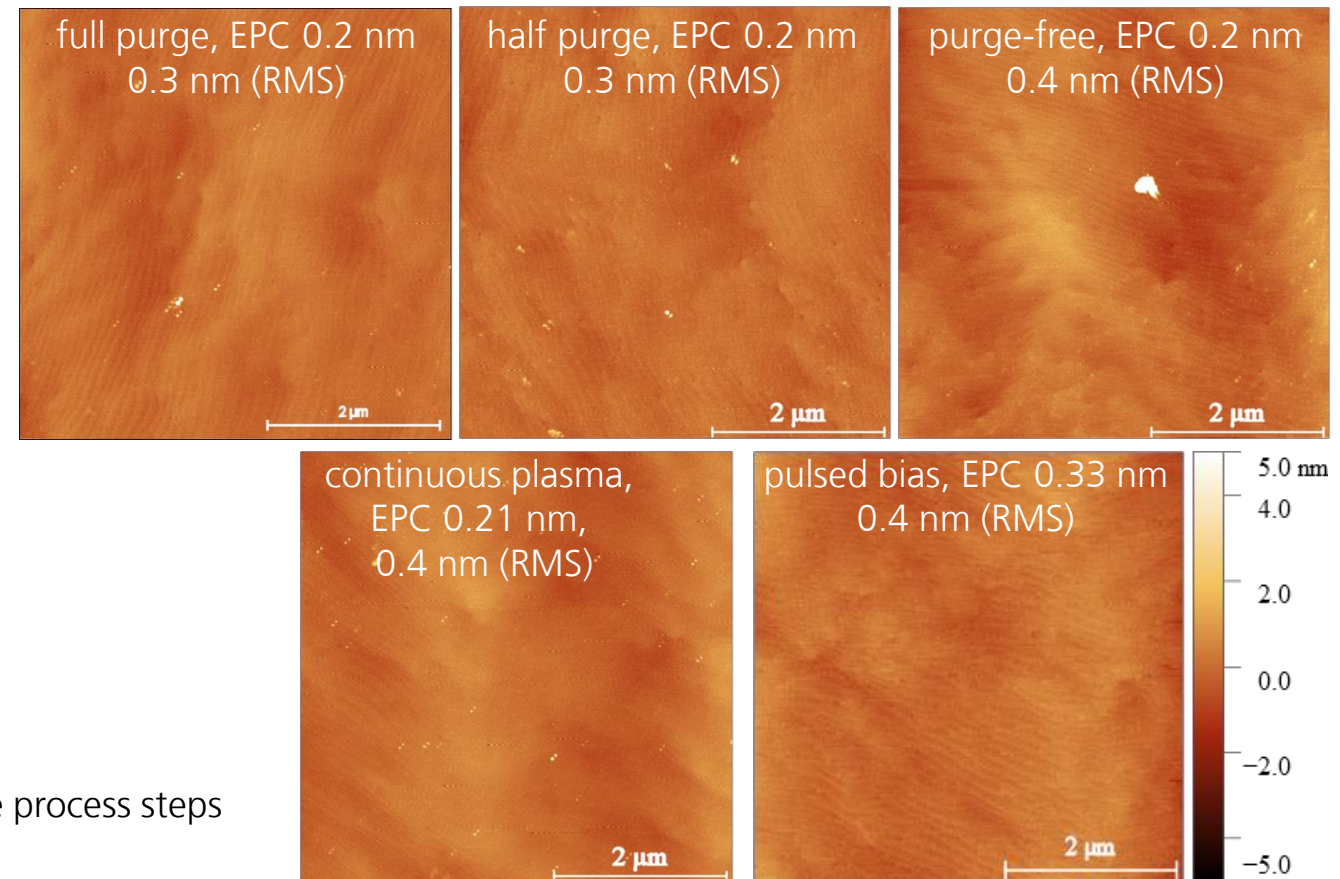
PEALE mode comparison

Results of surface morphology (AFM)



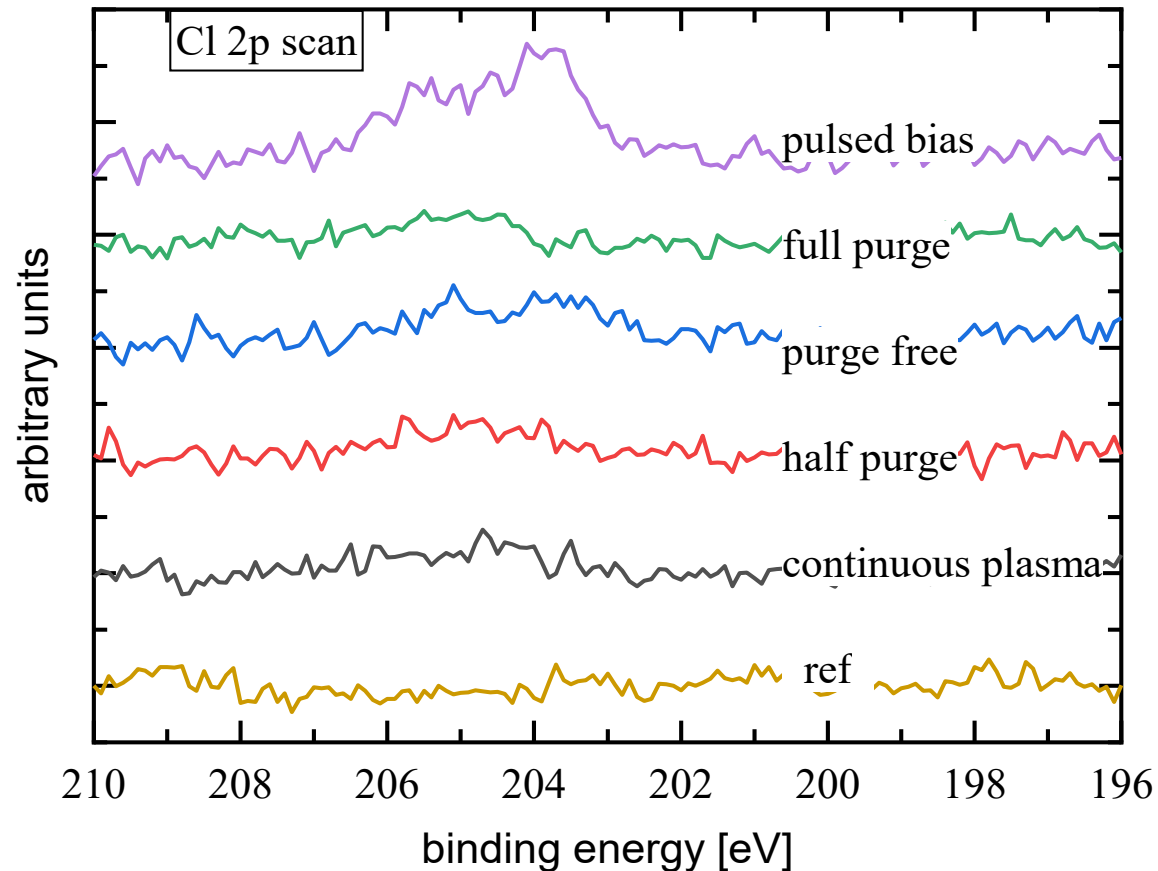
- comparable low roughness for all modes
- EPC increased for pulsed bias mode → no self limitation of the process steps
→ „quasi“ ALE process

C. Miersch et al. *J. Vac. Sci. Technol. A* **43**, 042603 (2025)



PEALE mode comparison

ex-situ XPS results of all 5 ALE modes concerning the Cl content



C. Miersch et al. *J. Vac. Sci. Technol. A* **43**, 042603 (2025)

- full / half purge, purge free and continuous plasma do not exhibit a significant chlorine content
 - within the ALE window with optimized parameters
→ **time reduction of 60 %** without quality loss using the **continuous plasma mode**
- **pulsed bias mode show slight chlorine contamination** due to accelerating Cl_2 , BCl_3 and Ar ions
 - assumption: accelerated Cl radicals produce strong bounded GaCl_x compounds on the surface not completely removed
 - additional post-treatments are necessary for removing

PEALE on AlGaN/GaN heterostructures

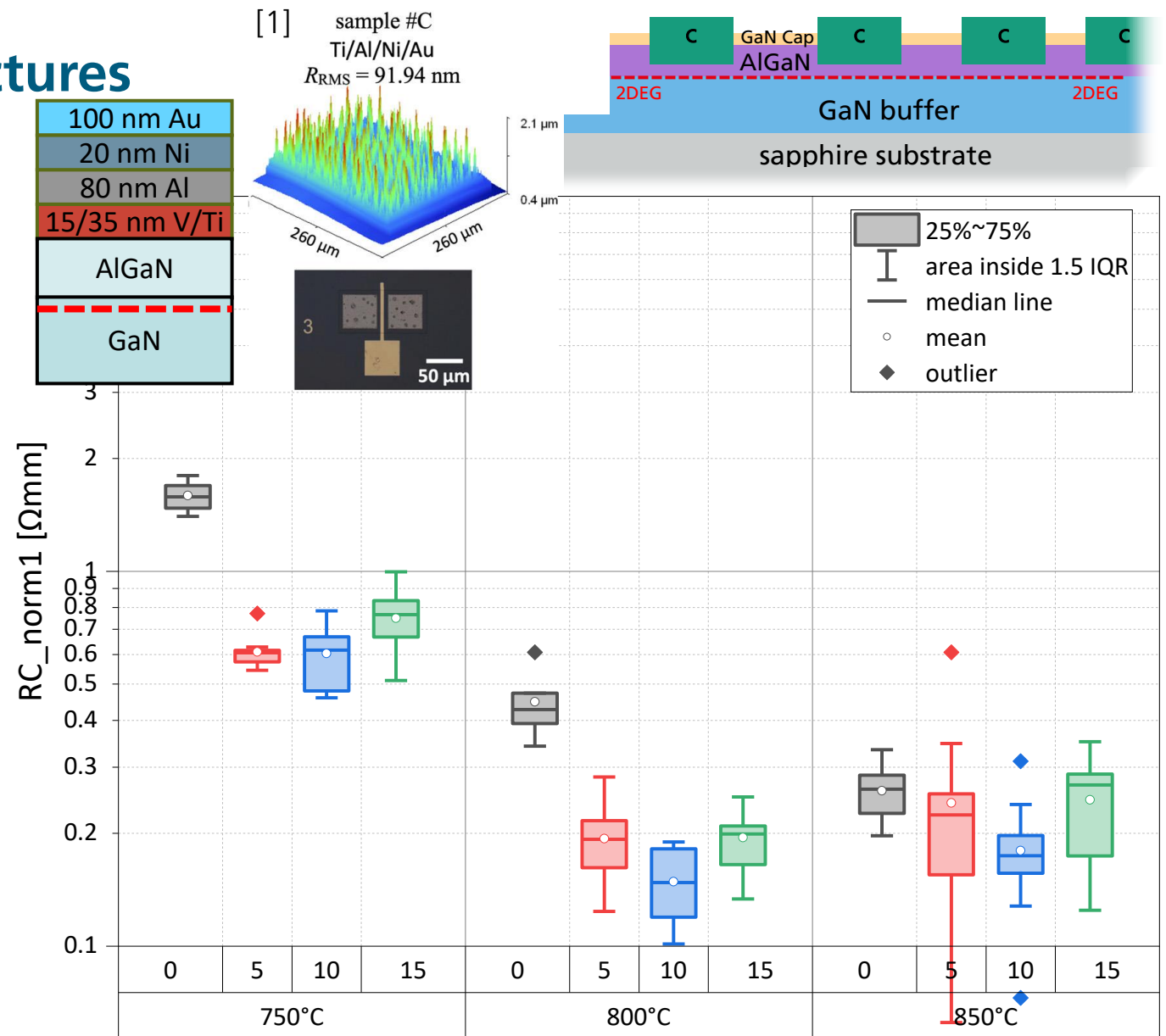
Source / Drain recess

Results of electrical characterization of the TLM structures

- measured on TLMs for Au-based contacts
- recess etch improves ohmic contact by reducing the contact resistance for 750 °C, 800°C and 850°C annealing temperature
- visible trend → optimum achieved at 10 nm recess etch
- recess etch has higher impact on the contact resistance at lower annealing temperature

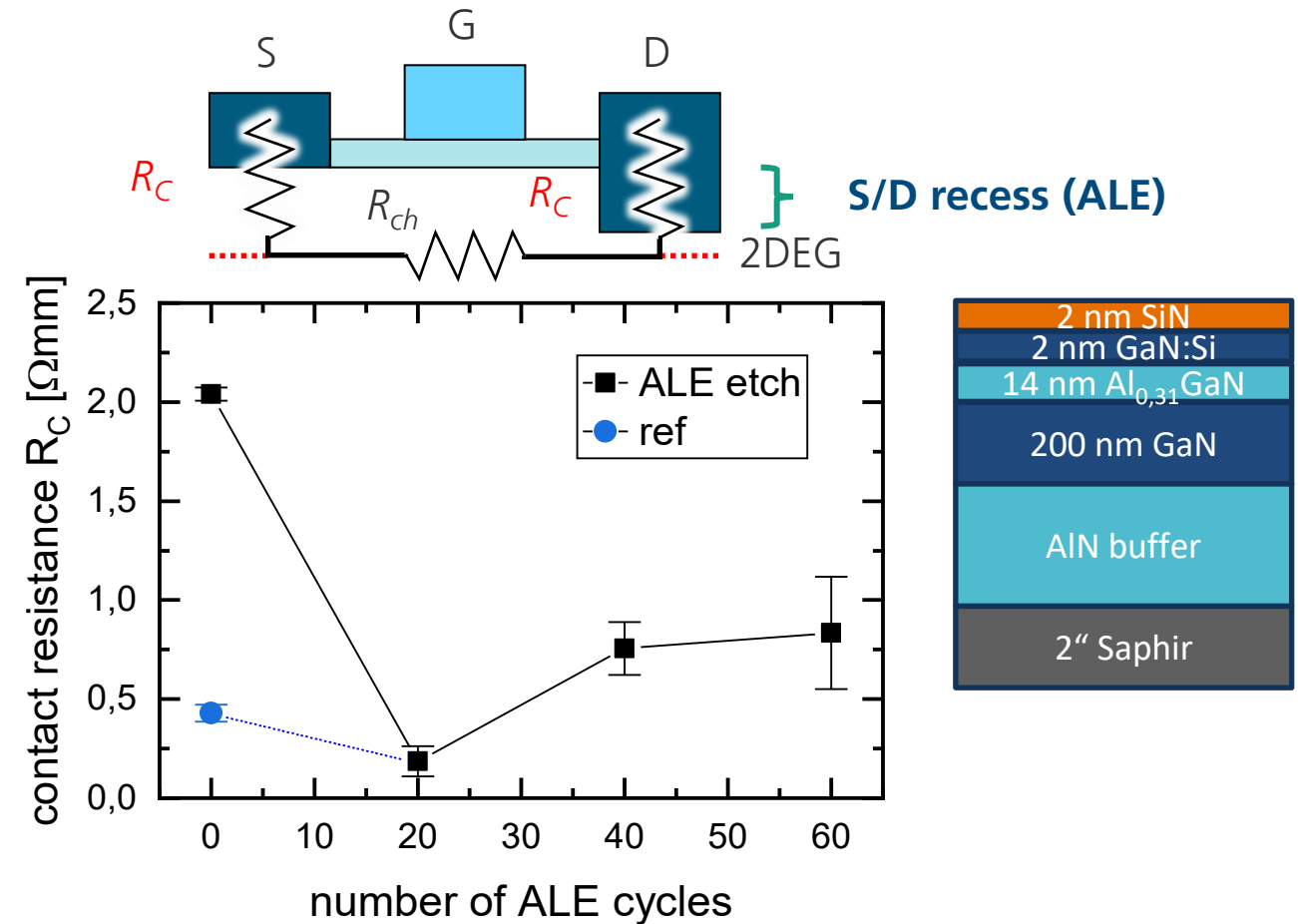
[1] V. Garbe et al. *Appl. Phys. Lett.* **123**, 203506 (2023)

C. Miersch et al., *J. Vac. Sci. Technol. A* **42**, 022604 (2024)



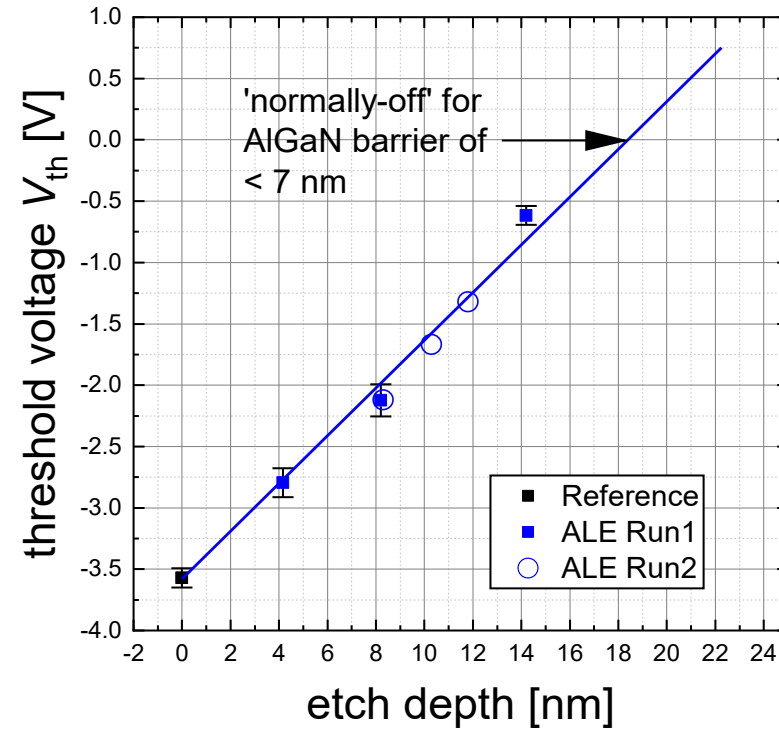
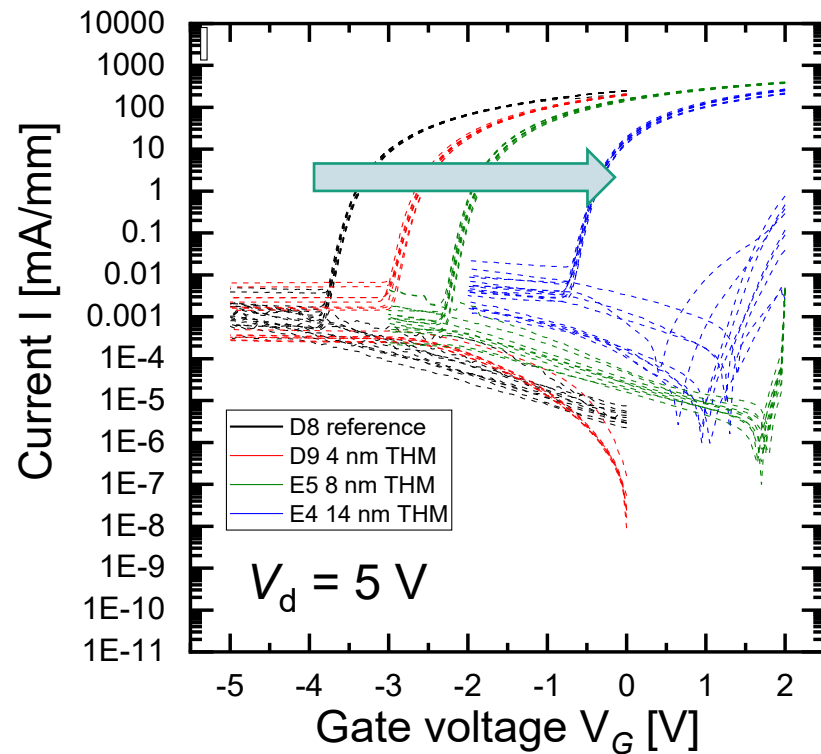
Systematic material screening for Al-rich $\text{Al}_{0,31}\text{Ga}_{0,69}\text{N}$

- Al-rich barrier (grading: $x = 0.25 \dots 0.60$, avg. 0.31)
- reduction of R_C by local recess of the S/D areas
- process:
 - SiO_2 hard mask
 - atomic layer etching (ALE) with Cl_2
 - deposition of Zr/Al/Ni/Au with thickness of 30/80/20/100 nm
 - anneal: 300 s @ 800°C
- R_C of **0.19 Ωmm** after 20 ALE cycles
 - etch depth $\sim (4 - 6)$ nm
 - reference w/o ALE: 0.43 Ωmm

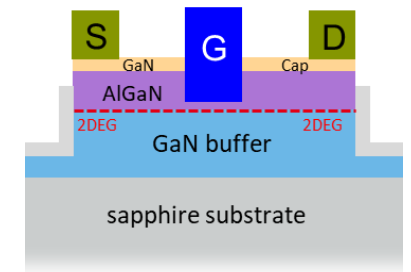


PEALE on AlGaN/GaN heterostructures

HEMTs with gate recess



- good overall behaviour for non passivated short loop HEMTs
- linear behaviour between etch depth and V_{th}
- Reproducible for fixed process flow
- New results indicate no significant difference for different ALE modes (excluding bias pulsed mode)

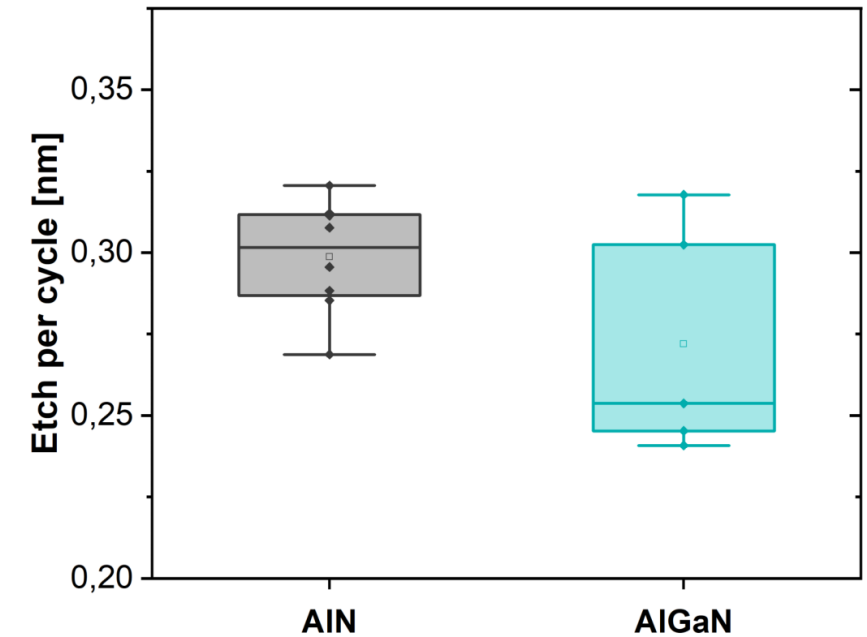
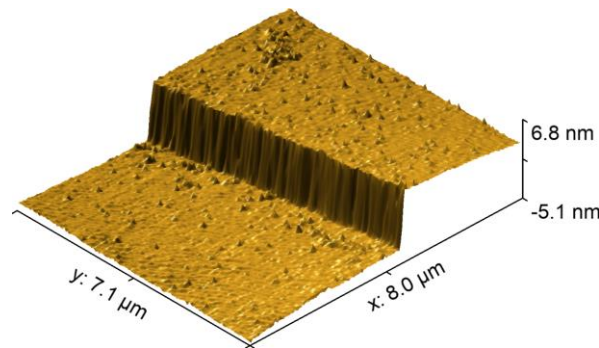


C. Miersch et al., *J. Vac. Sci. Technol. A* **42**, 022604 (2024)

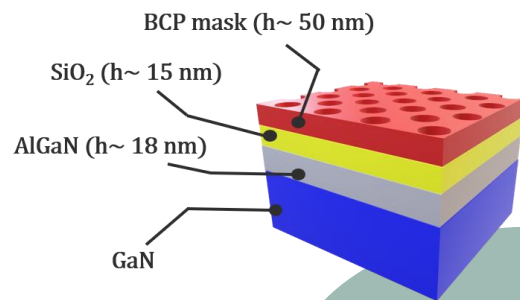
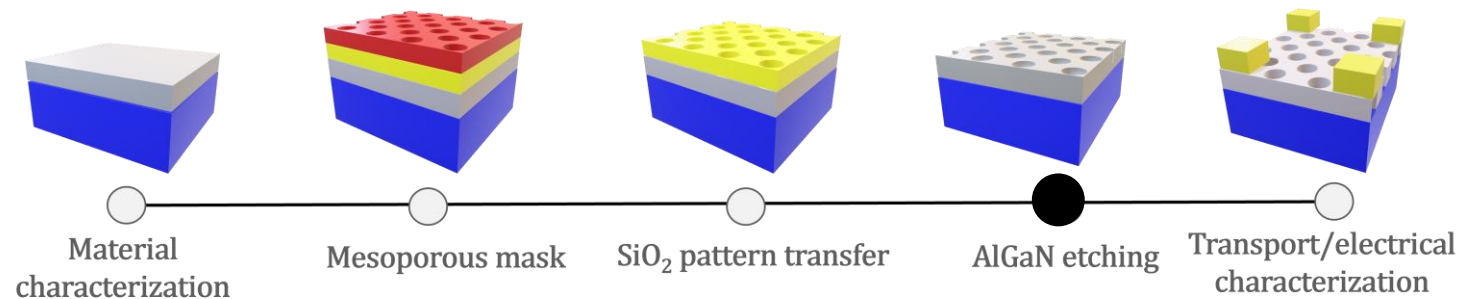
PEALE on sputtered AlN

ALE on AlN

- (1) Cl_2/Ar plasma | ICP power: 400 W | pressure: 0.5 Pa | RT
- (2) Ar plasma | ICP power: 200 W | bias: -25V | pressure: 0.7 Pa
- etch per cycle (EPC)
 - AlN: 0.30 nm
 - $\text{Al}_{0.24}\text{Ga}_{0.76}\text{N}$: 0.27 nm



ALE applied for Block Copolymer for Nanopatterning



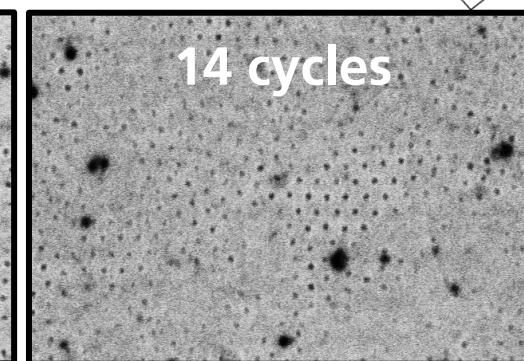
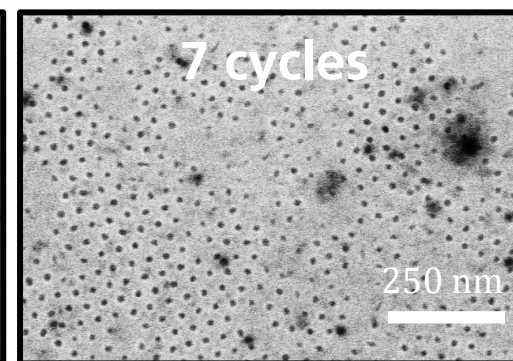
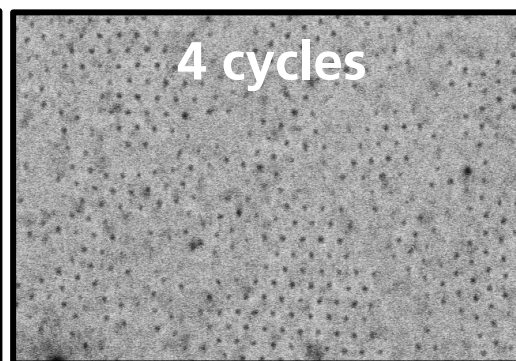
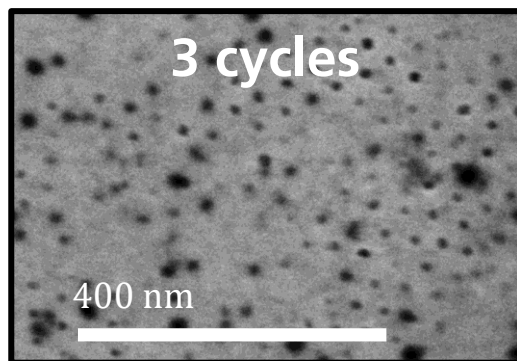
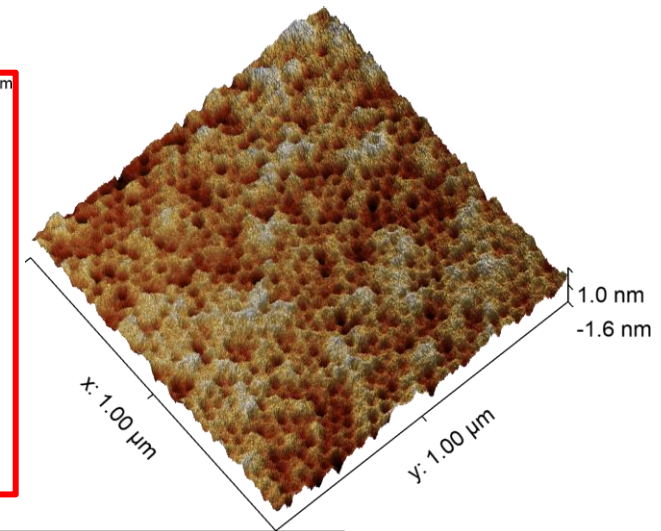
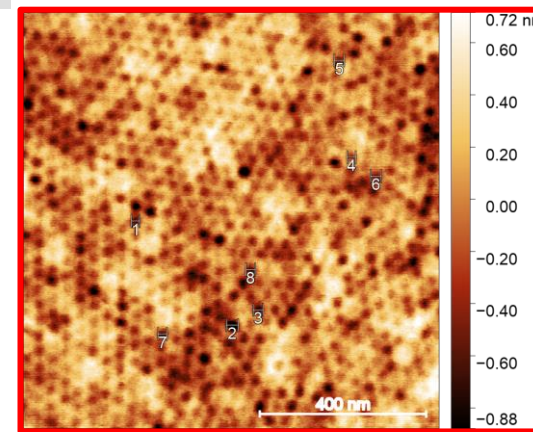
A. Patelli Poster Session Tuesday

Diameter = 20 ± 2 nm

$L_0 = 35 \pm 1$ nm

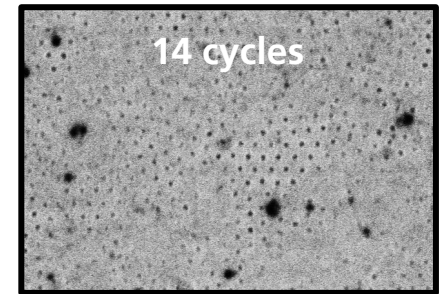
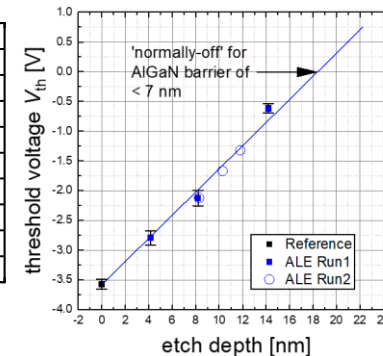
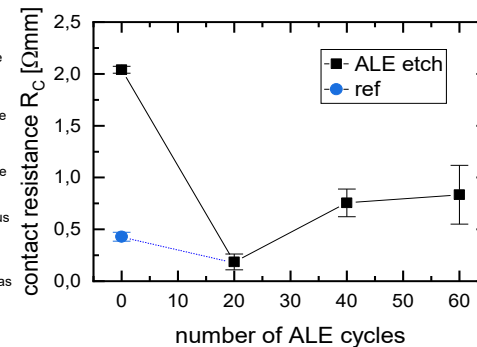
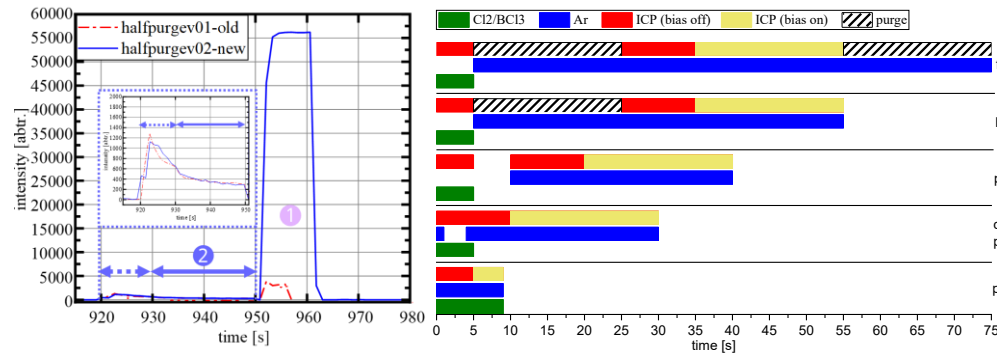
Controlled and efficient process

Transferred hexagonal pattern



Summary - Nitrides

- In-line OES enables monitoring and optimization of ALE, cleaning, and conditioning. → Optimized Cl-radical concentration improves surface saturation.
- Five ALE modes developed for AlGaIn/GaN heterostructures. → Optimized ALE parameters cut process time by >60% without compromising etch or surface quality.
- Lower ohmic contact resistance achieved in AlGaIn/GaN and Al-rich AlGaIn/GaN HEMTs.
- ALE successfully applied to gate-recess etching of AlGaIn/GaN HEMTs. → Electrical characterization reveals a linear relationship between V_{th} and etch depth.
- First PE-ALE processes demonstrated for sputtered AlN thin films on Si and block polymer structuring.



Outline

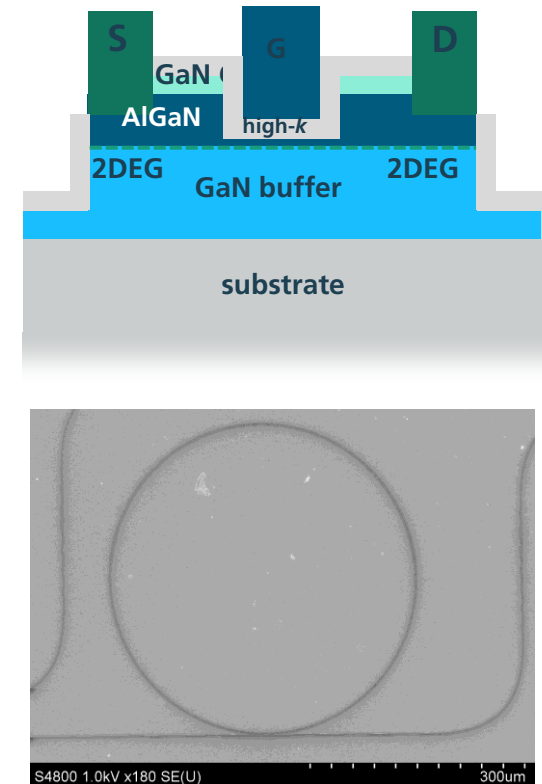
Development and characterization of ultra wide band gap (UWBG) (test) devices

Nitrides

- Development of device process steps for e-mode HEMTs

SiC

- Development of device processing for photonics and quantum electronics
 - Realization of ALE process and their application
 - Side-wall roughness detection



SiC combines quantum functionality with engineering robustness

No photonic platform is universal - SiC covers an unusually broad application space.

[1] Integrated photonic platforms - The case for SiC (2024)
[2] Boretti, Li, and Casteletto, *Optics & Laser Technology* **181** (2025) 111910

MATERIAL	DISTINCTIVE ADVANTAGE	TRADE-OFF / MATURITY	BEST-FIT ROLE
Silicon	Mature process ecosystem; direct link to integrated electronics	Indirect bandgap; two-photon absorption at telecom wavelengths	Passive + electronic integration
III–V	Direct bandgap and efficient light emission	Specialist active-material platform	Integrated lasers
Other platforms	Complementary strengths across photonic building blocks	Specialized rather than universal	Specialized components
SiC	Wide bandgap, color centers, high thermal conductivity and mechanical strength	SiCOI, low-loss nanofabrication and coupling still maturing	Quantum • nonlinear • harsh-environment photonics

SiC’s edge → unusually broad combination of optical, quantum and environmental capability.

SiC's performance ceiling is set by fabrication quality^{a)}

Fabrication quality converts material potential into device performance.

01 CONFINEMENT

- SiCOI enables strong guiding
- thermal-expansion mismatch can introduce stress, cracks and dislocations

02 NANOFABRICATION

- **Sidewall roughness and crystal defects increase scattering**
- **high-Q resonators demand exceptionally smooth, pure material**

03 COUPLING & SCALE

- Efficient in/out coupling and reproducible profiles remain key
- angled etching has already been demonstrated on 5-inch wafers. [2]

DEMONSTRATED PERFORMANCE [3]

$Q \approx 1 \times 10^6$

ring resonator

$\approx 0.4 \text{ dB/cm}$

propagation loss

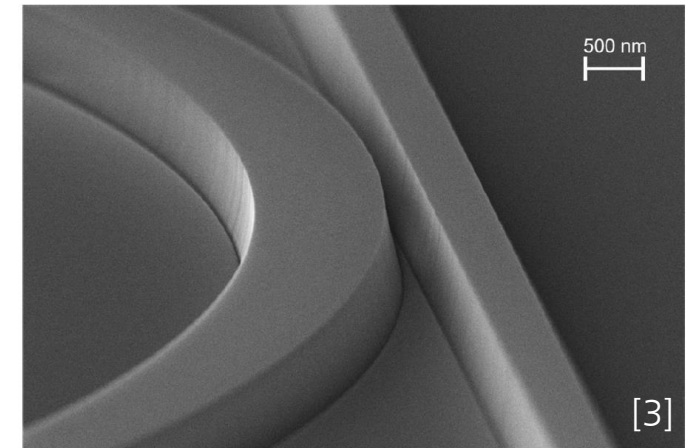
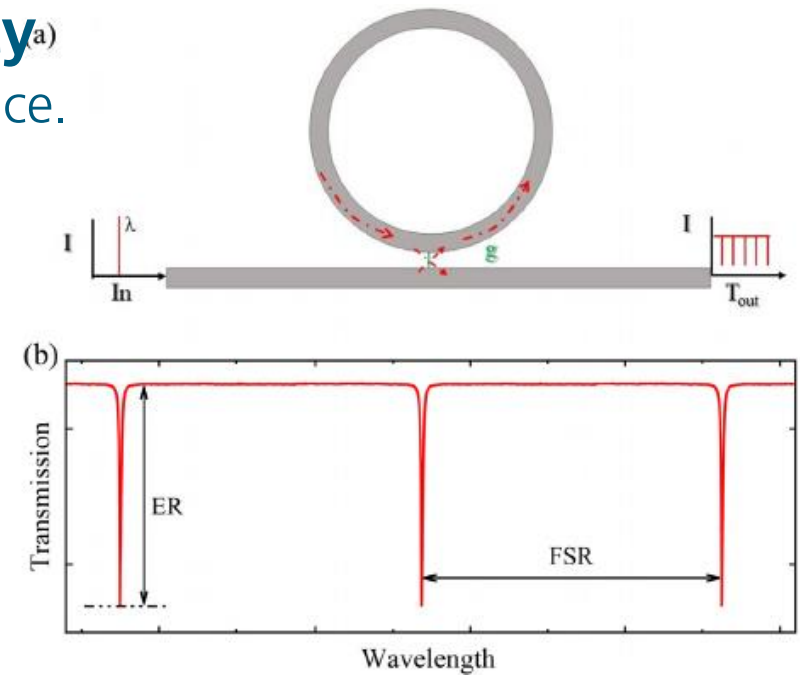
$< 1 \text{ nm}$

CMP roughness

[1] Boretti, Li, and Casteletto, *Optics & Laser Technology* **181** (2025) 111910

[2] Majety, S., Norman, V.A., Saha, P. et al. *npj Nanophoton.* **2**, 3 (2025)

[3] A. Afridi et al. *Appl. Phys. Lett.* **124**, 170502 (2024)



Cl-based ALE process for 4H-SiC

[1] M. Balooch and D.R. Olander *Surface Science* **261** 321 – 334 (1992)

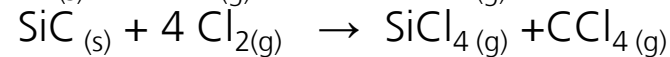
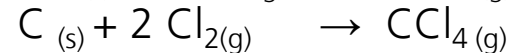
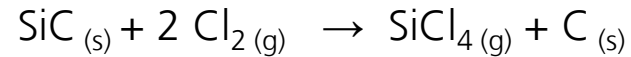
[2] J.E. Marra et al. *J. Am. Ceram. Soc* **71** 1067 -73 (1988)

[3] H. Habuka in *Physics and Technology of Silicon Carbide Devices* edited by Yasuto Hijikata (2012)

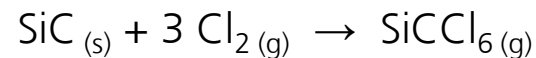
Transfer of chlorine based etching process from nitrides to SiC

1. surface modification by a chemical precursor Cl_2

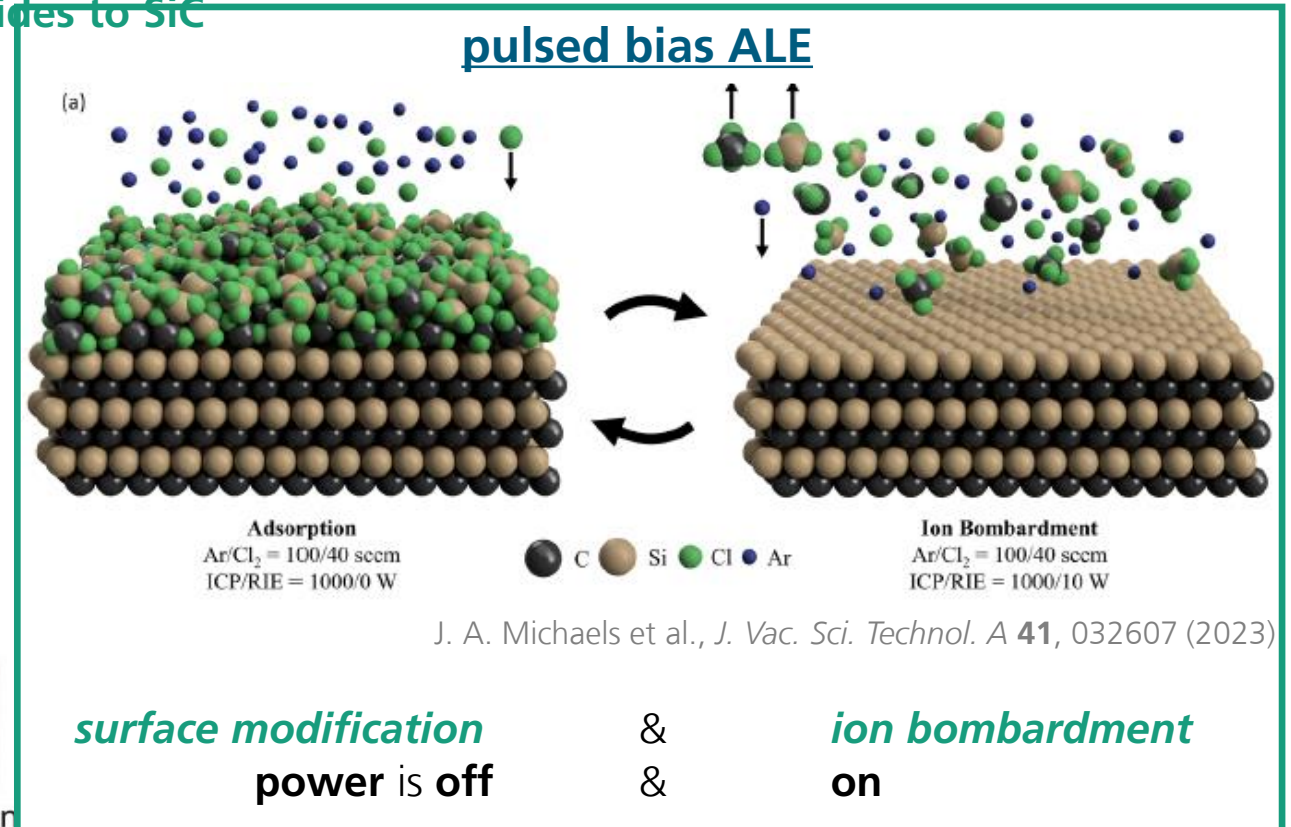
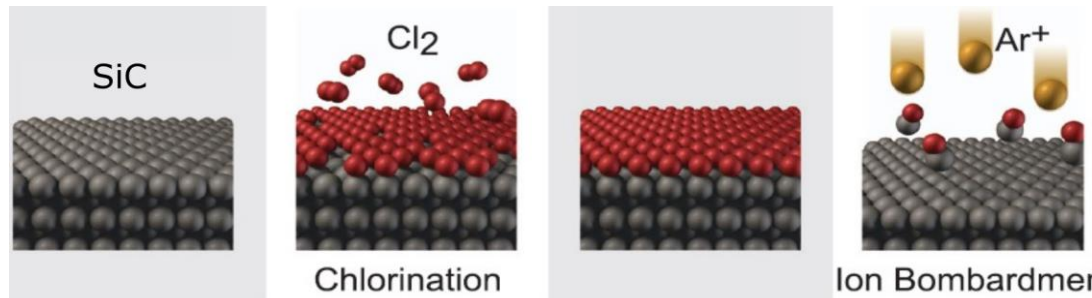
possible reactions [1, 2]:



Possible side reaction [3]:



2. removal of modified layer by low energy Ar^+ ions



J. A. Michaels et al., *J. Vac. Sci. Technol. A* **41**, 032607 (2023)

K. J. Kanarik et al, *J. Vac. Sci. & Tech. A: Vacuum, Surfaces, and Films*, **33**, 20802 (2015)

First results of ALE applied 4H-SiC surfaces

Investigation of surface roughness and etch rates

■ **modification step**

- surface is modified by reactant Cl_2
- self limitation: $\text{SiC} + 4 \text{Cl}_2 \rightarrow \text{SiCl}_4 + \text{CCl}_4$

■ **removal step**

- modified surface is removed by low energy Ar-ions
- self limiting nature enables precise etching of dimensions and low induced damage

■ **ALE window:** -15 V to -24 V bias

- EPC 2.5 Å → about bilayer thickness of 2.5 Å [1]

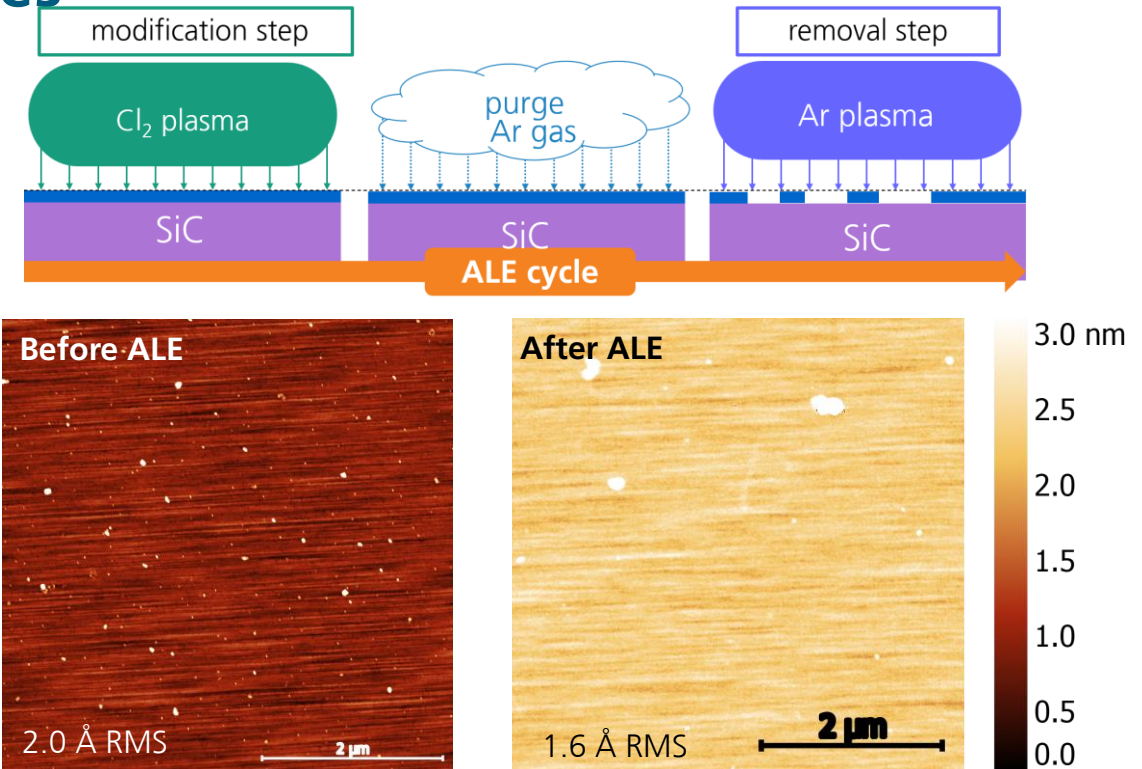
■ **Etching of different 4H-SiC materials**

- applied bias of - 18 V bias
- trend Si-face with higher EPC than C-face

→ due to different surface reaction rates of C and Si in SiC [2]

[1] W.Y. Ching et al. *Materials Science and Engineering A* **422** 147–156 (2006)

[2] M. Balooch, D.R. Olander, *Surface Science* **261** 321-334 (1992)



Surface roughness on SiCOI

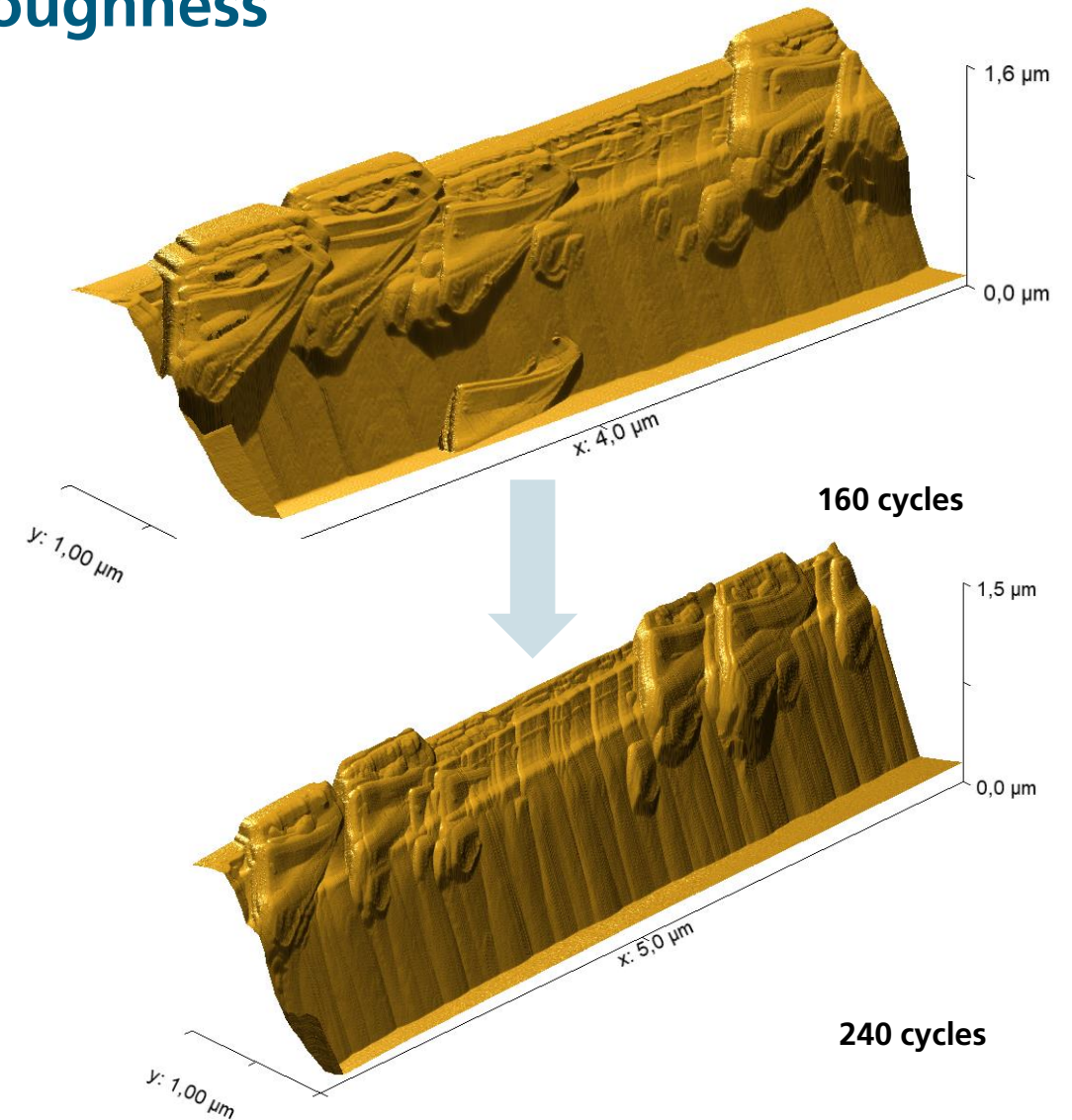
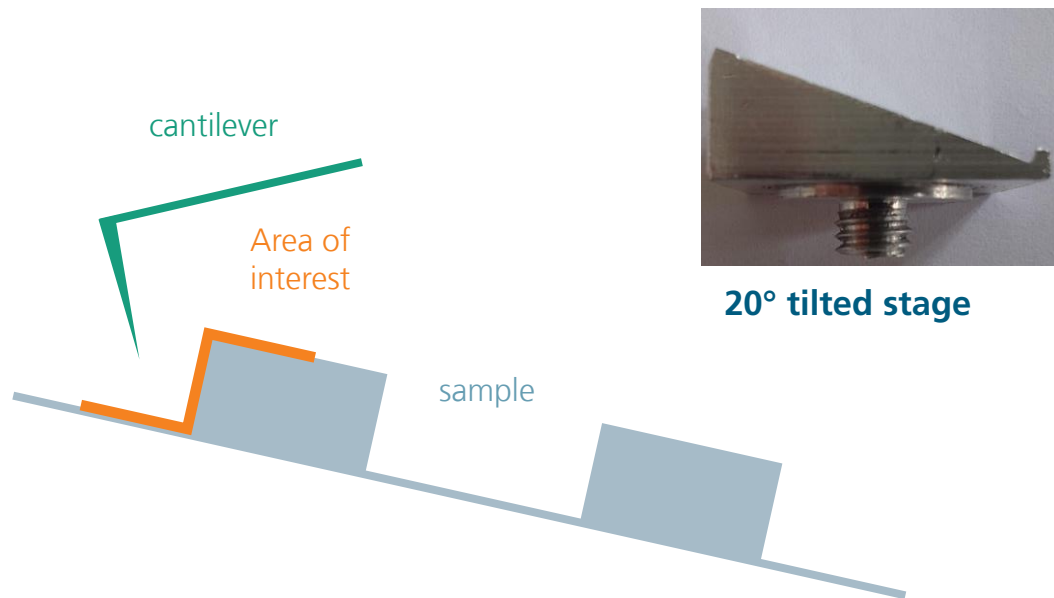
- low surface roughness of 2 Å is improved on SiCOI
- ALE is not inducing surface roughness

	Standard SiC	C-face EPI	SiCOI
EPC in Å/cycle	3.7 ± 0.2	2.5 ± 0.2	2.6 ± 0.1

Tilted-stage AFM quantifies SiC sidewall roughness

Non-destructive measurement and data preparation

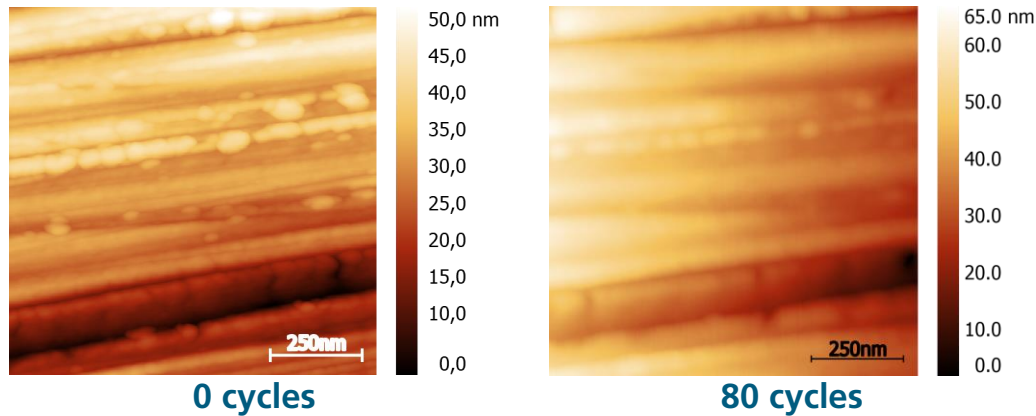
- **20° tilted stage** exposes trench sidewall to the AFM cantilever
- **PPP-NCHR cantilever:** 322 kHz resonance frequency; 42 N/m force constant
- **Feature height:** 1.0–1.2 μm



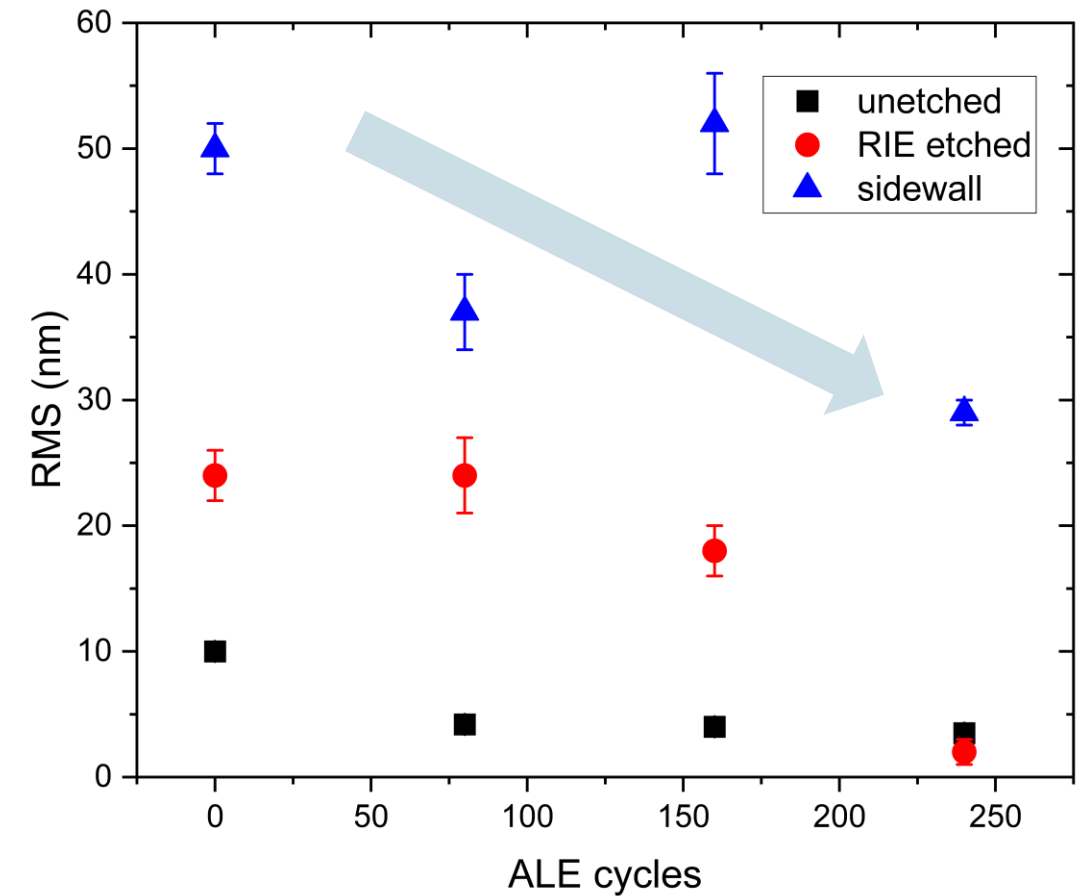
ALE reduces SiC sidewall roughness over 240 cycles

Standard 4H-SiC test structure | same trench feature

- **Measurements** cover initially unetched surface, RIE-etched surface and sidewalls
- **ALE-Cycle series:** 0, 80, 160 and 240 ALE cycles



ALE reduces surface and sidewall roughness and could support higher-Q photonic devices.

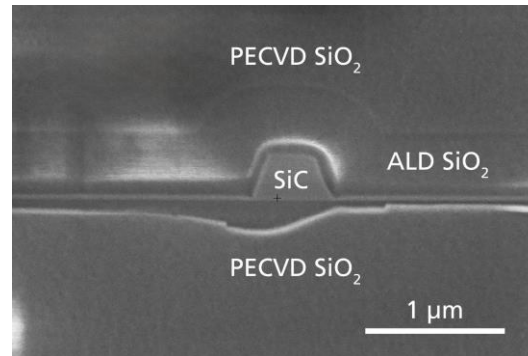
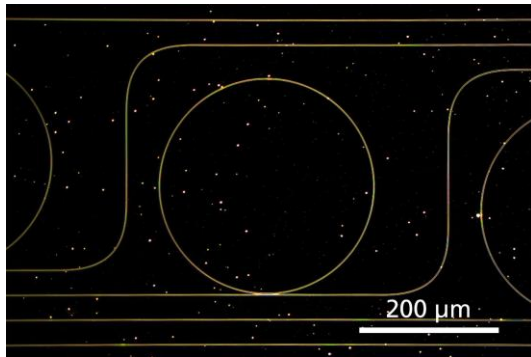


SiC Photonics @ IISB

Atomic layer processing for SiC for applications in photonic and quantum communication



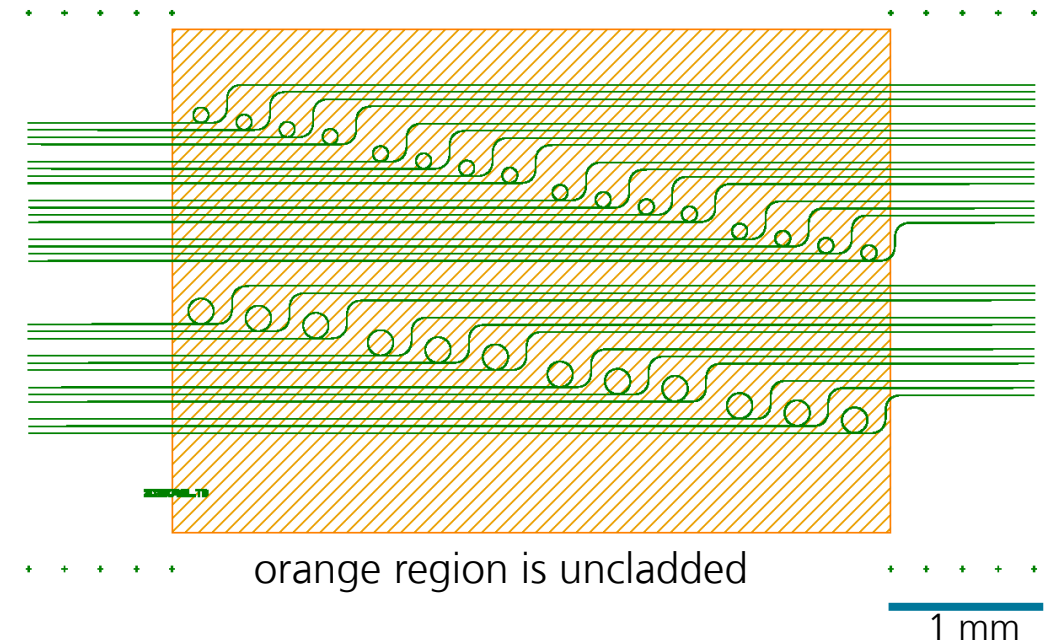
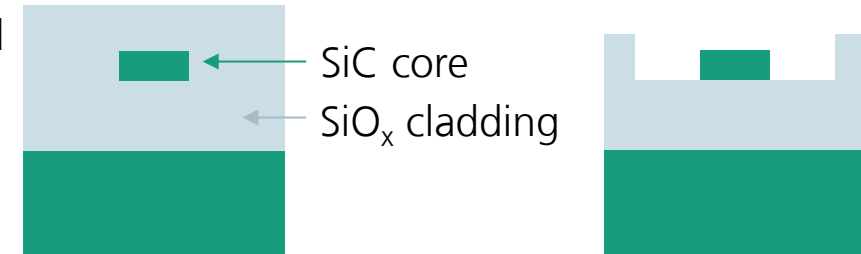
- Silicon carbide (SiC) promising material platform for photonic integrated circuits (PICs) and miniaturized solid-state quantum systems
- @IISB → Atomic Layer Processing for SiC for Applications in Photonics and Quantum Communication



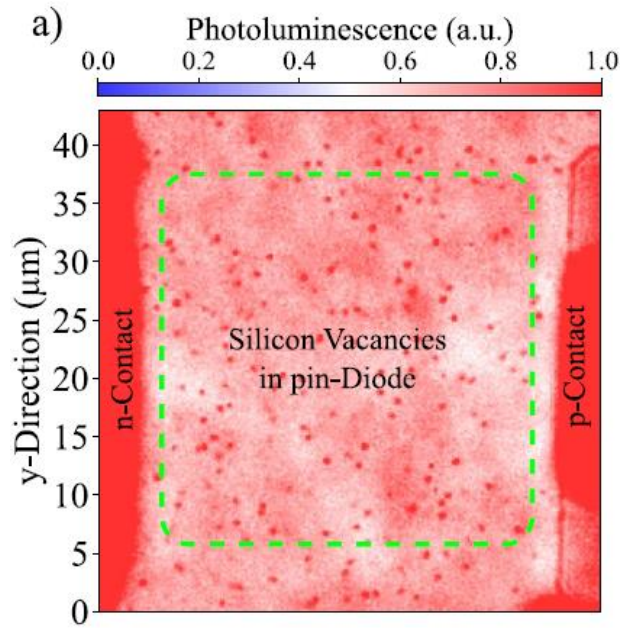
© Pascal Del'Haye / MPL

Develop ring resonators and waveguides with

- optical losses < 0.2 dB/m
- Q-factor > 100,000

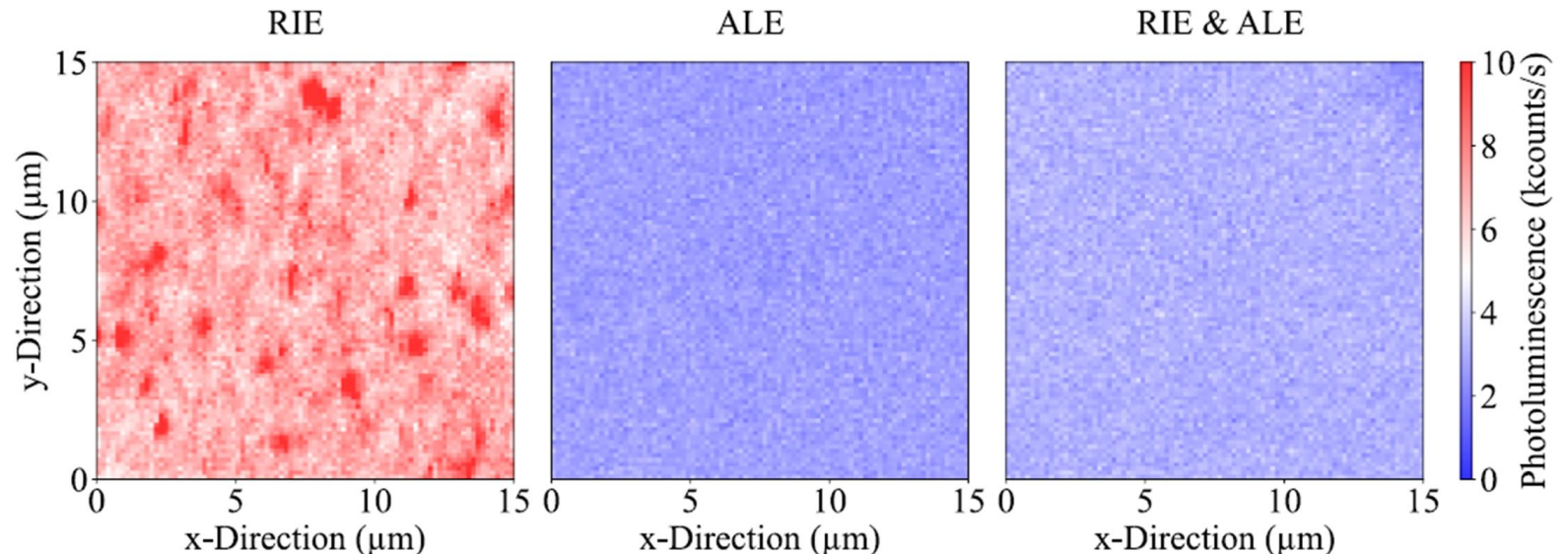


Atomic layer etching and its benefits for detectors



- Low surface roughness
- Less surface defects beneficial for various types of detectors

- CMOS-fabricated lateral 4H-SiC pin diode with generated color centers
- PL xy-scan reveals high background noise
- Passivation layers and crystal damage reduce coherence and broaden excitation linewidths
- Focus: strategies to minimize processing-induced PL noise



Nano Letters by J. Schwarberg "Impact of Surface Treatment on Noise in PL-Measurements of Silicon Vacancies in 4H-SiC Lateral pin-Diodes"

Summary

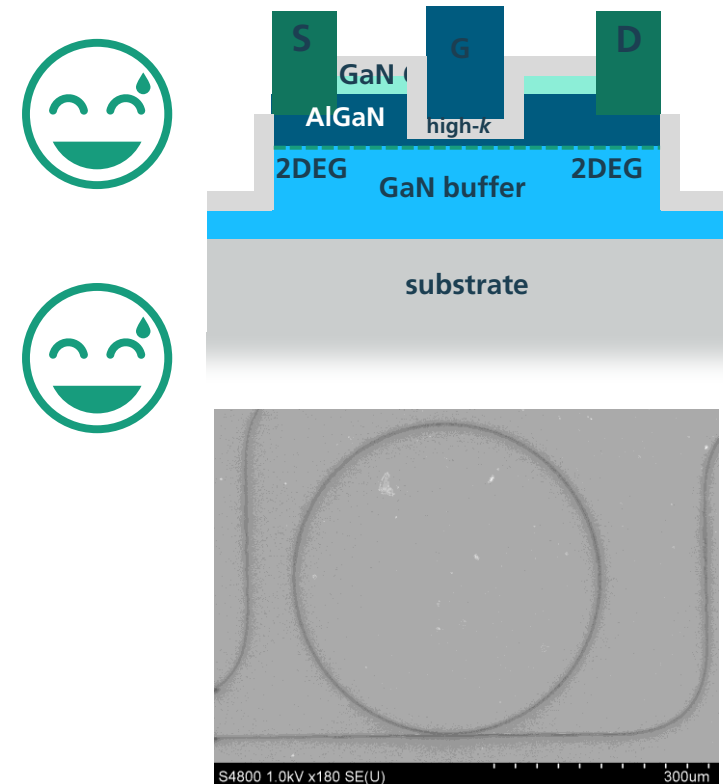
Development and characterization of ultra wide band gap (UWBG) (test) devices

Nitrides

- Development of device process steps for e-mode HEMTs

SiC

- Development of device processing for photonics and quantum electronics





Anita Patelli & Michele Perego



Fraunhofer-Institut für Integrierte
Systeme und Bauelemente-
technologie IISB

Thanks to our team and to you for our attention!

Dr. Franziska Beyer
Group Manager Spectroscopy and Test Devices
Tel. +49 3731 2033-103
Franziska.Beyer@iisb.fraunhofer.de

Fraunhofer Institute for Integrated Systems and Device Technology
Am S. Niclas Schacht 13
09599 Freiberg



https://www.iisb.fraunhofer.de/en/research_areas/energy_materials/spectroscopy-testdevices.html

