

Numerical Modeling of Residual Stress-Induced Wafer Warpage in 4H-SiC Substrates

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Motivation

- During PVT growth, thermomechanical stresses are generated, some of which remain in the crystal as residual stresses.
- Residual stresses influence mechanical and geometrical properties of the wafer¹.

→ Negative impact on device processing
(Step flow in epi, wafer handling, alignment in lithography)

- Goal: Numerical simulation of bow for given residual stress for bare and epitaxial SiC wafers.**
 - Validate model using experimental data
 - Predict maximum allowable residual stress for bare and epi wafers
 - for certain bow limits
 - for different wafer diameters and thicknesses

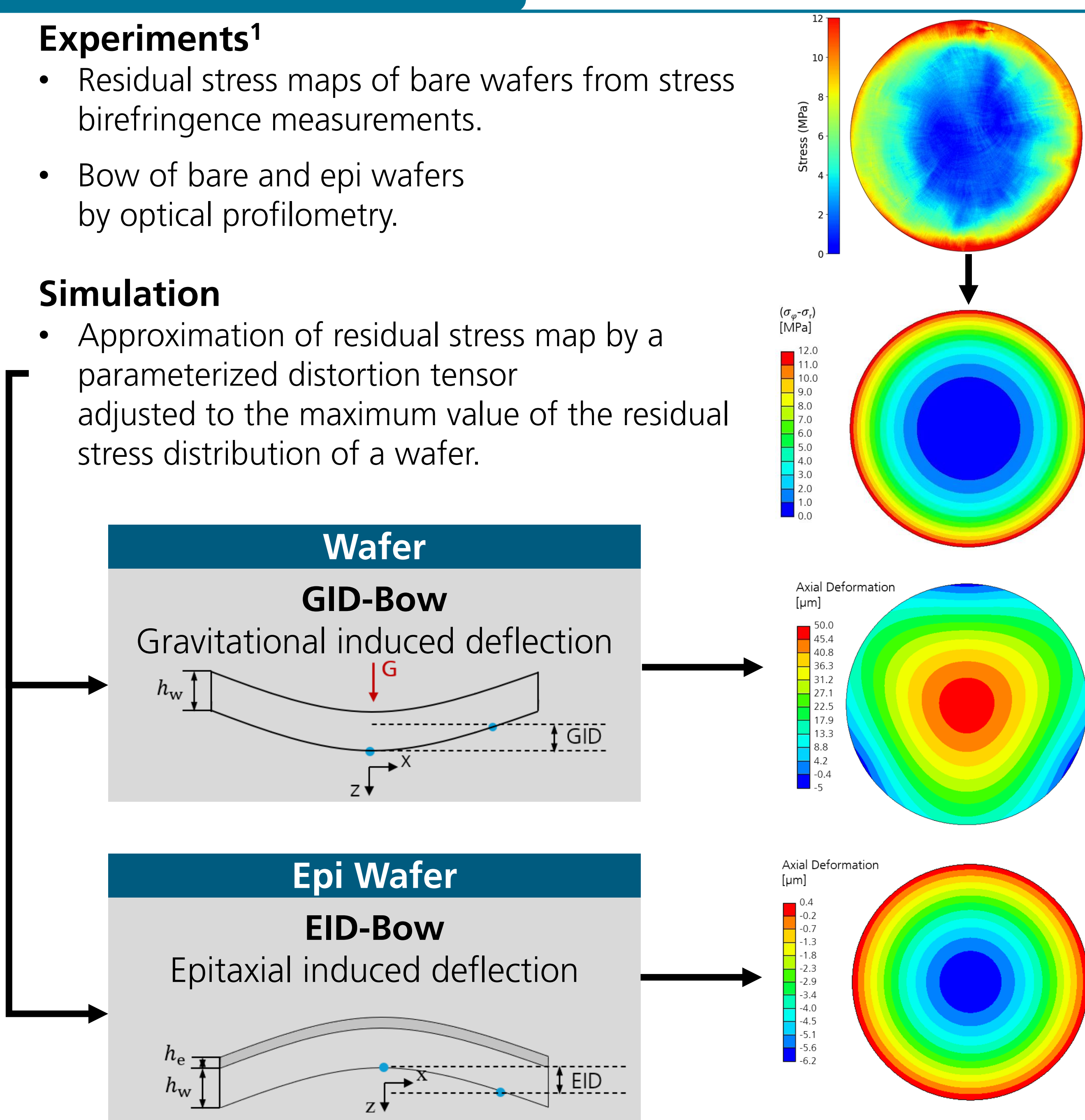
Approach

Experiments¹

- Residual stress maps of bare wafers from stress birefringence measurements.
- Bow of bare and epi wafers by optical profilometry.

Simulation

- Approximation of residual stress map by a parameterized distortion tensor adjusted to the maximum value of the residual stress distribution of a wafer.



Theoretical Model

- 3D finite element model of a SiC wafer in Ansys Mechanical taking into account anisotropic material properties.
- Geometrically nonlinear calculation of deflection w and stress σ ($=N/t$) under consideration of membrane forces N_r und N_ϕ (Kármán equation):

$$D \nabla^4 w(r) = q(r) + N_r(r) \frac{d^2 w}{dr^2} + \frac{N_\phi(r)}{r} \frac{dw}{dr}$$

D : Bending stiffness
 q : Area Load
 w : Deflection

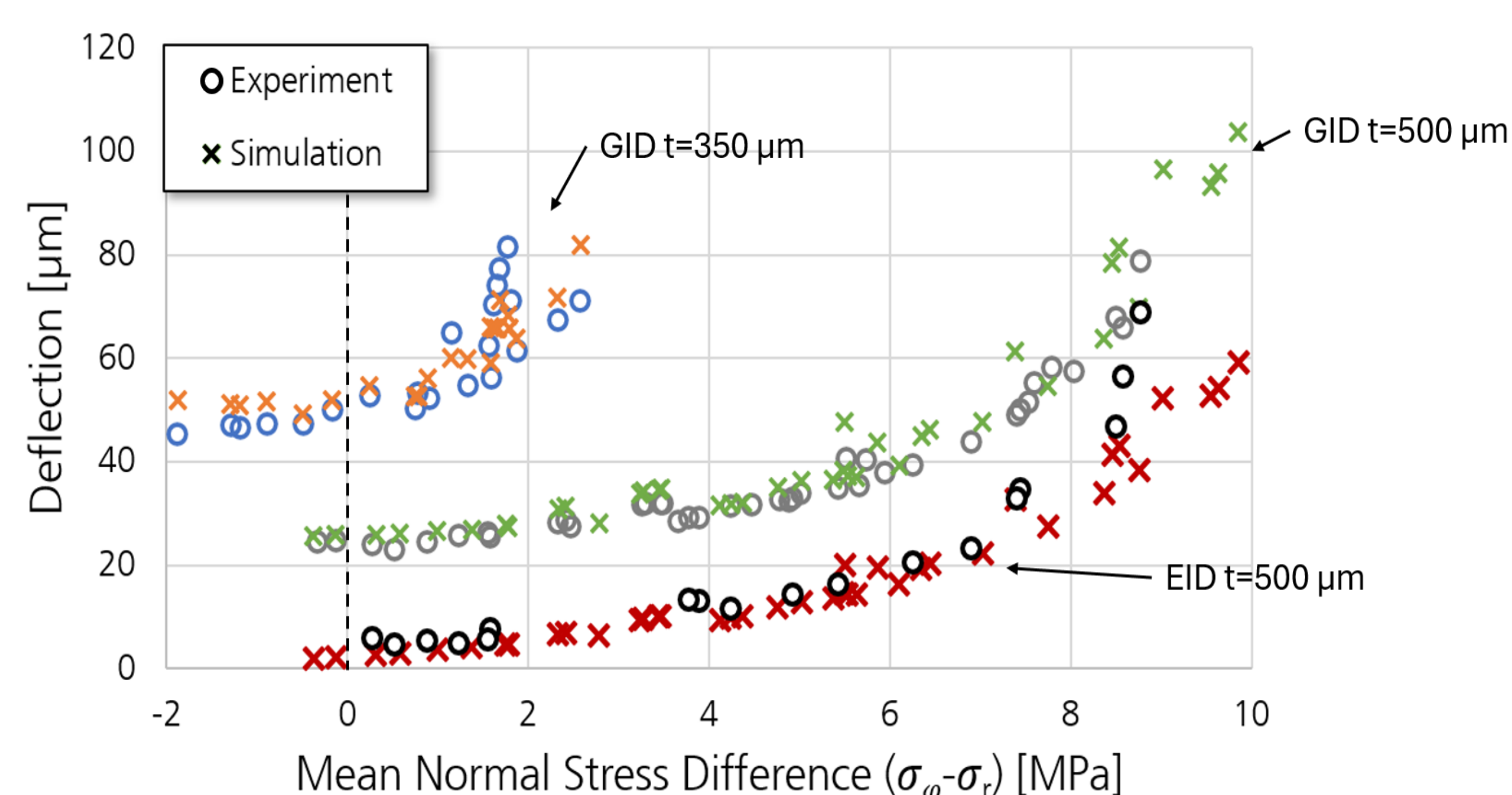
- Specification of local residual stress state σ via a parameterized distortion tensor.
- For epi-wafer:
 - Same stress distribution as bare wafers.
 - Consideration of misfit strain caused by lattice mismatch, calculated after Jacobson et al.² between the n- doped, 12μm thick epi layer and the n+ doped wafer; verified via Stoney equation³.

$$\epsilon = \frac{\kappa \cdot t_w^2}{6 t_e}$$

t_w : Thickness of the wafer
 t_e : Thickness of the epi layer

Validation

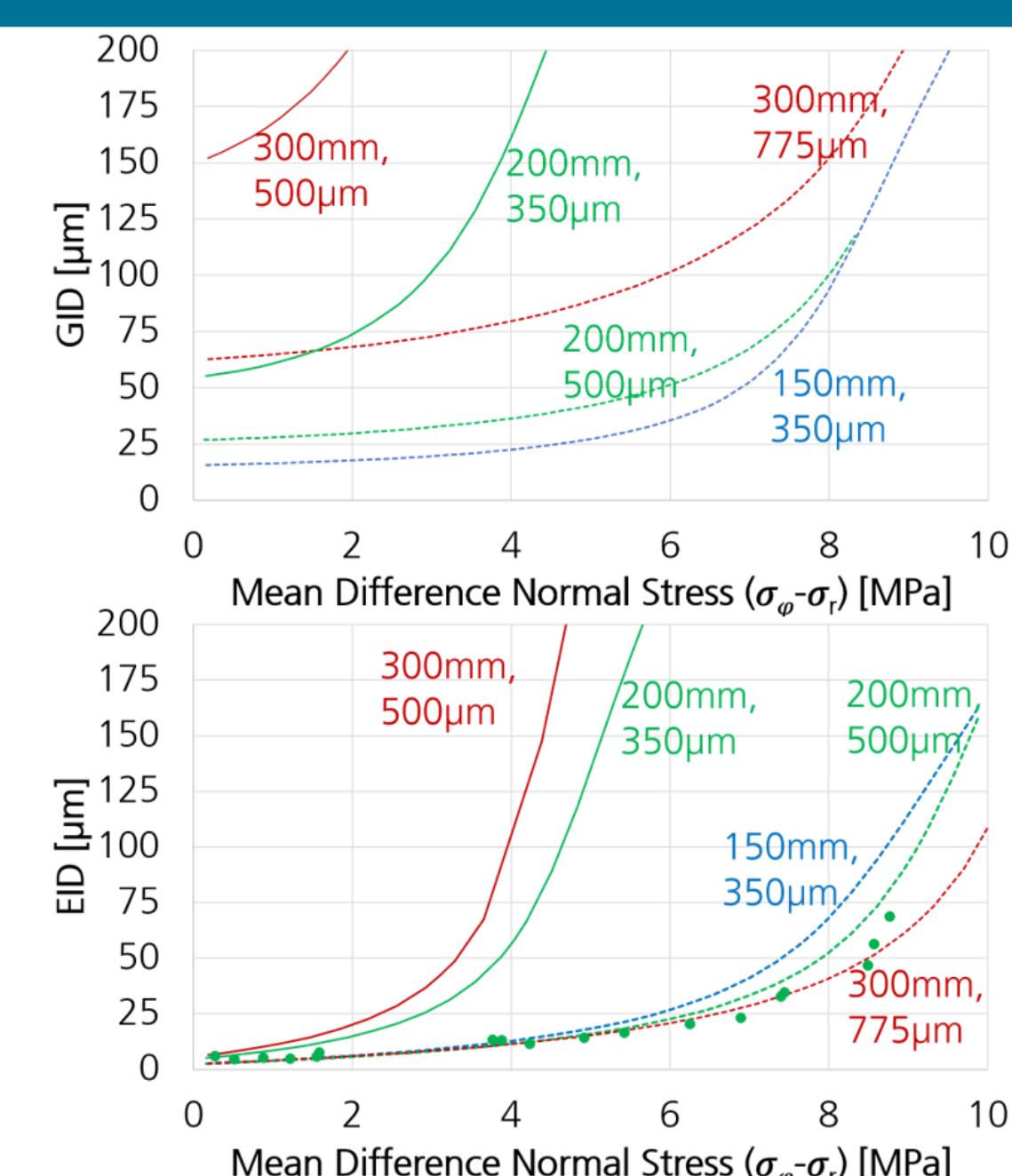
- Experimental data of residual stress and GID of 350μm&500μm thick 200mm wafers.
- Experimental data of EID of the same 200mm wafers with 500μm thickness.
- Calculation of GID and EID using the parameterized distortion tensor adjusted to the maximum measured stress value of a wafer.



Comparison of the calculated GID and EID to experimental data¹ for 200 mm SiC wafers with a thickness t of 350 μm and 500 μm

- The higher the stress difference ($\sigma_\phi - \sigma_r$) → the higher the deflection (GID & EID).
- The thinner the wafer → the higher the deflection for the same stress difference.
- Smaller deflection after epi for the same stress difference due to the tensile stress within epilayer according to the Stoney equation.

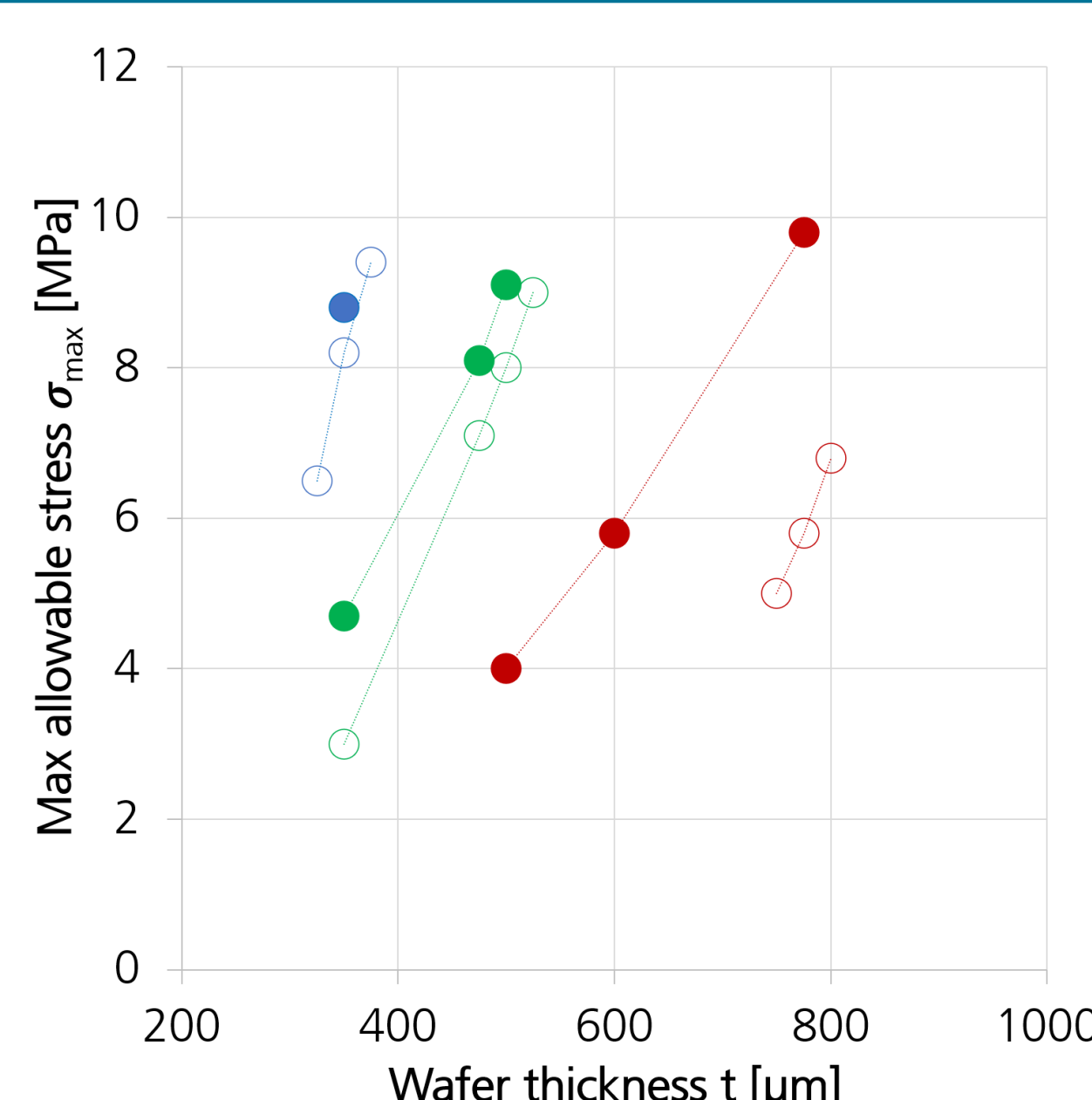
Predictions for 300mm Wafers



- Significant GID of 300mm/775μm wafers even in stress-free state, similar to 200mm/350μm wafers but with small stress dependence.
- Enormous GID of 300mm/500μm wafers in stress-free state, which further increase rapidly with stress.
 - May pose severe challenges to wafer handling tools.
- Less severe impact of diameter for the EID.
 - Similar results for 300mm/500μm wafers as for 200mm/350μm wafers with slightly higher sensitivity on stress.

Conclusion

- A numerical model was set up in Ansys Mechanical to calculate bow of bare (GID) and n- doped, 12μm thick epi (EID) SiC wafers for given parameterized distortion tensor
- The model was evaluated by experimental data obtained from stress birefringent measurements and optical profilometry for 200mm bare and epitaxial wafers



σ_{max} for bow of 100μm of GID (open circles) and EID (filled circles)

- GID (especially relevant for wafer handling) is most critically influenced by the wafer diameter.
- EID is mostly connected to aspect ratio of the wafer.
 - 300mm/500μm wafers exhibit a similar behavior as 200mm/350μm wafers.
 - 300mm/500μm wafers seem to be feasible in general as long as enormous GID can be managed in automated wafer handling.

- The model was used to investigate GID and EID of 300mm SiC wafers
- For 300mm bare wafers the maximum allowable stress for a GID < 100μm is the same range as for smaller diameters if the thickness is between 750-800μm
- For 300mm/775μm epi wafers EID remains < 100μm for σ_{max} < 10MPa in the bare wafer, which however will have a GID >> 200μm

References

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- B. Kallinger et al., J. Cryst. Growth 349, 43-49 (2012).

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