

Data-driven Remaining Useful Life Prediction for Si IGBT in a Digital Twin Architecture



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Motivation & Challenge

- Direct current (DC) distribution systems gain importance due to increasing application of DC loads and generation sources.¹
- Absence of current zero crossing poses challenges on fast and selective fault protection in DC grids.²
- Semiconductor circuit breakers (SCCBs) address this but degrade during operation.^{2, 3}
- Accurate remaining useful life (RUL) prediction is needed to avoid unplanned downtime.

RUL prediction of SCCBs: Bond wire lift-offs (BWLOs) cause abrupt, discontinuous changes in degradation indicators, posing a fundamental challenge for RUL prediction algorithm

Project Context – d.gitaLE

- DC SCCBs with SiC MOSFETs and integrated sensors,
- ML algorithms for RUL prediction,
- Demonstrator operated under real-world load profiles,
- Digital Twin (DT) integrating historical, live, and simulation data as well as digital services for RUL prediction.

Current investigation: Development and validation of RUL prediction algorithms capable of handling BWLO, using Si IGBT power cycling datasets from product qualification

Degradation Indicators & Power Cycling Dataset

Degradation Indicators

- Package-level failures account for the majority of failures,⁴
- $V_{CE(sat), norm}$ as indicator for bond wire degradation,
- $R_{th, norm}$ as indicator for solder layer fatigue.

Power Cycling Dataset

- Accelerated power cycling data from 34 commercially available Si IGBT modules.
- End-of-life (EOL) criterion:
 - $V_{CE(sat), norm}$ reaches 105% of pristine state value.
 - $R_{th, norm}$ reaches 120% of pristine state value.
 - For $V_{CE(sat), norm}$ 30 of 34 devices reach EOL criterion while for $R_{th, norm}$ no device reaches the EOL criterion.
- High device-to-device variability driven by BWLOs: EOL range within devices is 36% of maximum lifetime.

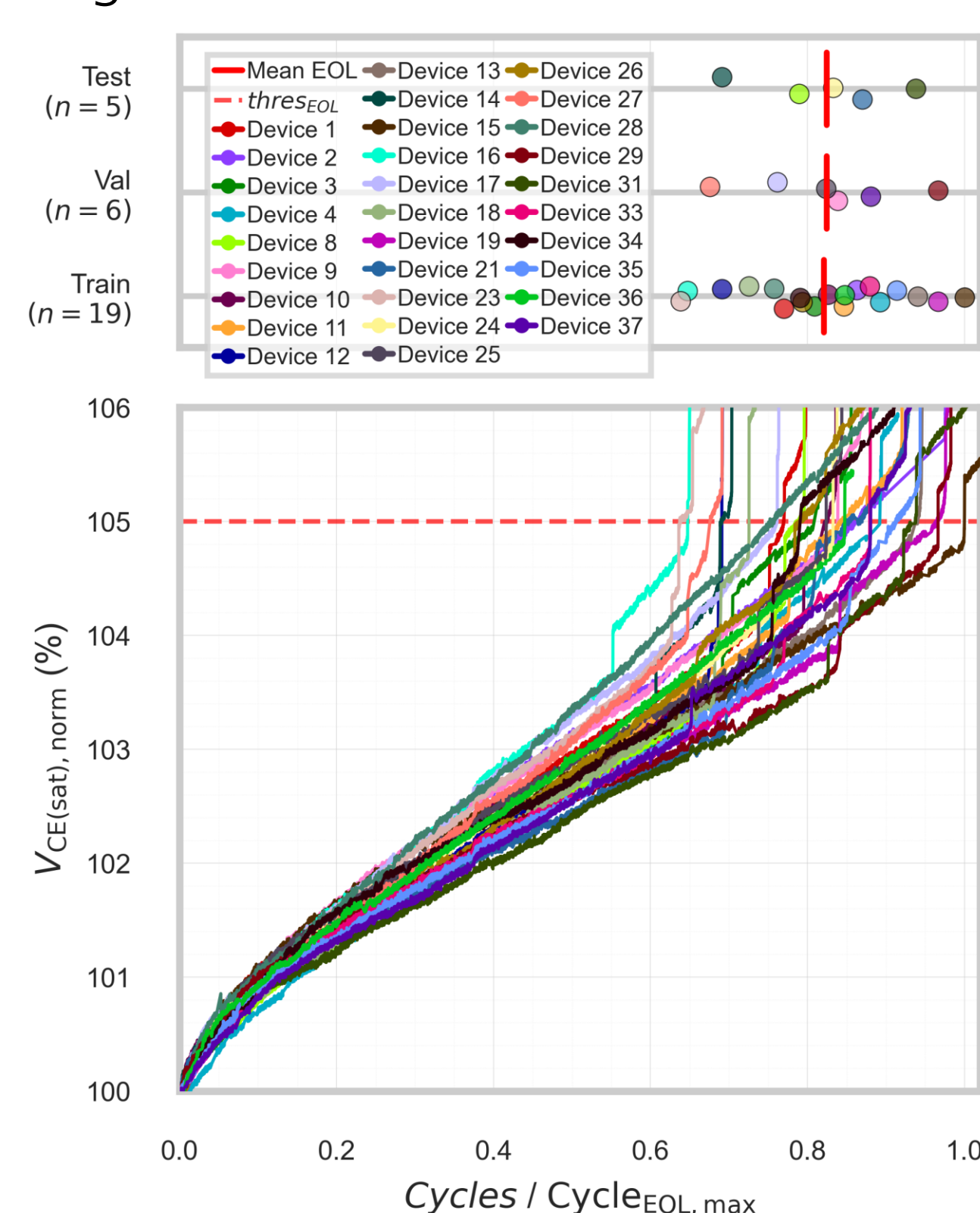


Fig 1: Si IGBT power cycling degradation characteristics: $V_{CE(sat), norm}$ degradation trajectories showing device-to-device variation & discontinuities with corresponding end-of-life cycle distribution.

LSTM-Based RUL Prediction Model

- Long Short-Term Memory (LSTM) networks are a variant of Recurrent Neural Networks (RNNs), designed to learn long-term dependencies through internal gate mechanisms.
- The recurrent architecture maintains a hidden state across time steps, enabling the network to capture temporal dependencies in sequential data.
- LSTMs are therefore particularly suitable for RUL prediction tasks, where degradation patterns evolve over extended time horizons.

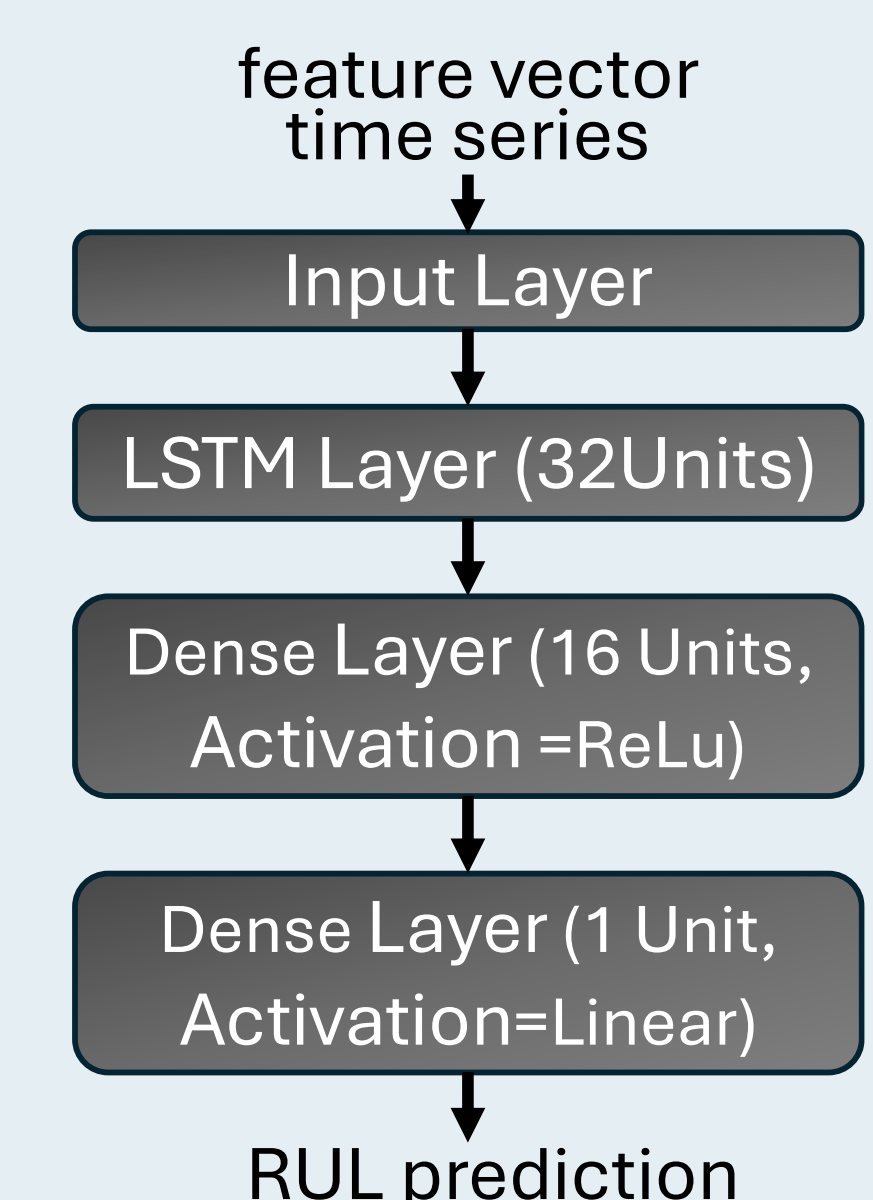


Fig 2: LSTM Neural Network Architecture

Hyperparameter

Sequence length	200 steps
Downsampling	Every 600th cycle
Stride	50
Optimizer	Adam, learning rate = 0.001
Loss / Batch	MAE / 16
Early Stopping	Patience 20
Epochs trained	47 (early stop)

Input Features

$V_{CE(sat), norm}$ (%)	Measured and normalized $V_{CE(sat)}$
Cycle	Power cycle number
ΔT_{vj} (K)	Junction temperature difference within the power cycle
$\Delta T_{vj, norm}$	Normalized junction temperature difference
$T_{vj, max}$ (°C)	Maximum junction temperature within the cycle
$\sum V_{CE(sat), norm}$	Cumulative sum of $V_{CE(sat), norm}$
P_{loss} (K)	Power loss during the cycle
$\overline{\Delta T_{vj}}$ (K/cycle)	Average temperature difference per cycle

Digital Twin Integration

- The DT integrates the LSTM models.
- This extends DT RUL prognostics from [3] with RUL prediction and Kalman filter approaches using continuous state-model updates.
- The database layer is the central data hub with an extended schema for prognostic outcomes.
- The DT RUL prognostics also supports other algorithms with minor schema adaptations.

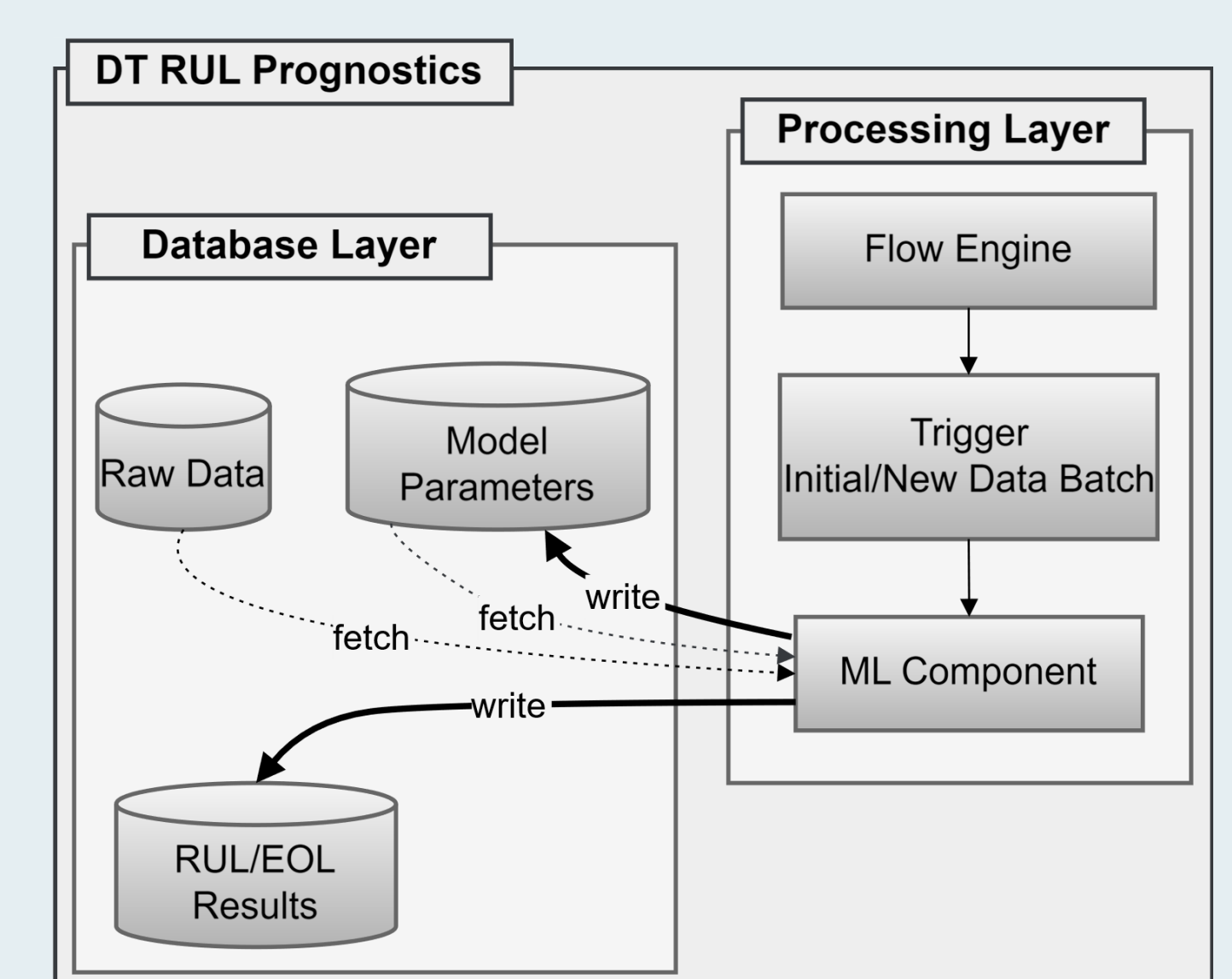


Fig 3: Architecture of the digital twin for RUL prognostic

¹ H. Lotfi, A. Khodaei, S. Bahramirad, and M. Bollen, "Optimal Design of Hybrid AC/DC Microgrids," 2017, doi: 10.48550/arXiv.1710.00094.

² D. Liu et al., "A Predictive Maintenance Concept for LVDC Power Electronics-Based Circuit Breakers Using Artificial Intelligence," in *PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, pp. 2808–2815.

³ L. Köhler et al., "Machine Learning and Digital Twins for RUL Prediction of DC Semiconductor Circuit Breakers," in *PCIM Conference 2025; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 204–213, doi: 10.30420/566541026.

⁴ F. Hosseinabadi, S. Chakraborty, S. K. Bhoi, G. Prochart, D. Hrvanovic, and O. Hegazy, "A Comprehensive Overview of Reliability Assessment Strategies and Testing of Power Electronics Converters," *IEEE Open J. Power Electron.*, vol. 5, pp. 473–512, 2024, doi: 10.1109/OJPEL.2024.3379294.

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Results & Discussion

RUL prediction in an evaluation window of 150 000 cycles before EOL with error bounds of $\pm 5\%$ ($\pm 16\,711$ cycles) of average device lifetime (334 227 cycles).

Visual Assessment of RUL Traces

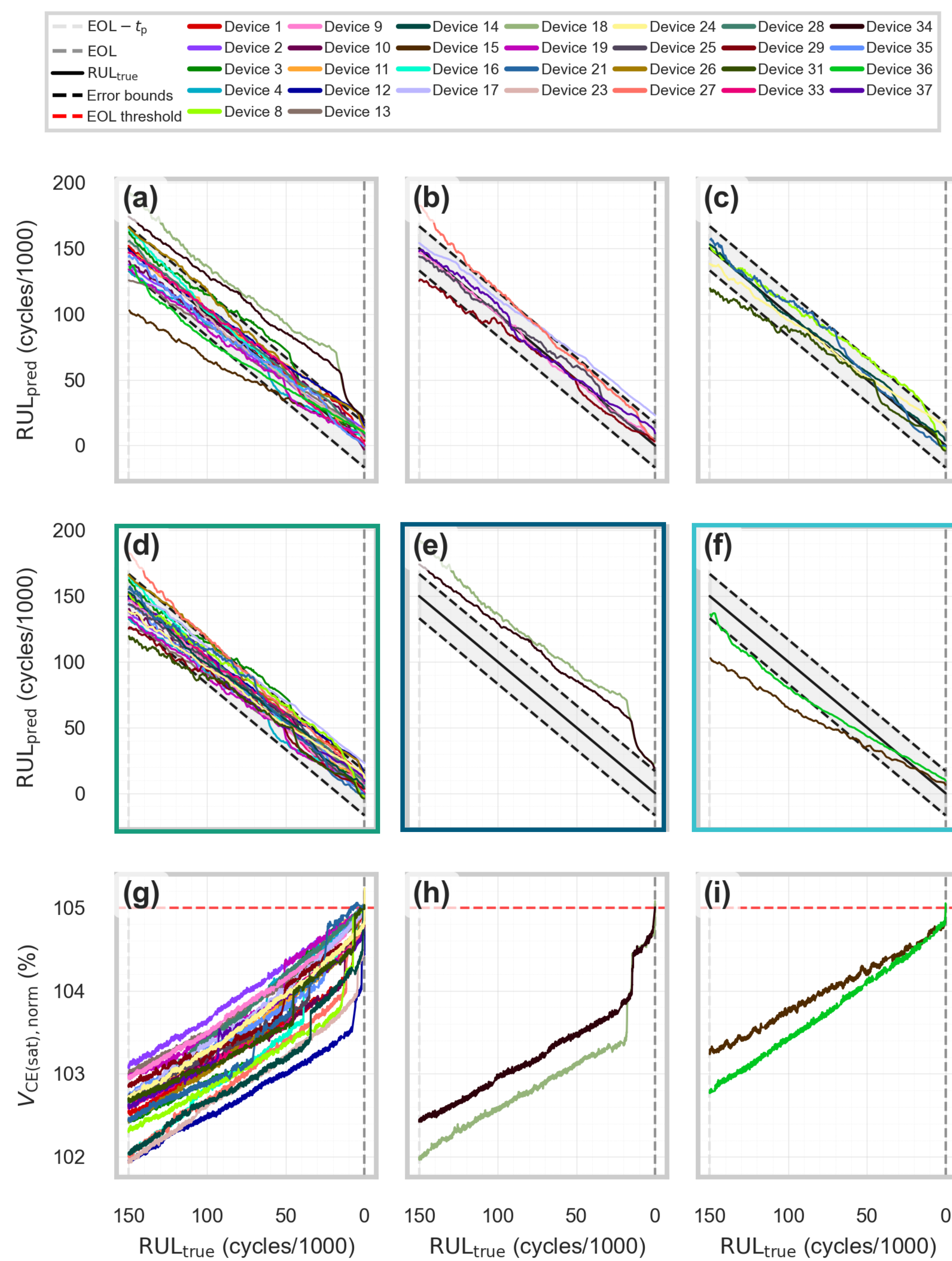


Fig 4: (a-c) RUL predictions versus true RUL for training, validation, and test sets with $\pm 5\%$ error band (grey). (d-f) Device stratification: (d) accurate predictions, (e) overestimation cases (devices 18, 34), (f) underestimation cases (devices 15, 36). (g-i) Corresponding $V_{CE(sat), norm}$

Performance Metrics

- 82 % of all RUL predictions fall within the defined error band across training, validation, and test sets.
- The test set yields a Mean Absolute Error (MAE) of 7 070 cycles, corresponding to 2.1 % of average device lifetime, indicating high prediction accuracy relative to total operational duration

Dataset	C_{emp}	MAE (% of avg. lifetime)	R^2
Training	79%	3.3 %	0.87
Validation	81%	2.5 %	0.93
Test	90%	2.1 %	0.90

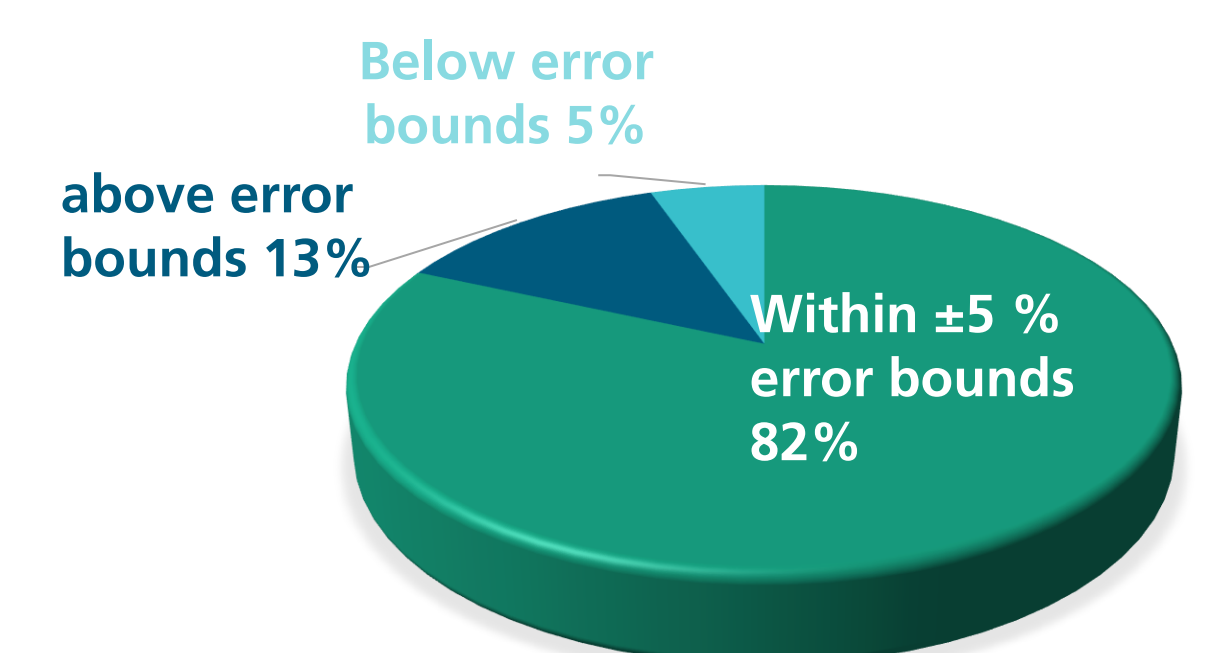


Fig 5: RUL predictions for training, validation and test set.

Device Specific Analysis

Majority – Accurate (d):

- Predictions stay within error band despite BWLOs,
- Model effectively compensates BWLO-induced jumps,
- Physically relevant degradation patterns learned.

Devices 18 & 34 – Overestimation (e):

- Unusually large BWLO jumps near EOL,
- Earlier BWLOs compensated; extreme event magnitudes underestimated,
- BWLO at EOL: too little time for BWLO compensation.

Devices 15 & 36 – Underestimation (f):

- No significant BWLO activity until late stage,
- Model anticipates statistically typical BWLO timing,
- Unexpected late-stage BWLO triggers RUL overestimation close to EOL.

Results suggest that the model is able to compensate for BWLO-induced degradation jumps in most cases, while observed prediction deviations appear to be linked to atypical BWLO timing or magnitude near EOL rather than general model limitations.

Conclusion

- LSTM-based RUL prediction was developed and integrated into the digital twin framework for power semiconductors.
- Validation with Si IGBT power cycling data showed good RUL prediction performance and robustness to BWLO-related degradation changes.
- The model captures physically relevant degradation patterns and adaptively adjusts its RUL estimates following BWLO-induced discontinuities in degradation indicator traces.

- In two cases where BWLOs occurred close to EOL, the limited remaining time for adjustment led to increased prediction errors. Incorporating confidence intervals into RUL estimates could enhance reliability assessment in such scenarios.
- Future work will address uncertainty quantification and validation with SiC MOSFET-based SCCB data under real-world operating conditions.